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Advancements in KM3NeT Acquisition Electronics: Current Status and Upgrades

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The KM3NeT Collaboration is constructing and managing two deep-sea neutrino telescopes on the Mediterranean Sea floor. These telescopes are composed of networks of light detectors enclosed in pressure-resistant glass spheres, known as digital optical modules. Each module contains 31 photomultipliers, each with a 3-inch diameter, along with acquisition electronics. The detection units consist of vertical strings where these digital optical modules are mounted. In the initial construction phase, several dozen detection units were manufactured incorporating over 20,000 photomultipliers that are actively collecting data. Upon completion, the telescopes will feature more than ten thousand digital optical modules synchronized at the level of the nanosecond, forming one of the most intricate operational and synchronized networks globally. This work provides an update on the current status of the Digital Optical Module and DU Base acquisition electronics, highlighting upgrades to key components, such as the central logic board and the base module backplane.

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1. Introduction

The KM3NeT Collaboration is constructing and operating two large-scale deep-sea neutrino telescopes located in the Mediterranean Sea. These detectors are designed to observe neutrino interactions by capturing the Cherenkov light emitted by secondary particles using a dense three-dimensional array of light sensors. Each sensor, known as a Digital Optical Module (DOM) [1], consists of a pressure-resistant glass sphere housing 31 3-inch photomultiplier tubes (PMTs) along with integrated data acquisition and control electronics.

The DOMs are deployed along vertical structures called Detection Units (DUs), each comprising 18 DOMs. In the current construction phase, a substantial number of DUs have been installed, incorporating over 20,000 PMTs actively collecting data. Once fully operational, the two KM3NeT telescopes will feature an extensive and highly synchronized network exceeding 10,000 optical modules—representing one of the most sophisticated real-time underwater detection systems in the world.

This contribution provides an overview of the present status of the acquisition electronics in KM3NeT [2–4], with emphasis on the ongoing upgrade of critical components such as the Central Logic Board (CLB) [5, 6], Signal Collection Boards, Switching Core Board, and Glenair backplane. These upgrades are designed to enhance data throughput, increase system robustness, and improve the overall efficiency of the KM3NeT data acquisition system. The results presented in this contribution highlight the recent progress in the electronics development and demonstrate the readiness of the system to support long-term, high-precision neutrino observations.

Figure 1: KM3NeT Digital Optical Module.

2. KM3NeT hardware

The Digital Optical Module (DOM) is the core element of the KM3NeT telescope. Each DOM integrates 31 photomultiplier tubes (PMTs), along with all necessary electronics for power management, data acquisition, and internal control. The central component of the DOM's electronics is the *Central Logic Board* (CLB), which manages all operational aspects, including communication, synchronization, and signal processing.

Connected to the CLB is the *Power Board* (PB), which is responsible for generating the multiple voltage levels required by the DOM subsystems. Each PMT is interfaced through a dedicated *base board*, which supplies the high voltage to the PMT and digitises its analog signal before sending it to the CLB.

The digitised PMT signals are transmitted to the CLB through two *Signal Collector Boards* (SCBs). Additionally, each DOM includes a *Nanobeacon* device for timing calibration, which utilizes a programmable pulsed LED [7].

Figure 1 shows a DOM.

2.1 Central Logic Board

The CLB [8, 9] is a multilayer electronic board that governs the operation of the DOM, covering acquisition, synchronization, environmental monitoring, and communication interfaces. Its core is a Xilinx Kintex-7 Field-Programmable Gate Array (FPGA), which implements all control logic and signal processing algorithms. The FPGA handles both the acquisition of optical signals from the PMTs and acoustic signals from the integrated piezoelectric sensor used in the positioning system. The CLB also hosts the acquisition firmware and embedded software [10, 11]. All events—optical and acoustic—are time-stamped using the White Rabbit (WR) synchronization protocol, which ensures sub-nanosecond synchronization accuracy across the entire KM3NeT array.

2.2 Power Board

At the DOM interface, a voltage converter steps down the external high-voltage supply of 375–400 V DC, delivered via the KM3NeT DU cable, to a stable 12 V DC. The Power Board (PB) receives this 12 V input and generates the full set of required voltages: 1 V, 1.8 V, 2.5 V, two 3.3 V rails (one dedicated to the CLB and another to the PMT base boards), 5 V, and an adjustable output ranging from 5 to 30 V for calibration components [12]. Successful voltage generation is indicated by the activation of a *Power Good* signal. The PB also includes two analog-to-digital converters (ADCs) that continuously monitor voltage and current levels for all output rails, enabling remote diagnostics and fault detection.

An analysis has been conducted to accurately select the voltage converters, taking into consideration the current requirements for each power supply rail. This has enabled the optimization of the board's efficiency. The total power consumption of a DOM is approximately 6 W. The PB incorporates a sequential start-up of the voltages, ensuring proper power supply to the FPGA. This prevents excessive currents during start-up that could damage the system.

2.3 Signal Collection Board

The Signal Collection Boards (SCBs) serve as the interface between the PMT base boards and the Central Logic Board (CLB), handling both data transmission and configuration control. The Low Voltage Differential Signals (LVDS) produced by the PMT bases are routed to the CLB via two SCBs.

The first board, referred to as *SCB Large*, handles the signals from the 19 PMTs installed in the lower hemisphere of the DOM. The second, known as *SCB Small*, is responsible for the 12 PMTs located in the upper hemisphere. Beyond data transfer, both SCBs also manage the communication of configuration settings and monitoring commands from the CLB to the PMTs.

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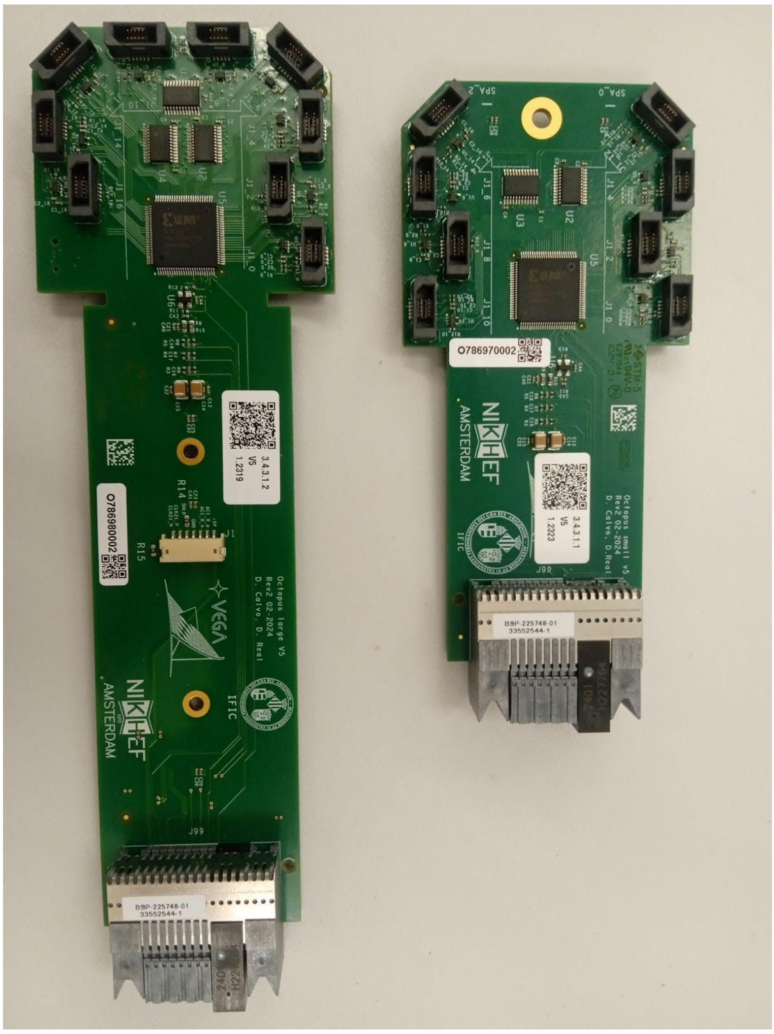

Figure 2: Set of Signal Collection Boards of the latest version.

Each SCB integrates several key components, including:

- A Molex 754332104 connector for interfacing with the PMT bases,
- A Xilinx CoolRunner Complex Programmable Logic Device (CPLD) for logic control and status monitoring,
- Current sensors and limiters to ensure safe operation of each PMT,
- A multiplexer for managing multiple I^{2}C communication lines,
- A dedicated link for relaying acoustic signals from the piezoelectric sensor to the CLB.

This architecture ensures efficient signal routing, robust monitoring, and precise control of all PMTs within the DOM. Figure 2 shows a set of SCBs.

2.4 White Rabbit Switch Hardware

The KM3NeT experiment is an infrastructure composed of thousands of DOMs, which are responsible for detecting and processing the Cherenkov radiation induced by the charged particles produced in neutrino interactions, in order to reconstruct the trajectory and energy of the incident neutrinos. The DOMs, separated by tens of meters, each contain acquisition electronics and operate on independent time references. Therefore, precise nanosecond synchronization of all DOM clocks is critical. To achieve this, KM3NeT employs the White Rabbit (WR) protocol [13, 14], a high-precision time synchronization system built on top of the Ethernet physical layer. WR establishes a hierarchical network topology using bidirectional *timeTransmitter–timeReceiver* links, where the DOMs act as timeReceivers and the White Rabbit Switches (WRSs) serve as timeTransmitters. This setup enables both synchronization and data transmission to be carried over a single optical link. The WRS consists of two main electronic boards: the Switching Core Board (SWCB) and the backplane.

2.4.1 Switching Core Board

The switching core board is implemented in the microTCA standard, which provides a compact format with redundant power supply and remote management capabilities, designed to support high-throughput data rates. Due to the form factor constraints of the microTCA standard, the optical connectors for the 18 communication ports are placed on a secondary card connected via two QSS-048-01-LD-DP mezzanine connectors. A reliability analysis based on the FIDES methodology revealed that the decoupling capacitors were the most significant contributors to the board's failure rate (measured in FIT—Failures In Time). To address this, a redesign was carried out using capacitors with a better voltage derating factor, which reduced the expected failure rate by approximately 66%. Additionally, the testing protocols for the switching core boards were enhanced to improve early fault detection and overall reliability.

2.4.2 Backplane

The backplane, which connects the switching core to the optical transceivers, has also been redesigned. The first version of the WRS backplane used Glenair optical transceivers due to their compact size, low power consumption, and enhanced mechanical robustness—important factors given the operational constraints of KM3NeT.

In the latest version, the backplane has been adapted to integrate standard Small Form-factor Pluggable (SFP) modules instead of Glenair transceivers. This change aligns with the redesign of the switch and enables the use of commercially available high-performance optical modules, improving maintainability and long-term component availability. The updated backplane geometry also simplifies mechanical integration and thermal management.

3. Upgrade and new developments

3.1 Central Logic Board

The CLB has been designed with a total of 12 layers, consisting of 6 signal layers, 2 power planes, and 4 ground planes, symmetrically arranged around the power planes to optimize electromagnetic compatibility and thermal performance. The proximity of ground planes to signal layers

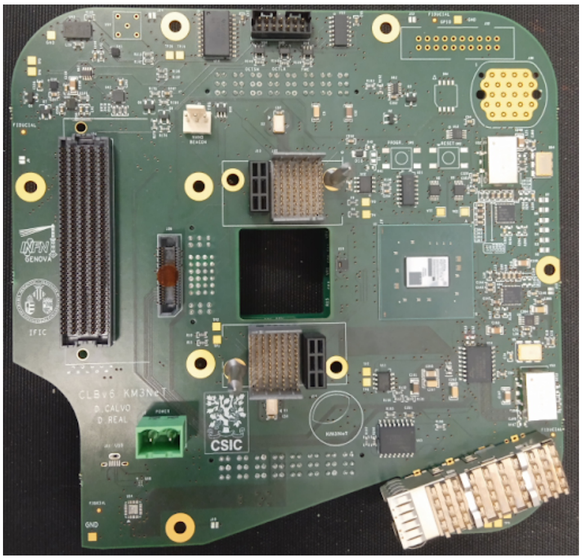

Figure 3: CLBv6, the latest of the versions developed for KM3NeT.

enhances signal integrity across high-speed traces. Particular care was taken in routing differential pairs to ensure a timing mismatch of less than 100 ps between PMT channels and under 20 ps between clock signals.

A reliability analysis was carried out using the FIDES methodology [15], yielding an estimated failure risk below 4% over 10 years. Additionally, signal integrity simulations demonstrated excellent performance in maintaining timing precision and noise immunity across critical signals.

Several key improvements have been made over the original CLB design. One of the most significant is the inclusion of a redundant clock circuit. Given the inaccessibility of the DOMs after deployment, a failure in the primary clock system would result in the permanent loss of the module. To mitigate this risk, a backup clock system has been incorporated, providing increased robustness.

Obsolescence of electronic components is another major challenge in long-term experimental deployments. Some components originally used in the CLB, such as the Molex connectors interfacing with the Signal Collection Boards, have become obsolete. A redesign of the board layout was therefore required, replacing the outdated Molex connectors with a new configuration based on SAMTEC connectors, tailored for KM3NeT requirements.

Furthermore, a new version of the CLB, known as *CLBv6* (see Figure 3), has been developed. This version integrates a high-speed Small Form-factor Pluggable (SFP) transceiver, enhancing communication capabilities and bandwidth for future applications. The CLBv6 is currently undergoing an extensive validation campaign to qualify its performance and reliability under the operational conditions of the KM3NeT infrastructure.

The Signal Collection Boards (SCBs) have also undergone a redesign due to component obsolescence. As with the CLB, the most critical issue was the discontinuation of the Molex connector that interfaces the SCBs with the CLB. This required the adoption of a new connector scheme based on SAMTEC components, specifically configured to meet the mechanical and electrical requirements of KM3NeT.

Figure 4: New version of the WRS to be installed in KM3NeT.

The updated SCB design has been integrated alongside the revised CLB within the DOM mechanical frame. This integration ensures compatibility and mechanical stability, while maintaining signal integrity and power distribution.

Following successful prototype testing, the production pipeline for the new SCB version has been initiated. Validation tests are currently underway with the updated SCBs installed in full DOM assemblies. These tests aim to confirm the reliability and performance of the redesigned electronics under real operational conditions. Once this validation phase is completed, mass production of the SCBs will start to support the continued deployment of KM3NeT detection units.

3.2 White Rabbit Switch

Currently, a new version of the switching core board is being developed. This updated design incorporates a mezzanine module dedicated to hosting the Small Form-factor Pluggable (SFP) optical transceivers, providing greater modularity, maintainability, and improved thermal management. The mezzanine-based approach facilitates future upgrades and addresses obsolescence challenges more effectively. Figure 4 shows the last version of the WRS. These upgrades to both the switching core board and the backplane components will ensure enhanced performance, improved long-term reliability, and increased flexibility in the deployment and maintenance of the White Rabbit timing infrastructure within KM3NeT.

4. Conclusions

The principal electronic boards used in the KM3NeT experiment have been presented in this work, detailing their fundamental roles within the system. Key upgrades and redesign strategies—focused on enhancing efficiency, reliability, and addressing component obsolescence—have been discussed. The implemented improvements have substantially increased the overall robustness and operational performance of KM3NeT. By proactively adapting to obsolescence challenges -by periodically analyzing, with the help of producing companies, the availability of components -these developments ensure sustained system functionality while minimizing failure risks.

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