Leap in Advancing of critical Quantum key distribution-spAce components (LaiQa)

Deliverable D4.2

Development of the PIC-based EPPS on-board source

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List of abbreviations

Term	Meaning
ADC	Analog-to-digital converter
APD	Avalanche photodiode
BSM	Bell state measurement
CW	Continuous wave
DAC	Digital-to-analog converter
DAQ	Data acquisition board
DWDM	Dense wavelength-division multiplexing
EPPS	Entangled photon pair source
FSR	Free spectral range
FWHM	Full width at half maximum
HR	High rate
HWP	Half wave plate
IM	Intensity modulator
ITU	International Telecommunication Union
KPI	Key performance indicator
LaiQa	Leap in advancing of critical Quantum key distribution space components
MRR	Micro ring resonator
OGS	Optical ground station
OS	Optical switch
PIC	Photonic integrated circuit
PM	Power Meter
QKD	Quantum key distribution
RMS	Root mean square
SNSPD	Superconducting nanowire single photon detector
SOI	Silicon-on-insulator
SPAD	Single photon avalanche diode
SPD	Single photon detector
TE	Transverse electric
TEC	Thermo-electric control
TM	Transverse magnetic

Executive Summary

This deliverable presents the full summarized overview of the development and benchmarking of a Photonic Integrated Circuit-based Entangled Photon Pair Source (PIC-EPPS) designed for space-based quantum communication, as part of the LaiQa project. The project aims to advance critical quantum internet components, focusing on a compact, robust, and high-performance entangled photon source suitable for satellite deployment.

The PIC-EPPS is fabricated on a silicon-on-insulator (SOI) platform, leveraging double-bus microring resonators to enhance spontaneous four-wave mixing (SFWM). This architecture enables the generation of spectrally multiplexed, telecom-compatible photon pairs, with key specifications including MHz-level pair rates, high fidelity (≥95%), precise resonance alignment to the ITU DWDM grid (≈100 GHz spacing), a footprint below 1 mm², and low power consumption compatible with satellite payloads.

Development progressed through iterative cycles of simulation, fabrication, packaging, and characterization. Advanced electromagnetic and quantum mechanical simulations guided the design, ensuring compatibility with commercial telecom equipment and quantum memory integration. Fabrication utilized electron beam lithography and precision etching, with rigorous quality control and process improvements such as the introduction of a silicon dioxide top cladding.

Experimental results demonstrate robust performance: resonance alignment with the C-band DWDM grid, quality factors around 20,000, spectral stability with RMS deviation of ~4 GHz, fidelity values up to 99%, and photon pair rates in the kHz range per channel. The device operates reliably at optical pump powers between 35 and 50 mW, with ongoing efforts to further reduce coupling losses and improve spectral stability.

Key lessons include the importance of iterative design, close integration between simulation and fabrication, and comprehensive testing. Challenges such as coupling loss, resonance bandwidth, and packaging-induced spectral shifts are being addressed through targeted process improvements.

The PIC-EPPS platform meets or exceeds most project requirements, with ongoing work focused on integration with quantum memory modules as a critical step toward realizing space-based quantum repeater nodes for the quantum internet.

Keywords: Quantum Internet, Quantum Network, Quantum Repeater, Photonic Integrated Circuit, Entangled Photon Pair Source, Four Wave Mixing.

1 INTRODUCTION

The LaiQa project aims to advance the development of critical quantum internet components, with a particular focus on a photonic integrated circuit-based entangled photon pair source (PIC-EPPS) [1], suitable for space deployment. For an entangled photon pair source to function effectively in a satellite environment, several key requirements must be met. The source should be compact, lightweight, and capable of operating in the harsh conditions of space, including temperature variations and radiation exposure. Furthermore, it should exhibit high photon-pair generation rates to facilitate efficient quantum communication. In this context, a PIC-based EPPS emerges as a suitable solution for space applications. The integration of essential components on a single chip enhances reliability, reduces size and weight, and allows for precise control over the quantum properties of generated photons, making PIC-based EPPS well-suited for the demands of satellite-based quantum communication.

LaiQa's PIC-EPPS, is designed on a silicon-on-insulator (SOI) platform and leverages double-bus microring resonators to enhance spontaneous four-wave mixing (SFWM), enabling the generation of spectrally multiplexed entangled photon pairs. The main objectives are to achieve MHz-level pair rates with a compact footprint (<1 mm^2), and power consumption compatible with satellite payloads. The system is expected to operate with continuous wave (CW) optical pump power below +20 dBm, generating photon pairs at MHz rates with a fidelity above 95%. The photons generated by the source are in dual independent spectral windows in the C-band with precise resonance alignment to the International Telecommunication Union (ITU) frequency channels (≈100 GHz spacing), at a high spectral stability and a ring resonator quality factor of at least 10,000. The chip features thermo-electric control (TEC) with efficient power consumption (under 100 mW) compatible with satellite payloads. Multiple ring resonators are included on a single chip for redundancy, as shown in Figure 1.

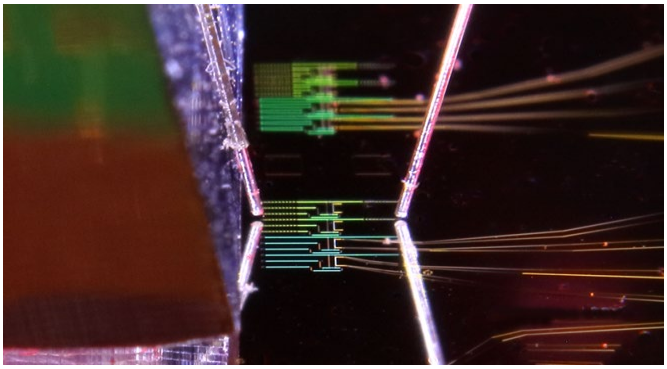

Figure 1. A set of four SOI ring resonators connected to fiber through free space grating couplers.

Over the past two years, the project has iteratively advanced through design, simulation, fabrication, packaging, and characterization, culminating in a robust, space-ready PIC-EPPS platform. This novel PIC-based EPPS will be integrated with a quantum memory block for a lab demonstration, forming a key component of a quantum repeater link in the envisioned entanglement-based quantum internet. The purpose of this deliverable is to provide a comprehensive overview of the development process and results achieved for the PIC-EPPS within the LaiQa project over the past two years. While previous reports have described individual milestones and detailed results [2], this document consolidates and summarizes that information to present a complete picture of the design, fabrication, and characterization efforts. Some key findings from earlier deliverables are repeated so that this report serves as a single reference point for the entire development cycle, ensuring clarity and continuity for future work.

2 DESIGN LAYOUT OF LAIQA'S PIC EPPS

2.1. Architecture & Operating Principle

The core of the LaiQa PIC-EPPS is a silicon-on-insulator (SOI) photonic integrated circuit, engineered for robust entangled photon pair generation via spontaneous four-wave mixing (SFWM). The architecture is built around double-bus microring resonators, which serve as the nonlinear medium for SFWM. These resonators are coupled to input and output waveguides using carefully designed grating couplers, enabling efficient fiber-to-chip optical interfacing. A schematic representation is shown in Figure 2.

The double-bus configuration allows for both through and drop port measurements, facilitating flexible characterization and multiplexed operation. The resonator geometry is optimized for a free spectral range (FSR) of approximately 100 GHz, aligning the generated signal and idler photons with adjacent ITU DWDM channels. This spectral alignment is crucial for compatibility with commercial telecom equipment and for future integration with quantum memory modules. Other critical design parameters include the waveguide width, ring path length, and the gap and length of the evanescent coupling region, all optimized to achieve critical coupling, low propagation loss, and high quality factor (Q) .

Thermal tuning is achieved via gold heater elements deposited adjacent to the microring resonators. These heaters, controlled by an microcontroller-based feedback loop, enable precise adjustment of the resonance wavelengths, compensating for environmental fluctuations and ensuring stable operation within the DWDM grid. The system is designed to operate with continuous-wave (CW) optical pump powers below 20 dBm, with the goal of achieving MHz-level photon pair emission rates and fidelity above 95%.

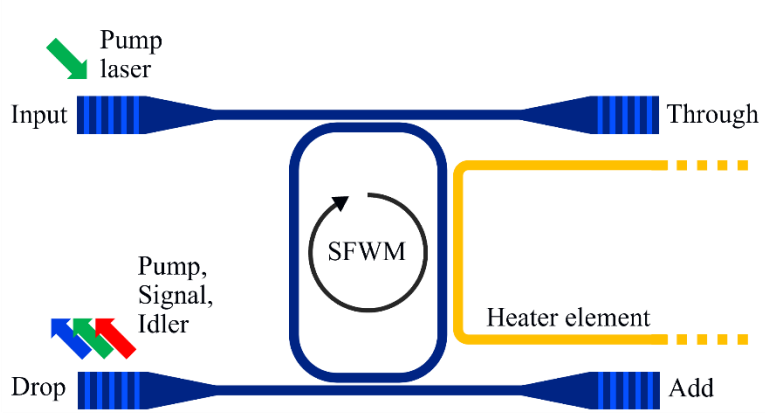

Figure 2. Schematic overview of elements in the PIC EPPS.

The overall footprint of the PIC-EPPS is kept below 1 mm², making it suitable for space-based applications where size, weight, and power consumption are critical constraints. The integration of the photon pair production in a single chip enhances reliability and simplifies packaging, paving the way for deployment in satellite payloads and quantum repeater nodes.

2.2. Simulation Strategy

The design and optimization of the PIC-EPPS relied on a comprehensive simulation workflow that integrated both classical electromagnetic modeling and quantum mechanical analysis. We used software tools such as Lumerical MODE and FDTD [5] to extract the effective refractive index and group index of the silicon waveguides, which are fundamental parameters for determining the free spectral range (FSR) and resonance conditions of the microring resonators. These simulations were essential for ensuring that the FSR would precisely match the 100 GHz ITU grid, a critical requirement for compatibility with commercial DWDM systems. The spectral profile of the resonator is also important for ensuring bandwidth matching to achieve future integration with quantum memory modules. Additionally from these simulations, the dispersion characteristics of the waveguide are obtained. This information is needed when designing the waveguide for phase matching of the SFWM process. The width of the waveguide is tuned so that optimal phase matching is achieved for the wavelengths involved, at the expected optical power during operation. An example of the type of visualization that can be obtained for the mode profile of light traveling through the simulated waveguide geometry is seen in Figure 3.

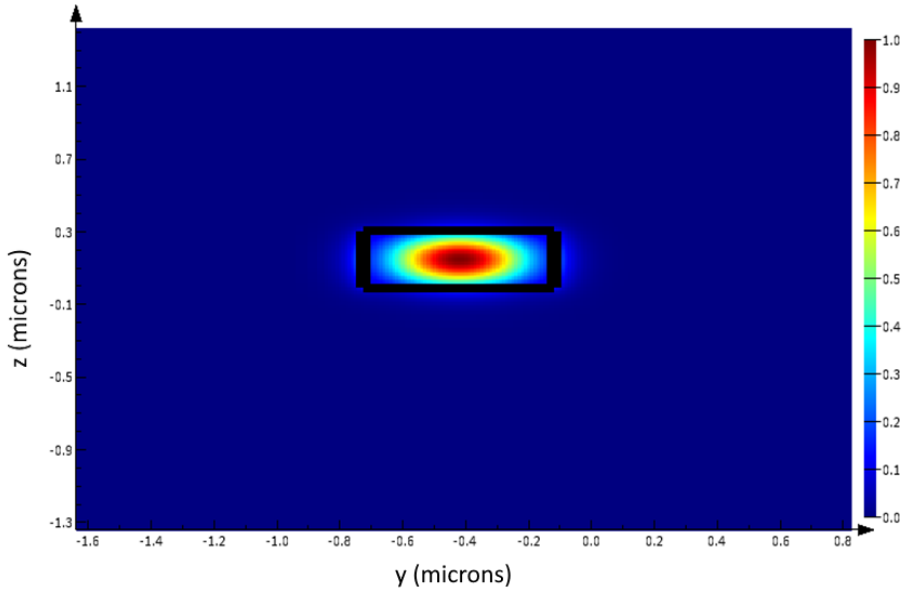

Figure 3. Mode profile for the fundamental transverse electric (TE) mode of the designed silicon waveguide. The color scale indicates relative intensity of transmitted light from 0 to 100%.

To optimize the grating couplers, we performed a series of finite-difference time-domain (FDTD) simulations, systematically varying fundamental parameters such as grating pitch (period of repetition in the grating structure), duty cycle (relative width of the high and low features in the grating), and apodization profile (variation in the pitch and duty cycle over the total length of the grating). The total number of features varied as different grating coupler types were considered, including straight and focused couplers, shown in Figure 4. The goal was to maximize coupling efficiency in the C-band, while also ensuring robust fabrication tolerances. The calculated scattering parameters for each grating design were incorporated into a circuit-level model, allowing us to predict the wavelength-dependent coupling efficiency and to identify the optimal geometry for the design in question.

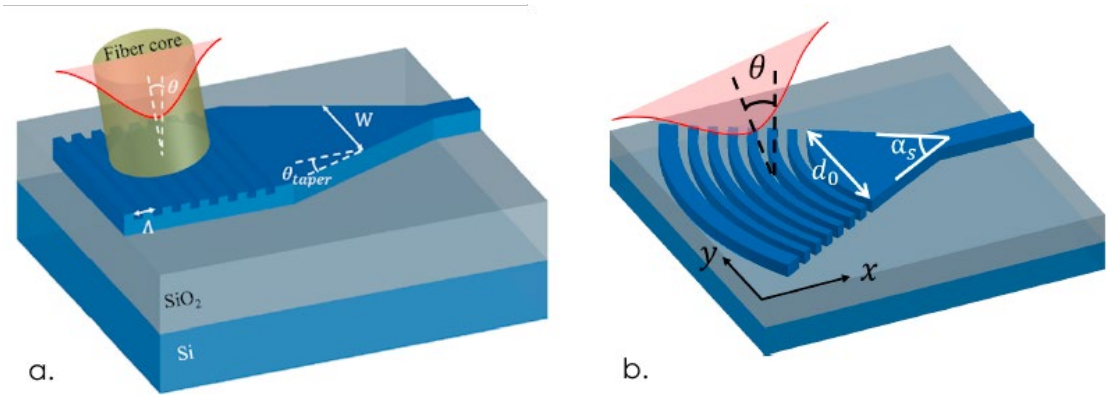

Figure 4. Different designs for the grating couplers that can diffract light from fiber core to on-chip waveguide for efficient coupling in the C-band. Figure a shows a straight coupler with performance depending on parameters like coupling angle θ, taper angle θ_{taper}, taper width W, and grating pitch Delta Δ. Figure b shows a focused apodized grating coupler with additional starting diameter d_0 and focusing angle a_s .

The evanescent coupling region between the bus waveguide and the microring resonator was modeled using eigenmode expansion techniques. By adjusting the gap and coupling length, we were able to tune the coupling coefficient to achieve critical coupling, which is necessary for maximizing the energy storage in the ring and, consequently, the photon pair generation rate. These simulations also provided insight into the sensitivity of the device performance to fabrication variations, informing our process control strategies.

Beyond classical modeling, we developed analytical models for the spontaneous four-wave mixing (SFWM) process, incorporating the dispersion and coupling parameters obtained from the electromagnetic simulations. These quantum mechanical models allowed us to predict the pair generation rate, spectral bandwidth, and fidelity of the entangled photon pairs as a function of pump power and device geometry. We also included the effects of self-phase modulation and temperature-dependent refractive index changes, the latter being particularly important for understanding the tuning range and stability provided by the integrated heaters. A full overview of all the modeled parameters is shown in Table 1.

Table 1. Overview of all parameters relevant to the simulation and design choices of the pic-based entangled photon pair source.

Description	Parameter	Component
Waveguide geometry	Width, Height	Waveguide
Waveguide optical properties	Effective index (n_{eff}), Group index (n_g), Dispersion	Waveguide
Mode profile visualization	TE mode intensity distribution	Waveguide
Resonator spectral characteristics	Resonator length for Free Spectral Range (FSR), Quality factor (Q), Resonance wavelength	Ring resonator
Coupling region geometry	Gap width, Coupling length	Evanescent coupling gap
Grating coupler geometry	Grating pitch (Δ), Duty cycle, Taper angle (θ_{taper}), Coupling angle (θ), Apodization profile, coupler width	Grating coupler
Grating coupler performance	Coupling efficiency, Scattering parameters (S-matrix)	Grating coupler

Heater leads design	Heater material, width, thickness	On-chip heater
Thermal tuning behavior	Resonance shift vs. temperature/current	Ring resonator
Nonlinear process characteristics	Phase matching conditions, SFWM pair generation rate vs power	Waveguide + Ring resonator

All component-level simulations were integrated using Lumerical INTERCONNECT [8], which enabled us to model the complete optical circuit and to perform rapid parameter sweeps. This approach allowed us to optimize the overall device performance, balancing competing requirements such as coupling efficiency, resonance alignment, and fabrication robustness. The simulation results were validated against experimental measurements at each stage, providing confidence in the predictive power of our models and guiding the iterative refinement of the PIC-EPPS design. This process is described further in section 3.1.

2.3. Fabrication Baseline

The fabrication of the PIC-EPPS was carried out on a silicon-on-insulator (SOI) platform, chosen for its compatibility with advanced nanofabrication techniques. Patterns for waveguides, microring resonators, grating couplers, and heater lines were defined using electron beam lithography (EBL), with alignment markers ensuring precise overlay during multi-step processing. After lithography, the structures were etched into the silicon device layer using inductively coupled plasma reactive ion etching (ICP-RIE), a process optimized for vertical sidewalls and minimal roughness to maintain low optical loss and high resonator quality factors. Grating couplers were etched to a depth of 100 nm, while waveguides and rings were etched through the full 300 nm device layer. The etching process is shown step-by-step in Figure 5. Scanning electron microscopy (SEM) was used throughout to verify feature sizes and identify any deviations from the intended geometry.

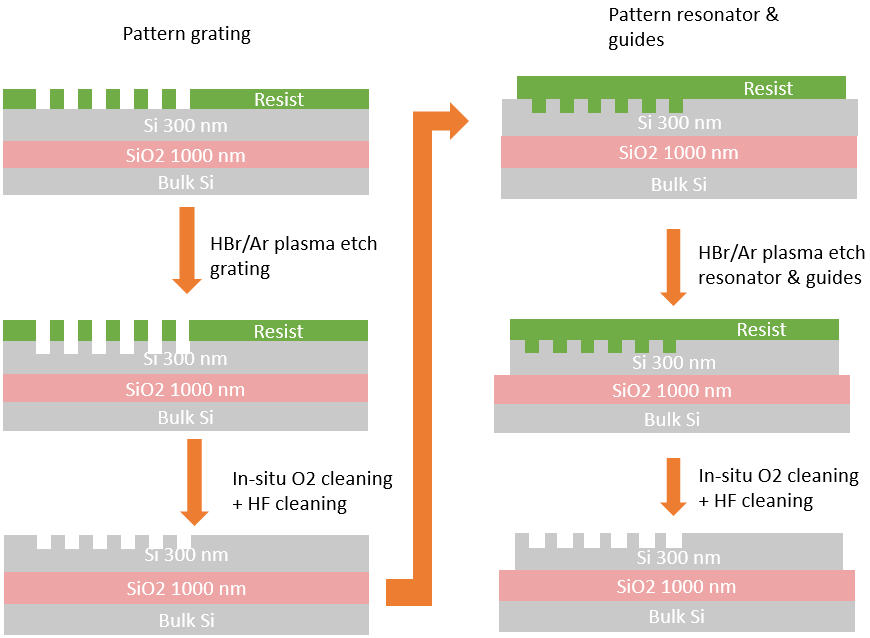

Figure 5. Schematic of the fabrication process for etching in a SOI platform. The patterning is written in a resist layer using e-beam lithography, with a HBr/Ar plasma etch removing silicon material. An oxygen and HF cleaning step removes the remaining resist. Two separate etching steps are taken to pattern the gratings and waveguides on the PIC.

Thermal tuning elements were integrated by depositing a thin titanium adhesion layer followed by 300 nm of gold using physical vapor deposition (PVD). Finally, a 1 µm silicon dioxide (SiO_2) top cladding layer is deposited over the chip by chemical vapor deposition (CVD), which improves efficiency of the waveguides and coupling to the chip.

After fabrication, chips were wire-bonded to custom printed circuit boards (PCBs) to provide robust electrical access for automated heater control. This layer reduced waveguide loss, narrowed resonance bandwidth, and protected the photonic structures, but also required re-optimization of the grating coupler design due to a measurable shift in the coupling peak wavelength.

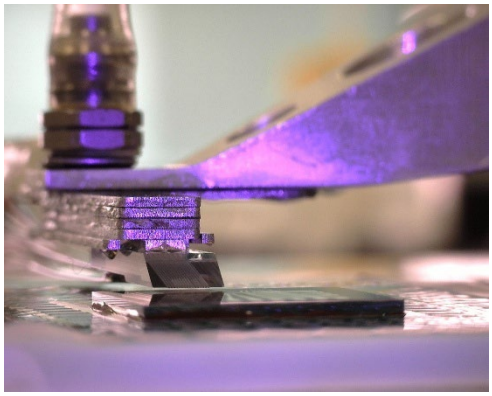

Figure 6. Fiber array packaging of chip 24 at the CITC facility in Nijmegen

For optical interfacing, a 16-fiber array was attached to the chip using precision alignment and UV-curable adhesive, positioned at a slight angle to match the grating coupler design. The packaging process is shown in Figure 6. Careful application was required as the adhesive's refractive index could induce a shift in the coupling peak, especially if it encroached on the grating area. Quality control was maintained through SEM imaging, optical microscopy, and electrical testing of heater lines, with feature sizes typically controlled within 5 nm of the design target. This rigorous approach has enabled the realization of high-performance, reproducible PIC-EPPS devices suitable for both laboratory research and future space-based quantum communication systems.

3 DEVELOPMENT SUMMARY OF LAIQA'S PIC EPPS

3.1. Iteration History & Key Steps

The development of LaiQa's PIC-EPPS followed an iterative cycle of theory and simulation, design and fabrication, and experimental characterization. Each stage informed the next: simulations guided the initial design choices, fabrication translated these designs into physical devices, and characterization provided critical feedback to validate the models and refine parameters. This feedback loop allowed us to progressively optimize the source, ensuring that theoretical predictions aligned with practical performance and that improvements were systematically implemented across successive chip iterations. This process is illustrated in Figure 7.

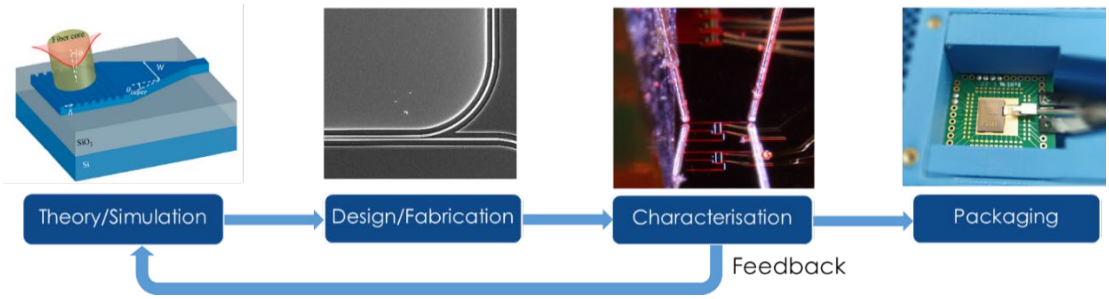

Figure 6. Iteration process for the design of the PIC EPPS.

In the process of iterating over multiple design parameters, thirty entangled photon pair sources were fabricated. The main focus of iteration per fabricated chip is shown in Table 2. Some measurements were repeated over multiple chips, not every single measured parameter has been included for brevity.

Table 2. Overview of main targeted parameter per fabricated chip, numbered in order of fabrication timeline.

Chip iteration nr.	Parameters	Description
1-6	E-beam patterning settings, etching depth, processing steps.	Fabrication recipe in SOI
7	Grating duty cycle	Grating optimization for 1550nm coupling
8-9	Ring resonator length	Ring length variation for FSR of 100GHz
10-11	Grating duty cycle, grating pitch, focusing angle	Focused and Straight grating parameter test
12	Gold heater lead width, thickness, wire bonding	Thermal control with on-chip heaters
13	Fiber array application	Packaging test with 16-channel fiber array
14-15	Evanescent gap length	Optimize coupling into ring resonator
16-19	Grating coupler apodization profile, focusing angle	Experiment with further grating coupler adjustments
20	Grating coupler period, pitch	Further grating coupler optimization for least loss at 1550nm
21	Top oxide cladding	Change to fabrication recipe with addition of SiO_2 layer deposition on top
22-23	Evanescent gap width, grating coupler period, pitch	Adjust parameters for top oxide addition
24	Fiber array application	Optimize coupling loss after packaging with 16-channel fiber array
24-30	Design parameters kept constant	Repeatability of fabrication, further characterization for validation of analytical simulations

Thirty chips were fabricated over the course of the project, each incorporating incremental improvements based on previous results. The initial phase of chip development focused on establishing a robust simulation and fabrication workflow and validating the theoretical models against experimental data. For example, the group index was extracted from both simulation and measurement, with values converging around 4.18, confirming the accuracy of the modeling approach. Multiple ring resonator designs were simulated, varying the path length to tune the FSR. Grating coupler designs were iteratively optimized, exploring variations in pitch, duty cycle, and apodization. Both straight and focusing grating couplers were fabricated and tested, with apodized profiles included, in order to finally converge on a single design.

In addition to optical design, the fabrication recipe was also validated with additional measurements. SEM inspection revealed that etch precision was typically within 5 nm of the target, though occasional edge roughness and gap deviations were observed. Adjustments to the electron beam dose and etch recipes improved feature consistency and reduced sidewall roughness. Physical vapor deposition of heater lines was refined to ensure reliable adhesion and electrical contact. Wire bonding the on-chip heaters to PCBs enabled automated thermal control. A key process change was the introduction of a 1 µm silicon dioxide (SiO_2) top cladding, deposited by chemical vapor deposition. This layer reduced waveguide loss, narrowed resonance bandwidth, and protected the photonic structures, but also required re-optimization of the grating coupler design due to a measurable shift in the coupling peak wavelength.

The main measurement types used in the process of characterizing the chips and refining the design parameters are described in the next sections. This includes resonance and correlation measurements as well as temperature control sweeps and comparisons before and after packaging the chips. The results of key individual measurements have also been described in more detail in deliverables D4.1 and prior presentations within Laiqa.

3.2. Classical and Quantum Measurements

Classical Characterization:

The characterization process began with classical measurements to determine the fundamental optical properties of the microring resonators. Through-port and drop-port wavelength sweeps were performed using a tunable C-band laser source. The laser was aligned to the chip via grating couplers, with a polarization controller ensuring optimal coupling into the TE mode of the waveguide. The transmitted and dropped signals were monitored using a calibrated Thorlabs power meter, allowing precise measurement of wavelength-dependent transmission. A simplified image of the setup is shown in Figure 8.

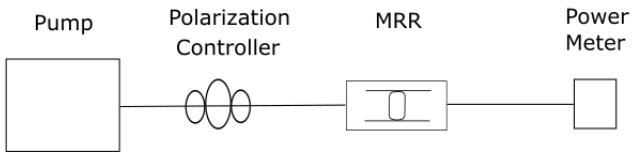

Figure 7. Classical measurement setup: a tunable C-band laser (pump) is connected to the on-chip microring resonator (MRR) after tuning with the polarization controller for optimal coupling. The wavelentgh dependant resonance and loss is measured with a thorlabs power meter.

From these sweeps, of which an example is shown in Figure 9, several key parameters were extracted. The spacing between successive resonance dips provided the Free Spectral Range (FSR), which consistently matched the 100 GHz target required for DWDM compatibility. The Full Width at Half Maximum (FWHM) of each resonance was calculated from the transmission spectrum, enabling

determination of the Quality Factor (Q) of the resonators, which reached values up to 38,000 in pre-packaging chips. Additionally, the resonance alignment with ITU channels was verified by comparing the measured wavelengths to the DWDM grid, confirming that the resonances fell within the passbands of commercial multiplexers. These measurements also allowed estimation of insertion loss and coupling efficiency for different grating designs.

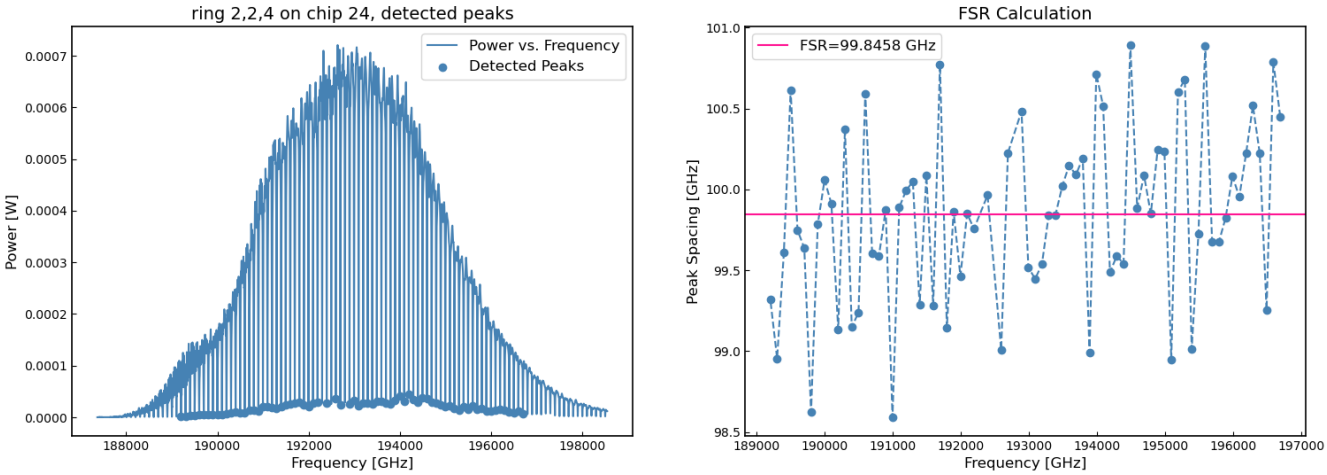

Figure 8. Classical wavelength sweep between 1510 and 1600nm with an input power of 35mW, shown on the left. From this classical data, the spectral with of the resonances in the MRR can be calculated, along with their spacing (FSR), shown on the right.

Quantum Characterization:

To evaluate the source performance for entangled photon pair generation, quantum measurements were carried out using the spontaneous four-wave mixing (SFWM) process. The pump laser was filtered through channel 40 (centered at 1545.32 nm) using a dense wavelength division multiplexer (DWDM) before entering the ring resonator. Photon pairs generated inside the resonator were separated by the same DWDM into symmetric channels (e.g., 37 and 43) and directed to single-photon detectors, either silicon based single photon avalanche diodes (SPAD) of 10 percent detection efficiency or superconducting nanowire single photon detectors (SNSPD) with 85 percent efficiency. Figure 10 shows the experimental setup expanded to extract correlated data.

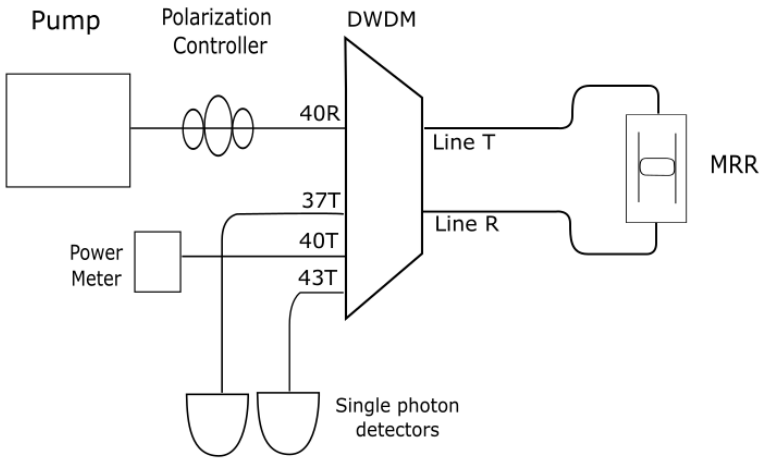

Figure 10. Correlation measurement setup: the pump laser is filtered through channel 40 (centered at 1545.32nm) using a dense wavelength division multiplexer (DWDM) before entering the ring resonator. The generated photon pairs pass through the same DWDM to be separated by wavelength channels 37 and 43.

This setup enabled extraction of several critical parameters. A correlation peak in arrival time was formed from coincidence measurements on the photon detectors, which were connected to a time tagger. The fidelity of the entangled state was derived from the visibility of the correlation peak, ranging from 94% to 99% depending on the detector type (SPAD vs SNSPD) used for the measurement, as the higher relative detector dark count in SPADs affects the background noise. The Coincidence-to-Accidental Ratio (CAR), related to the second-order correlation function (g^2), was also determined from these correlation peaks, with the target to be remaining above 2 even at low pump powers, indicating robust entanglement. Furthermore, the pair generation rate was estimated from the peak counts and measurement time, yielding detected rates in the kHz range at pump powers of 35–50 mW. The true generation rate can then be calculated to be approximately two orders of magnitude higher after correcting for detector efficiency and optical losses. A correlation peak measurement is shown in Figure 11 with fitted gaussian for data extraction.

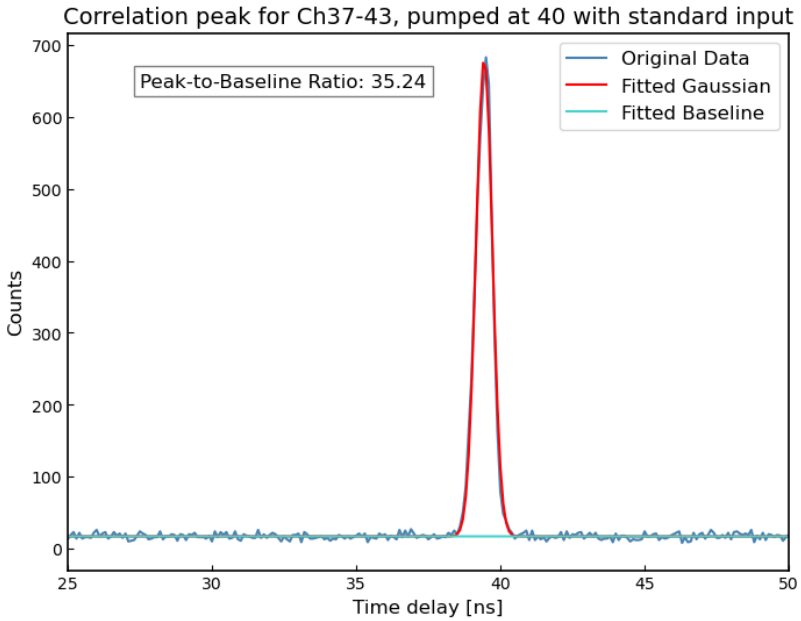

Figure 9. Example of a correlation measurement taken on chip 24. From the gaussian fit to the correlation peak, the spectral width and total pair rate can be determined. The peak height can be compared to the background noise for an estimation of the signal to noise ratio or g2. This result was obtained after pumping in wavelength channel 40 (1545.32nm) and measuring detection events in channel 37 and 43, with a silicon single photon avalanche photodiode of 10 percent efficiency.

3.3. Thermal Control and Stabilization

Thermal tuning was demonstrated using gold heater lines and an Arduino-type microcontroller based feedback loop. Resonance sweeps such as the sweep in Figure 9 were repeated at various voltage settings, showing that the system could shift the resonance wavelength by more than one ITU channel. This enabled precise alignment with DWDM passbands. An example of a repeated resonance sweep at different voltages is seen in Figure 12.

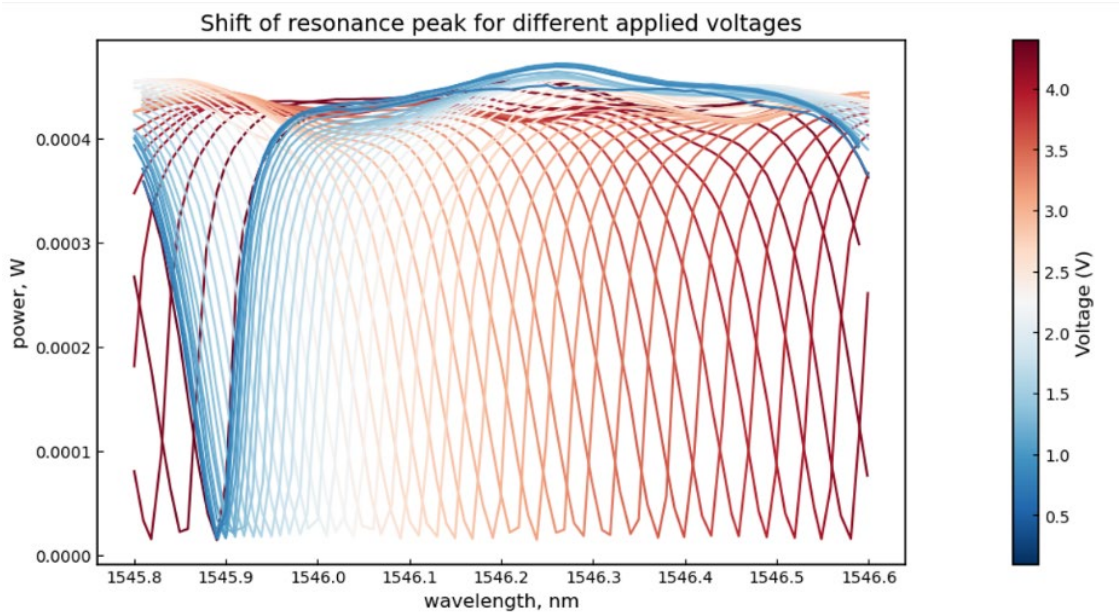

Figure 12. Wavelength sweep of the ring resonator at different heater lead voltages, showing a shift in resonant wavelength due to current increasing the temperature locally and shifting the index of refraction of the ring resonator.

The thermal stabilization results are described in more detail in deliverable D4.1 [2]. Closed-loop operation minimized drift and stabilized both resonance and coincidence counts, ensuring consistent performance over extended measurement periods.

3.4. Packaging and Integration

The attachment of a 16-fiber array to the chip using UV cured adhesive improved coupling efficiency and stability. However, the adhesive used for bonding can introduce a wavelength shift due to its refractive index. Measurements before and after packaging in some cases showed a 30 nm shift in the maximum coupling wavelength as shown in deliverable D4.1, highlighting the need for careful control of adhesive placement and selection. One change to the chip design was to increase the grating coupler-to-chip edge distance to reduce the chance of array adhesive landing on the couplers.

3.5. Current Performance Snapshot

From characterization results as obtained using some of the measurements described previously, a summary of the current state of some key parameters as defined by the Laiqa requirements document has been included here:

FSR Alignment: Measurements confirm an average FSR of 99.83 GHz, fully compliant with the C-band DWDM grid and commercial multiplexing equipment.

Quality Factor: Packaged devices consistently achieve Q values around 20,000, with FWHM of resonance peaks near 10 GHz at 1545 nm.

Spectral Stability: The RMS deviation of resonance peaks is approximately 4 GHz, exceeding the interim requirement of ≤10 GHz but above the long-term goal of <100 MHz for optimal quantum memory integration.

Fidelity: Quantum measurements yield fidelity values between 95% and 99%, with the highest values observed using SNSPD detectors and optimized filtering.

Pair Generation Rate: Detected pair rates are in the kHz range per channel, with true generation rates estimated to be 100× higher after accounting for detector and optical losses. These channels could be multiplexed to even further increase the pair rate by an order of magnitude.

Optical Pump Power: Devices operate reliably at CW pump powers between 35 and 50 mW (≤17–20 dBm), well within the target range for space-based applications.

Coupling Loss: Post-packaging coupling losses are measured at 6.1–6.5 dB per coupler, with ongoing efforts to reduce this to <2.5 dB through edge coupling and improved grating designs.

Footprint and Power Consumption: The device footprint is approximately 0.5 mm² per ring block, and total power consumption (optical + thermal) ranges from 35 to 150 mW, depending on stabilization duty cycle.

3.6. Lessons and Technical Challenges

Throughout the development of the PIC-EPPS, several important lessons have emerged that continue to shape our design and process choices. The introduction of a silicon dioxide top cladding was a clear improvement for reducing waveguide loss and narrowing resonance bandwidth, but it also highlighted the sensitivity of the device to fabrication changes. The resulting shift in grating coupler peak wavelength required additional design iterations, emphasizing the need for thorough characterization after each major modification. Grating coupler optimization in general proved to be a delicate balance between simulation and fabrication realities. While apodised and focusing grating designs offered promising improvements in coupling efficiency, their performance was highly dependent on precise lithography and etching. Small deviations in feature size or process parameters could lead to unexpected spectral shifts or reduced efficiency, underscoring the importance of robust process recipes.

Packaging and fiber array attachment introduced further complexity. The adhesive used during bonding was found to influence the coupling spectrum, particularly if it encroached on the grating region. This effect prompted us to reconsider the layout, increasing the distance between the grating couplers and the chip edge and exploring alternative adhesives to minimize refractive index perturbations.

Thermal control and resonance stabilization have also been essential for reliable operation. The integration of gold heater lines and feedback electronics enabled precise tuning and long-term stability, but also required calibration and monitoring to maintain performance over time. We have found that thermal stabilization becomes more difficult at higher input powers above 75mW due to optical self-heating effects, which has been documented in silicon ring resonators before [9]. To meet the performance requirements in LaiQa, we do not need to operate the source at input powers above 50mW, so this stabilization challenge did not interfere with our measurements.

Overall, these experiences have reinforced the importance of iterative design, close integration between simulation and fabrication, and comprehensive testing. Each challenge has led to practical improvements in the PIC-EPPS platform, and the lessons learned will guide future efforts as we move toward larger-scale integration and deployment in quantum communication systems.

4 COMPLIANCE TO REQUIREMENTS

The overview of compliance to the requirements set by LaiQa has been copied from the previous deliverable [2]. They are included here once more for completeness. In this case, the work has been extended by addressing the remaining actions to target any requirements that were not fully met in section 4.1.

The requirements on the source for this work package were defined based on the proposal document and are also outlined in deliverable D2.2. Table 3 summarises the functional and overall requirements for the PIC entangled photon pair source.

Table 3. PIC EPPS overall requirements.

Req ID	Requirement description	Rationale
RQ-PIC-001	The PIC-EPPS shall be suitable for energy-time and polarization-encoded entanglement generation.	from proposal
RQ-PIC-002	The PIC-EPPS shall produce entanglement between at least 2 DWDM wavelength channel pairs	from proposal
RQ-PIC-003	The PIC-EPPS shall be designed to operate in conjunction with the Quantum Memory.	from proposal
RQ-PIC-004	The PIC-EPPS shall operate in the optical C-band	from proposal
RQ-PIC-005	The PIC-EPPS shall be temperature tuned with an automatic feedback system	From proposal

In addition, the following requirements in the proposal placed more specific targets on the performance of the PIC EPPS source, as shown in table 4:

Table 4. PIC EPPS performance requirements.

Req ID	Requirement description	Rationale
RQ-PIC-006	The PIC-EPPS shall emit >1k pairs/sec/channel with a g2(0) above 40 (F>95%)	from proposal
RQ-PIC-007	The PIC-EPPS shall have a fidelity of at least 95%.	from proposal
RQ-PIC-008	The spectral feature of the PIC-EPPS photons shall not exceed 10GHz	from proposal
RQ-PIC-009	The PIC-EPPS shall have at least 3 pairs of spectral channels available	from proposal

Table 5 shows the current benchmark evaluation for the PIC EPPS development, achieved between the end of 2024 and mid-2025 with the established design of chips 24-30, together with the requirement. The results in this table are taken at 50 mW (17 dBm) of pump power and correlation results were measured with SNSPDs detectors.

Table 5. Key performance indicators related to requirements set within LaiQa.

KPI	Targeted Value	Current Value	Related requirements
Thermal stabilization	Automatic tuning operational in standard conditions	Automatic stabilization possible between 0-50 C external temperature	RQ-PIC-005
Available spectral channels with correlated pairs	>3 channel pairs	7 channel pairs	RQ-PIC-001, RQ-PIC-002 and RQ-PIC-009
Channel resonance Matching to C-band	Centered in C band with ≈100GHz spacing	Centered in C band with 99.83GHz spacing	RQ-PIC-003 and RQ-PIC-004
Low Resonance RMS for High Spectral Stability	< 10 GHz	≈4 GHz	RQ-PIC-003 and RQ-PIC-008
Photon Pair Rates	kHz-scale with g2 >40	kHz-scale with g2 > 100	RQ-PIC-006
Fidelity	>95%	≈99%	RQ-PIC-007

There are further targets that were not translated into a requirement but indirectly mentioned in the proposal and kept in mind during the design phase for optimization of the PIC EPPS. For example, to comply with possible use in satellite-based applications it is important to limit the power consumption and footprint of the chip. These are shown in table 6.

Table 6. Additional performance indicators used as development guidance for the source.

KPI	Targeted Value	Current Value	Rationale
Optical Power for CW Optical Pump	<20 dBm	17 dBm	Achieving the desired performance at low input powers makes the PIC EPPS more suitable for satellite based applications.
Coupling Loss between chip and fiber.	<2.5 dB loss	6.1 dB loss	Reduction in coupling loss between chip and fiber will further improve fidelity and detected pair rates.
Waveguide Loss	<3 dB/cm	<2 dB/cm	Limit loss on-chip, thereby also reducing the optical power needed.
Footprint	<1 mm^2	≈0.5 mm^2	More suitable for satellite based applications.
Low Resonance RMS for High Spectral Stability	<100 MHz	≈4 GHz	Related to RQ-PIC-003, for more optimal integration with a quantum memory.
Resonance Quality Factor	>10K	≈20K	The quality factor of the ring resonator is also related to resonator waveguide loss and fabrication quality.
Power Consumption	<100 mW	35-155 mW	Limits required heat production. This includes contribution from 35 mW of optical power and between 0 and 120 mW of thermal control.

4.1. Actions to target noncompliance

To address the remaining gaps in performance, several targeted actions have been identified. First, reducing coupling loss to below 2.5 dB per coupler is a priority. This will involve transitioning from grating-based coupling to edge coupling or vertical evanescent couplers, which offer inherently lower insertion loss. In addition, maintaining a uniform top cladding layer that is optically compatible with the adhesive index will help minimize wavelength shifts introduced during packaging. These improvements will not only reduce overall loss but also enhance stability and repeatability in packaged devices.

Second, narrowing the resonance bandwidth toward <1 GHz (RMS <100 MHz) is essential for optimal integration with quantum memory systems. Achieving this will require fine-tuning the ring–bus gap to move toward under-coupling, which reduces linewidth while preserving acceptable pair generation rates. Further refinements in waveguide fabrication, such as improving sidewall smoothness and optimizing electron-beam lithography dose, will help lower propagation loss and improve Q-factor. Additionally, exploring slightly longer ring lengths with controlled dispersion will allow us to maintain the required FSR alignment while achieving narrower resonances. However, if we cannot reduce the resonance bandwidth further, integration with the quantum memory will still be possible, as described in the next section.

4.2. Outlook for integration with LAIQA's quantum memory

The PIC-EPPS platform has reached a level of maturity where its performance aligns closely with the project's objectives. With MHz-level pair generation rates, high fidelity, and robust thermal stabilization demonstrated, the next major milestone is integration with LaiQa's quantum memory module. This step is critical for validating the combined functionality of a quantum repeater node, where entangled photons generated by the PIC-EPPS can be stored and retrieved from the memory without loss of quantum coherence.

Integration will involve aligning the spectral properties of the source with the memory's absorption profile, ensuring compatibility in terms of bandwidth and channel spacing. The improvements outlined above, particularly narrowing the resonance linewidth, would directly support this goal. Alternatively, we can implement filtering to artificially match the bandwidth of the source to the memory. Once integrated, the combined system will enable proof-of-concept demonstrations of long-distance entanglement distribution, paving the way for space-based quantum internet applications. Future work will also focus on scaling up automated testing and packaging processes to ensure reproducibility and readiness for deployment in operational environments.

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