Quantum Large-Scale Integration in Silicon

QLSI

Report on deliverable D5.1.5

Open access online 8-qubit quantum computer prototype (TNO)

Other references: D5.9

(Revision 1.0)

Public deliverable

Date: 21/02/2025

Document Control Information

Settings	Value
Document Title:	D5.1.5 Open access online 8-qubit quantum computer prototype
Project Title:	QLSI
Document Author:	Jasper Winters (TNO), Richard Versluis (TNO)
Project Owner:	EU
Project Manager:	CEA
Doc. Version:	1
Sensitivity:	Public deliverable
Date:	21/02/2025
TNO Document number:	TNO 2025 R10451

Document Approver(s) and Reviewer(s):

NOTE: All Approvers are required. Records of each approver must be maintained. All Reviewers in the list are considered required unless explicitly listed as Optional.

Name	Role	Action	Date
Peter Verhoeff (TNO)	WP Leader	Approve	19/02/2025
Jérémy Veltin	Research Manager	Approve	ValidSigned by Jérémy Veltin on 2025-02-21 11:43:42

Document history:

The Document Author is authorized to make the following types of changes to the document without requiring that the document be re-approved:

- Editorial, formatting, and spelling
- Clarification

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Revision	Date	Created by	Short Description of Changes
0.1°	24/01/2025	Jasper Winters (TNO)	Creation
0.2°	12/02/2025	Jasper Winters (TNO)	Update all chapters
0.3°	13/02/2025	Richard Versluis (TNO)	Added pictures and dissemination information
1.0°	19/02/2025	Jasper Winters (TNO)	Formatting and details before review

TABLE OF CONTENTS

1. TASK OVERVIEW

1.1. Executive Summary

This deliverable reports on the completion of the open access online 8-qubit quantum computer, making use of the upgraded demonstrator setup (D5.5) and the chip presented in D5.8. This also completes M5.1.2. The 6-qubit chip design from WP3 (TUD) was the starting point for the demonstrator. The realized design of the demonstrator setup has been implemented in two of our setups, both showing the capability of controlling the 6-qubit chip. One of which is being used for this current deliverable.

The system was upgraded with the necessary hardware, software, calibration methods, web platform, publicly available API to access the quantum computer and website as per the requirements identified. After the integration process, the equipment and their functionality was validated, see D5.8 for details. Overall, the system was upgraded with the necessary hardware for the automated tuning, calibration and control of quantum chips.

1.2. Task Stakeholders

Deliverable Due Date	M30
WP 5	**Leader: TNO**
	Partners: TNO, TUD, CNR, IMEC, ATOS, QM
Task 5.1	**Leader: TNO**
	Partners: TNO, TUD
Other stakeholders	None

2. TASK DETAILS

2.1. Work carried-out

Using the 6-qubit chip design from WP3 (TUD) as starting point, manual and automatic calibration methods were developed and applied, resulting in the chip deployment report D5.8.

2.1.1. *Task goals*

- Implementing the chip from D5.8 into the online platform
- Creating the online platform and software interfaces
- Operating the chip
- Maintaining the quantum computer
- Dissemination

2.1.2. *The chip*

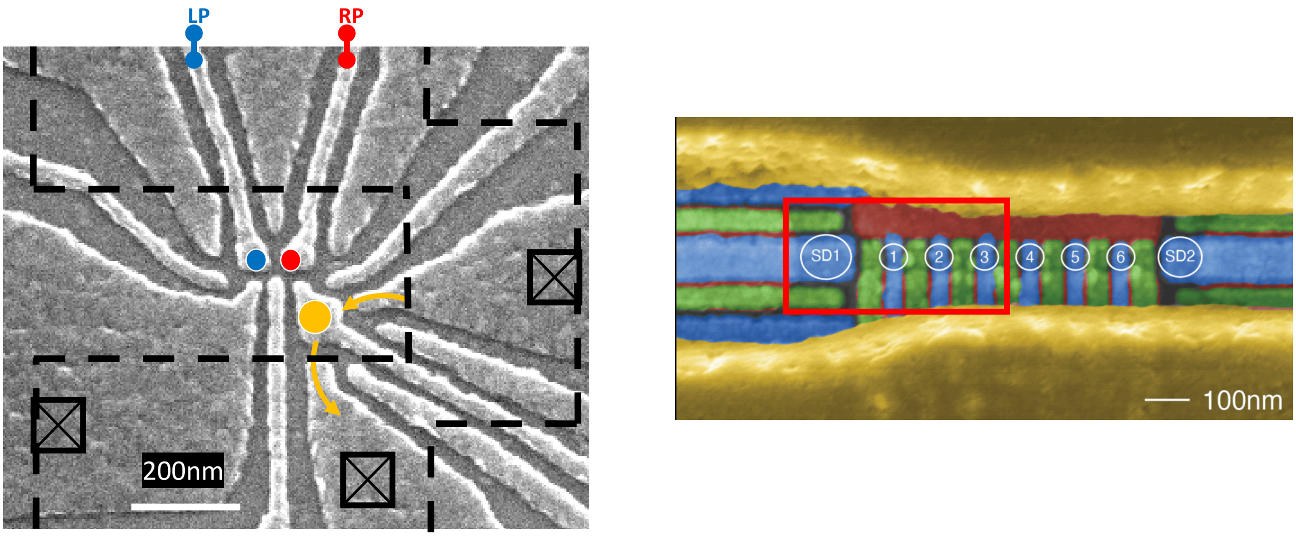


Figure 2-1 Two-dot quantum chip from 2020 and six-dot quantum chip from QLSI.

Figure 2-1 shows the quantum chip that was used in the first version of Quantum Inspire (left) and the version reported in in this report, named Spin-2+ (right). **Spin-2+ QPU** is based on multi-layer gate stack, defining a linear array of six quantum dots 1 to 6 on our in-house grown SiGe/^{28}Si/SiGe heterostructure (4-6). Spin-2+ utilizes the left three dots and Sensing Dot 1 (SD1) to define one ancilla qubit in dot 1 and two data qubits in dots 2 and 3. PSB readout through the ancilla qubit is used to readout the two data qubits. Static and dynamic potentials are defined by the screening gates (red), barrier gates (green) and plunger gates (blue). In the online demonstrator only qubits q0, q1 and q2 are used in Spin-2+ due to the insufficient frequency spacing between the other qubits, resulting in too much cross talk between q3, q4 and q5 to make them useful as computational qubits in an online system. For completeness, Figure 2-2 shows the measured resonance frequencies for the full system, visualizing the (too) limited frequency spacing between qubits q4, q5 and q6 (dots d3, d4 and d5).

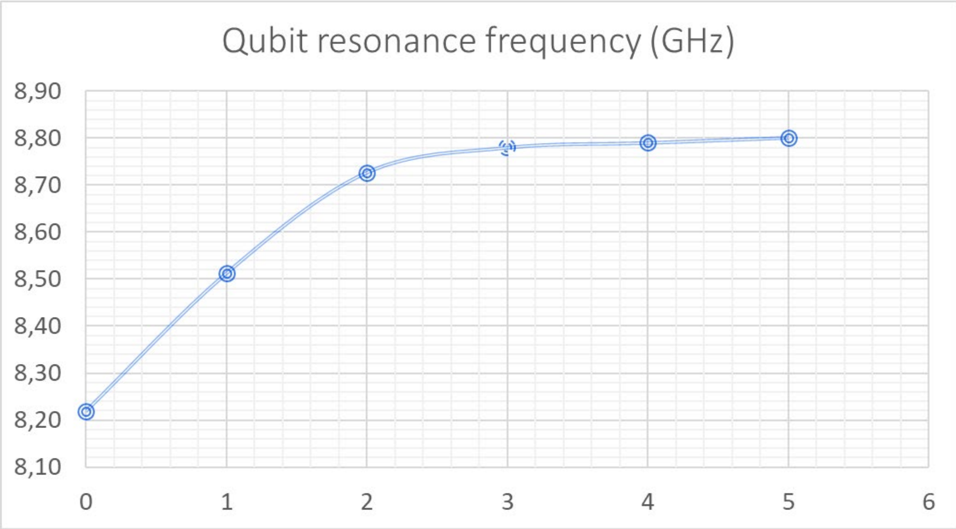


Figure 2-2 Qubit resonance frequencies at the applied external magnetic field of 80 mT. At this magnetic field, the resonance frequency of q3 was not determined. The value plotted is interpolated based on measured values at a different magnetic field.

Most electrodes have a DC component and an AC component. These are supplied by different sources (DC supply and AWG) and these signals are combined at the sample by means of bias-tee circuits. Also some additional DC sources are needed for chip conditioning of areas that don't need fast AWG signals.

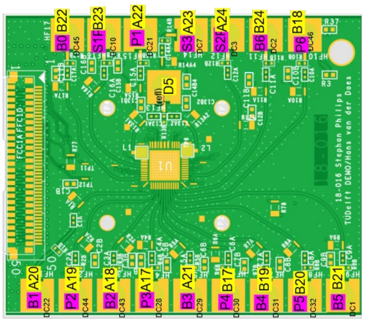


Figure 2-3 Sample PCB for 6 qubit chip.

2.1.3. *Software interface*

Together with TUD the software for controlling the room-temperature electronics was developed. This comprises of a.o. device drivers, device compilers, quantum compilers, calibration routines, software framework and data storages.

The hardware and software system can be accessed publicly from our web platform (Figure 2-4) and the API. The www.quantum-inspire.com website (Figure 2-4) contains more information about the project and contains a knowledge base about qubits, qubit operations, code examples and hardware backend specific information.

The website and compilers were jointly created with the EU flagship project OpenSuperQplus and with support of the Dutch National Growth Fund Quantum Technology.

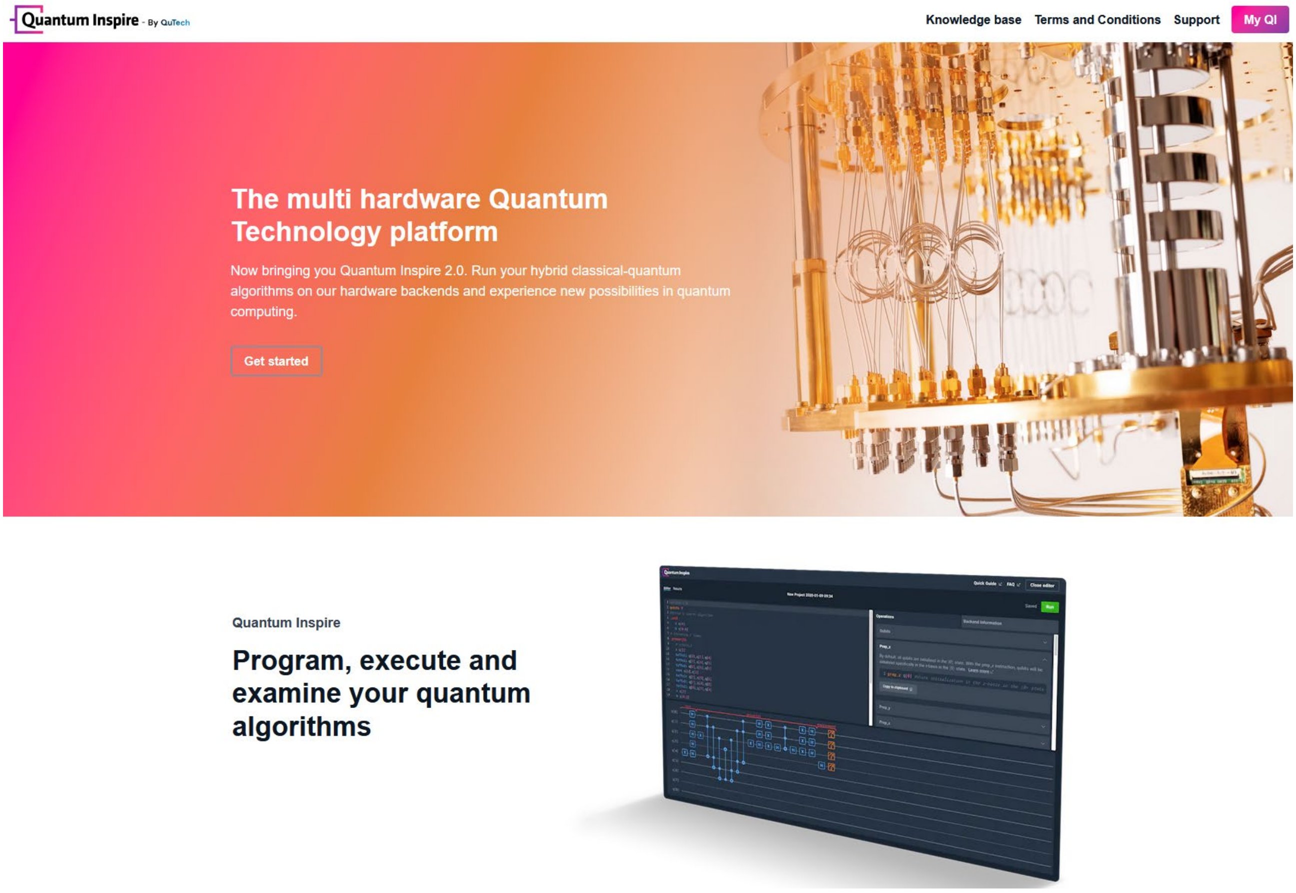


Figure 2-4 Screenshot of www.quantum-inspire.com .

2.1.4. *Operation*

The demonstrator and all the quantum computer backends are publicly available. We strive to keep the systems online for as long as possible, but scheduled (and unscheduled) maintenance actions are unavoidable. The reason for this is that we want to provide a good experience, and the quantum computer needs continuous maintenance to make sure it works properly. Large portions of the work are performed by automatic calibrations, but manual adjustments are also needed. The dilution refrigerator also needs regular maintenance. The latter two combined with limited availability of personnel, result in the need for a scheduled approach. Next to this, the control hardware and dilution fridges for the quantum computers being quite expensive to procure and operate will also be repurposed for follow-up projects, like QLSI-2 and OSQ+. This means that in the future some of the backends will need to be taken offline for a longer period (multiple months) to upgrade the chip and control hardware and software to enable the functionality and performance for those projects.

2.1.5. *Automatic calibration*

During operation of the quantum computer, minute changes in its surroundings cause that various calibration parameters need to be monitored and updated regularly. A systematic approach was chosen of checks and adjustments, to have as much time available to external users as possible, whilst safeguarding performance. An illustration of this approach, our calibration graph, is illustrated in Figure 2-5. An overview of the experiments done in the first few days after the launch is illustrated in Figure 2-6. In the calibration graph the interdependency between calibrations is used to control the order of calibrations and update calibrated parameters. The update of certain parameters triggers the activation of other nodes, depending on some (boundary) conditions. Secondly, independent operating timers can trigger the activation of certain calibration nodes at different frequencies, depending on the known drift of certain parameters.

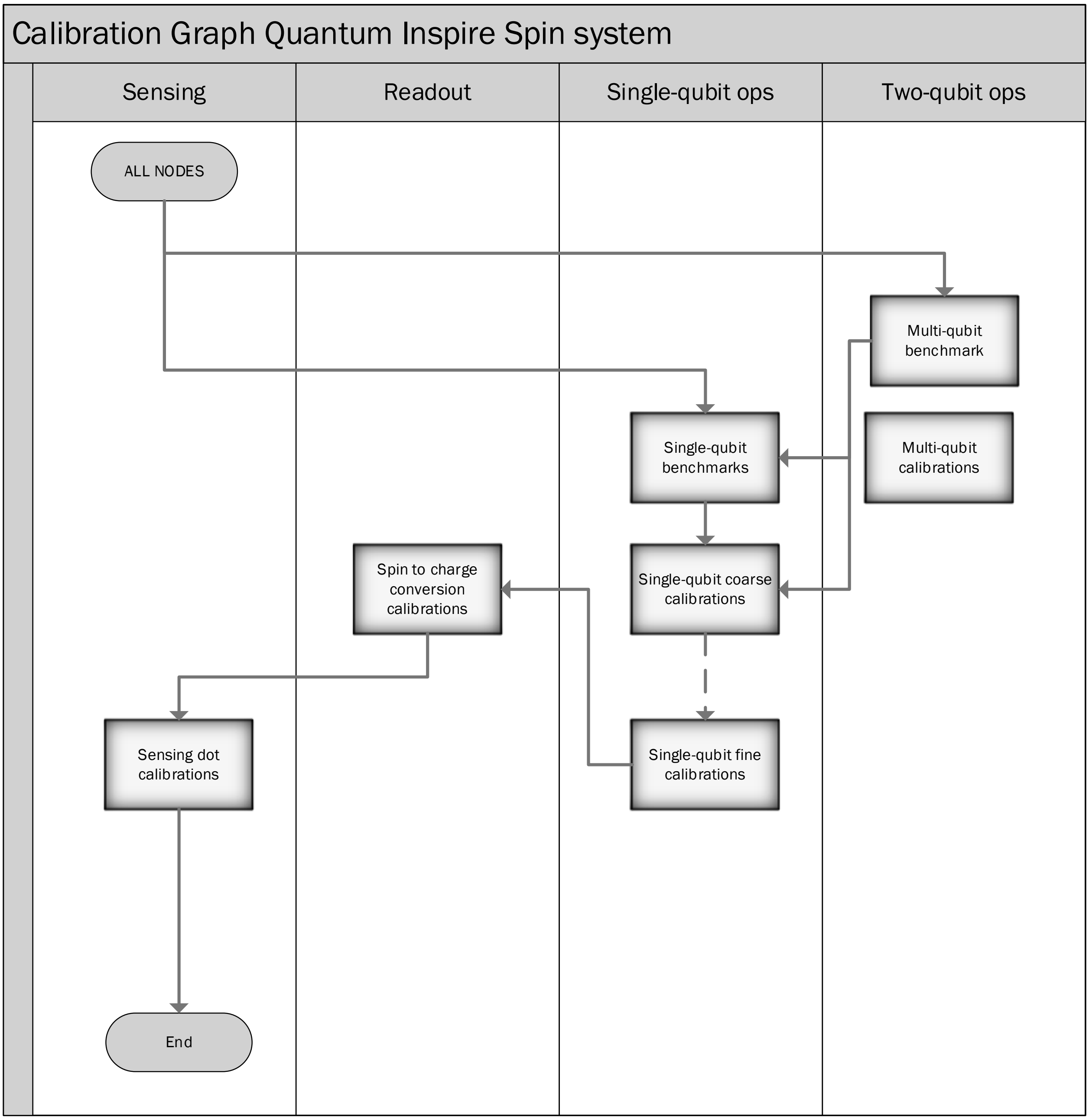


Figure 2-5 Calibration graph for Spin backend (highly simplified).

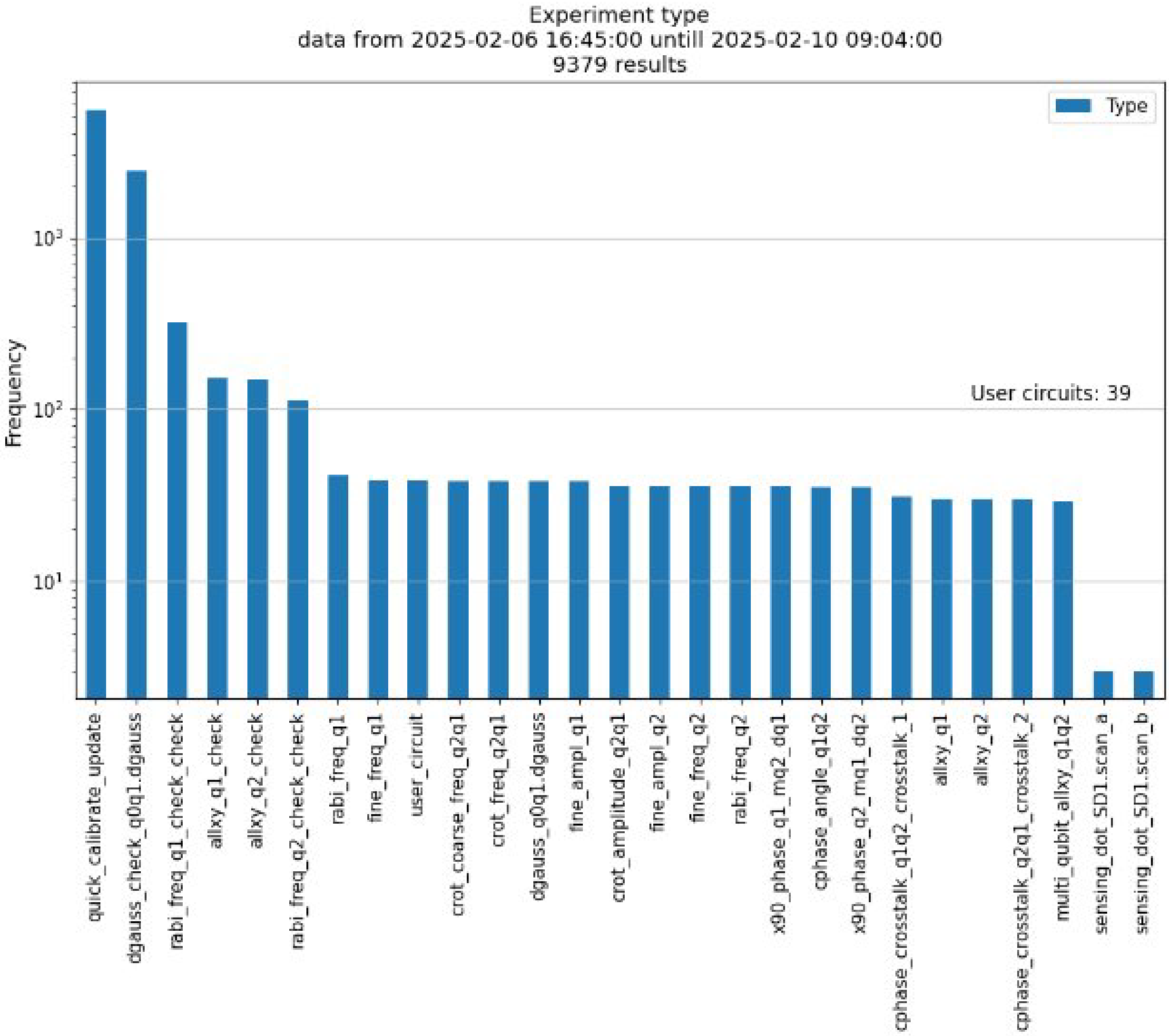
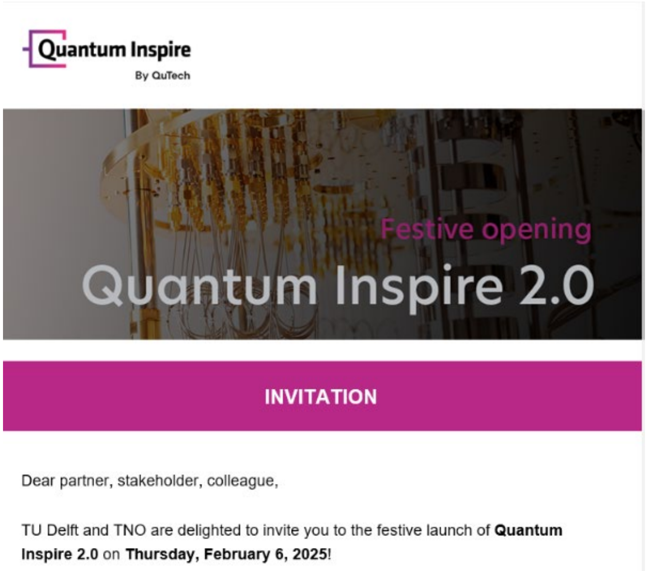
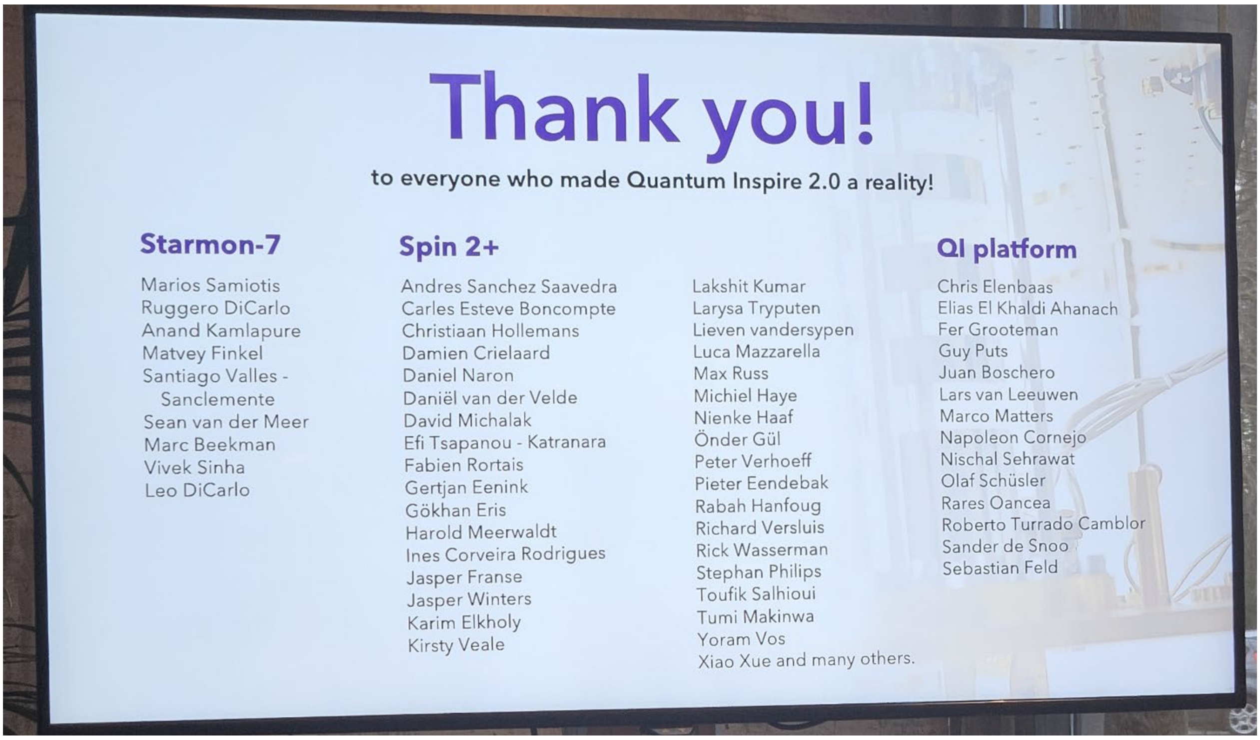


Figure 2-6 Overview of calibrations performed to keep Spin 2+ operational on 2025-02-06.

2.1.6. Dissemination

On Feb 6, 2025, we organized a public event to celebrate the launch of Quantum Inspire 2.0, with the Spin backend developed in QLSI (named Spin-2+), a hardware backend based on superconducting qubits, developed independently by TUD (not as part of QLSI project) and the new web interface, SDK and compiler suite. The event was visited by ~70 people with participants from the Dutch Ministry of Defence, The Dutch National Growth Fund Quantum technology, members from DG Connect and many visitors from the Dutch quantum ecosystem (companies, end users and academia).





The table below shows the main specifications of the new quantum computer (next to the specifications of the Spin quantum computer launched in 2020):

Key performance parameters	*Spin-2*	***Spin-2+***
Material	Si-28 in a 7 nm QW in SiGe	**Si-28 in a 6 nm QW in SiGe**
Single qubit gate control	EDSR microwave pulsing	**EDSR microwave pulsing**
Two-qubit gate control	Exchange interaction	**Exchange interaction**
Read-out method (spin to charge conversion)	Spin-selective tunnelling	**Pauli Spin Blockade (PSB)**
Visibility	~ 80%	**(98%) / 97% / 89%**
Energy relaxation time T1	> 20 ms (similar device)	**(280) / 181 / 261 ms**
Phase coherence time T2*	> 6 µs	**(3,4) / 1,5 / 6,4 µs**
Phase coherence time $T2^{Hahn}$	---	**(15,8) / 8,4 / 11,6 µs**
Single-qubit gate (X90) fidelity	~ 99,0% (avg per qubit)	**(99,8%) / 99,8% / 99,9%**
Two-qubit gate (CZ) fidelity	90,0%	**95,5%**
Qubit state preparation & readout fidelity [1]	~ 85% (avg per qubit)	**(96%) / 98% / 97%**
Single-qubit gate (X90) duration	250 ns	**(84) / 56 / 84 ns**
Two-qubit gate (CZ) duration	150 ns	**300 ns**
Readout duration (full register)	2 x 300 µs = 600 µs	**100 µs**
PSB integration time	n.a.	**37 us**

Notably, Spin-2+ demonstrates (relative to Spin-2):

- improved visibility: from 80% to **95%** on average
- improved single-qubit gate fidelity: from 99,0% to **99,8%**
- improved two-qubit gate fidelity: from 90% **to 95,5%**
- improved qubit state preparation and readout fidelity: from 72% to **97%**
- improved single-qubit gate duration: from 250 ns to **<90 ns**
- improved qubit register readout duration: from 600 µs to **100 µs**, at a single PSB readout duration of **37 µs**

2.1.7. Conclusion

The system was upgraded with the necessary hardware and software throughout the many subsystems. Online operation was achieved on 06-02-2025

[1] Benchmark method used does not distinguish state preparation from measurement errors.

2.2. Scope Changes

As explained in chapter 2.1.2, the current design of the quantum processors has 6 quantum dots and 2 sensing dots, which allows us to create 6 functional high-performance qubits. By exploiting PSB readout with one ancilla qubit we achieve fast readout with high fidelity with the cost of having one qubit less for operations. In future devices we expect that PSB readout could be a useful method to readout multiple qubits using multiplexing, making it a more favourable scalable solution for the future. Although the device has 6 operable qubits, which can be characterized and operated individually, we decided to make the online system available with only three dots (two qubits) due to the high cross talk between the other qubits. Otherwise, this would negatively affect the operation of the full system. With the project we started the design and manufacturing of a new design with 8 dots and 2 sensing dots and an improved micro-magnet design to eliminate these issues. This design will be the basis of a follow-up project (QLSI-2).

2.3. Major Risks and Actions Taken

Implementation of PSB. For details see D5.4.

2.4. Major Issues and Actions Taken

We have suffered up-time issues during the development stages. For details see D5.4.

2.5. Other On going and Planned Actions

Actions ongoing after this project:

- Developing the 8-qubit array with improved micro-magnet design
- QLSI-2 project
- Other projects

2.6. Achievements

Online quantum computer operational.