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## PID- and UVID-free n-type solar cells and modules

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### Abstract

In this paper we report on the high stability of our n-type front junction solar cells (n-PERT) exposed to potential-induced degradation (PID) and UV-induced degradation (UVID) conditions. These intrinsically stable n-Pasha cells enable PID- and UVID-resistant modules even with industrially low-cost standard EVA encapsulant, independent of system grounding and system voltage. Based on intentional modifications of the Boron emitter and/or the dielectric layer in the PID-free and UVID-free n-Pasha solar cells, we are able to replicate reported degradation effects and study the mechanisms behind it. A combination of altering the boron profile and the dielectric properties together with increasing the interface defect density  $D_{it}$  is detrimental for the stability. Applying our standard optimal B-diffusion and passivation scheme assure that the UV radiation and system voltage have virtually no effect on our n-Pasha cell and module performance.

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### 1. Introduction

In this paper we present potential-induced degradation (PID) and UV-induced degradation (UVID) resistant n-type c-Si solar cells enabling PID- and UVID-resistant modules even with common ethyl vinyl acetate (EVA) encapsulant, and independent of system grounding and system voltage.

The PID effect is a power loss of photovoltaic modules due to applied high system voltage. It has mainly been observed in standard front junction p-type c-Si modules [1]. The degradation mechanism has been attributed to massive shunting ( $FF$  loss) caused by  $\text{Na}^+$  ions bridging across the emitter [2]. PID was also observed in rear-contact IBC n-type cells and related to polarization effects leading to a passivation loss [3]. Although our n-Pasha (Passivated all sides H-pattern) cells and modules are resistant to PID and UV exposure, it has recently been reported that front junction (FJ) n-type based modules can suffer from PID [4, 5]. In contrast to p-type, no  $FF$  reduction but  $I_{sc}$  and  $V_{oc}$  loss was observed. The degradation was attributed to increased surface recombination [4] though the exact mechanism was still unclear. Similarly, a passivation loss was observed while exposing n-PERT (Passivated Emitter, Rear Totally Diffused) cells [6] to UV radiation resulting in UV-induced degradation (UVID).

As PID occurs at negative voltages for p-type cells [2] and at positive voltages for n-type IBC (Interdigitated Back Contact) cells [3] or n-PERT cells [5,7], PID can be prevented by grounding the system, respectively, at the negative and the positive connector/pole, thus preventing the degradation inducing system voltages. However, this solution is not possible with ‘floating’ PV systems and halves the possible voltage range for grounded systems, thus increasing the balance of system costs.

The amount of PID in PV modules can be strongly reduced by applying encapsulants with higher electrical resistance thus reducing the polarization effects [5,7]. However, the cost of these encapsulants, like e.g. polyolefin, is higher than for commonly used EVA.

During the development of our n-Pasha cells over the past years, a thorough understanding has been built up on why our n-type c-Si solar cells are both PID- and UVID-free. We present results on cells with intentionally modified dielectrics and emitters to demonstrate the effect dielectrics and emitter profiles can have on PID and UVID. We also present modelling studies showing the degradation effects are consistent with deteriorating surface passivation. Our PID- and UVID-free cells presented in this paper can be integrated in modules without the necessity of using non-standard (and more expensive) encapsulants, and without restrictions on the system voltage range and on the choice or absence of grounding, providing a low-cost solution to manufacture UVID- and PID-resistant modules.

## 2. Approach

### 2.1. Cell preparation

The n-Pasha cells (Cz Si,  $156 \times 156 \text{ mm}^2$  semi-square) are prepared according to standard industrial processes on industrial tools. The cross-section of such n-Pasha cell is presented in Fig. 1. Intentionally introduced modifications into the processing of the Boron (B)-emitter and the dielectric front side layer were applied to reproduce degradation effects that have been observed by others [4,5]. Table 1 summarizes the modifications for the different samples. These variations did not significantly affect initial cell efficiencies. For PID testing, cells with soldered tabs are laminated into (single-cell) mini-modules using a commercial, fast-cure EVA encapsulant. A selection of non-laminated n-Pasha cells, produced together with the cells for PID tests, undergoes UVID testing.

Table 1. Overview of the intentional modifications and performed tests for the standard and experimental groups.

	Standard	Experimental 1	Experimental 2	Experimental 3	Experimental 4
Boron emitter	stable	modified	modified	Stable	modified
Dielectric	stable	stable	modified A	modified B	modified B
PID test	yes	yes	yes	yes	yes
UVID test	yes	yes	no	no	yes

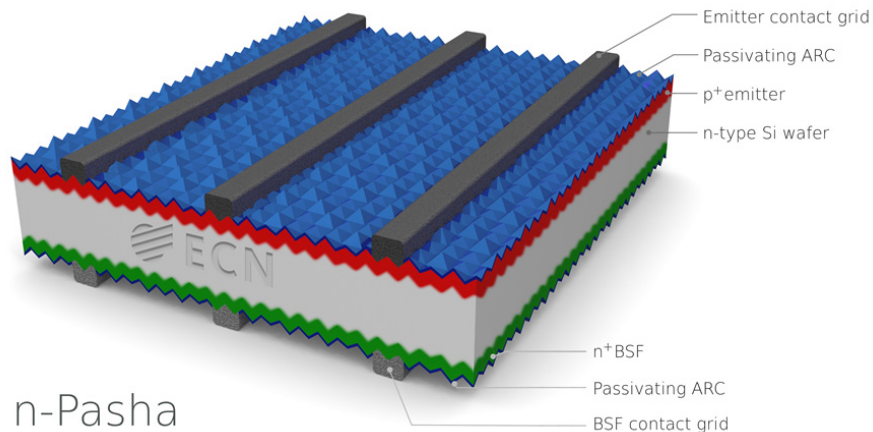


Fig. 1. n-Pasha cell architecture featuring PID- and UVID-resistant B-emitter and dielectric layer –denoted as anti-reflective coating (ARC).

## 2.2. PID testing

The mini-modules are exposed to high-voltage stress conditions in a dedicated climate chamber (-1000V, 60°C, 85% relative humidity (RH)) for 20 h steps. The  $I$ - $V$  characteristics are measured before the exposure and after each step to monitor the evolution of the module stability. PID exposure is finalized after a total of 100 h to be in line with the method discussed by NREL [8].

## 2.3. UVID testing

For the exposure to UV radiation an ATLAS UV-tester (351 nm, 1.55 W/m<sup>2</sup>/nm, total UV irradiance 62 W/m<sup>2</sup>) is applied. The UV exposure is carried out in a few steps until 320 h is reached. The  $I$ - $V$  characteristics are measured before the exposure and after each step to monitor the evolution of the cell stability. The 320 h of direct UV exposure of n-Pasha cells in the ATLAS UV-tester corresponds roughly to a direct continuous 20 kWh/m<sup>2</sup> UV radiation at cell level. In modules with UV-absorbing encapsulants and solar glass the yearly UV dosage is significantly reduced and 20 kWh/m<sup>2</sup> direct indoor UV radiation at cell level can be only roughly approximated to circa 1 year outdoors in Central Europe.

## 2.4. Modelling

The effect of deteriorating surface passivation of the B-emitter in n-Pasha cells was investigated by numerical simulations. The Atlas device simulation package by Silvaco [9] was used with the parametrization and physical models for the n-Pasha cell described elsewhere [10]. The effective surface recombination velocity parameter  $S$  of the emitter was varied between  $2 \cdot 10^3$  cm.s<sup>-1</sup> and  $1 \cdot 10^7$  cm.s<sup>-1</sup>.  $S$  represents the surface recombination velocity  $S_n$  caused by surface defects (thus related to  $D_{it}$ ) corrected for changes of the minority concentration induced by charges at the surface. The value of  $S = 2 \cdot 10^3$  cm.s<sup>-1</sup> represents a well passivated B-emitter surface. Increasing positive charge density at the interface will result in depletion which would lead to an increase of the effective  $S$ . At  $S > 1 \cdot 10^7$  cm.s<sup>-1</sup> surface recombination for this emitter is transport limited.

### 3. Results

#### 3.1. PID stability

Fig. 2 shows the time evolution of the mini-module relative efficiency loss, for various combinations of B-emitters and dielectric coatings exposed to PID conditions (-1000 V, 60°C, 85% RH). Our typical n-Pasha cells with the stable B-emitter and the stable dielectric show very high PID-stability (~1% relative efficiency loss after 100 h). However, for the combination of intentionally adjusted processing for the modified B-emitter and the modified dielectric of type-B the PID loss is reaching a saturation level of circa 12% already after ~40 h. In the case of the stable B-emitter, in combination with the modified dielectric B, deterioration is slower but after 100 h the same level of degradation is observed. For the modified B-emitter combined with the modified dielectric of type-A (different modification compared to dielectric B) the power loss is much smaller, reaching ~5% after 100 h, which is close to the pass/fail level of degradation as proposed by NREL [8], although no saturation of the efficiency loss is observed. These data show that although the combination of the modified emitter and the modified dielectric (A or B) is sensitive to fast PID degradation, the amount of PID loss is much lower than reported for n-type IBC [3] or p-type FJ solar cells [1]. Since modifications in the dielectric layer processing show the largest effect on PID, it suggests that the underlying mechanism is most sensitive to properties of the dielectric layer. This is further confirmed as the ultimate PID-solution in the form of the stable dielectric coating can be combined with either stable or modified B-emitter. Both combinations show similarly high PID-stability after a full PID-exposure test. A stability overview of the discussed combinations of stable/modified B-emitter/dielectric is presented in Table 2.

Fig. 2. also presents the time evolution of a relative efficiency loss expressed as  $J_{sc} * V_{oc}$  loss which is closely matching with the time evolution of the relative efficiency. The origin of these PID losses, manifested mainly by  $J_{sc}$  and  $V_{oc}$  deterioration and not by  $FF$  loss, will be discussed in section 4.1.

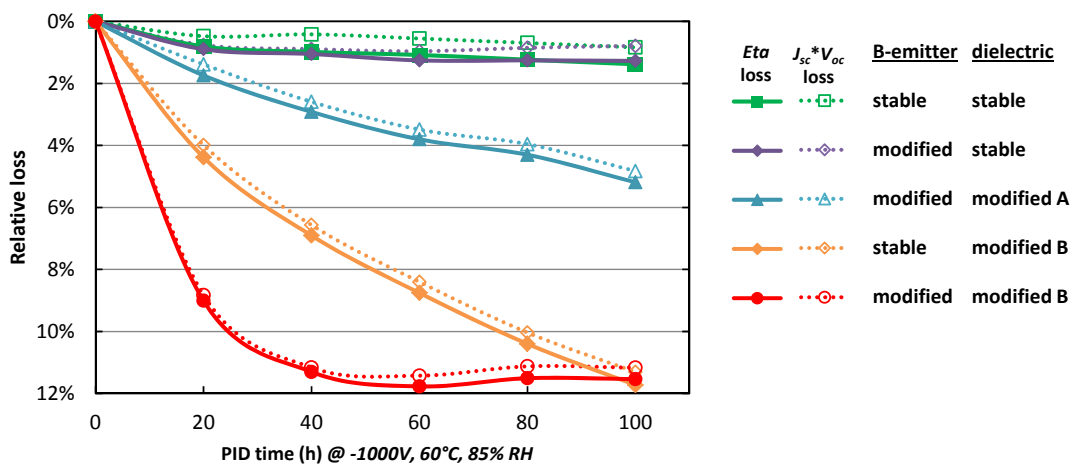


Fig. 2. Time evolution of the relative efficiency compared to initial values for n-Pasha single cell laminates (mini-modules) tested till 100 h PID exposure (-1000V, 60°C, 85% RH) plotted with solid symbols. Additionally the relative  $J_{sc} * V_{oc}$  loss is plotted with open symbols. Solid and dotted lines are to guide the eye.

#### 3.2. UVID-stability

Fig. 3 shows the time evolution of the relative efficiency loss for n-Pasha cells with various combinations of B-emitters and dielectric coatings exposed to direct UVID. Our stable n-Pasha cells show high UVID-stability (<<1% loss after 320 h). Similarly for the modified B-emitter combined with the stable dielectric layer the power loss is also negligible (the minor improvement of the relative efficiency is within the measurement error). However, for the intentionally modified B-emitter and the modified dielectric layer (type B) a large UVID loss does occur reaching

circa 4% loss already after 160 h UV exposure. This suggests that the underlying UV induced degradation mechanism is most sensitive to properties of the dielectric layer. A stability overview of the discussed combinations of stable/modified B-emitter/dielectric is presented in Table 2.

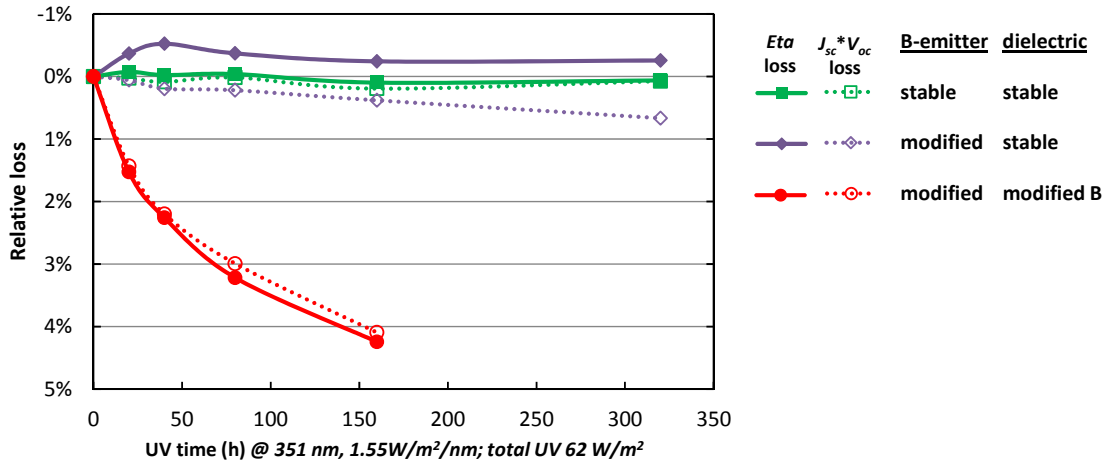


Fig. 3. Time evolution of the relative efficiency compared to initial values of selected n-Pasha cells exposed to UVID plotted with solid symbols. Additionally relative efficiency  $J_{sc} * V_{oc}$  loss is plotted with open symbols. Solid and dotted lines are to guide the eye.

Table 2. Stability overview of the investigated combinations of B-emitters and dielectrics.

	stable dielectric	modified dielectric B
stable B-emitter	PID: ☺	PID: ☹
	UVID: ☺	UVID: N.A.
modified B-emitter	PID: ☺	PID: ☹☹
	UVID: ☺	UVID: ☹

## 4. Discussion

### 4.1. Discussion on PID mechanism

Fig. 4 shows a schematic cross-sectional view of an n-type module exposed to a high system voltage. A strong cell potential bias (with respect to the frame of the module) induces a small leakage current  $j_D$  through the module. In the case of a negative bias, this results in accumulation of positive charges at the front side of the cell. These positive charges are either electronic in nature, i.e. an oxidized state in the nitride or oxide, or can result from mobile  $Na^+$  ions present in the module materials. The positive charges accumulated at the front of the cell destroy the surface passivation of the B-emitter as they attract electrons (minorities) to the emitter surface and the SRH recombination ( $S$ ) increases. Here  $S$  represents the surface recombination velocity  $S_n$  caused by surface defects, corrected for changes of the minority concentration induced by charges at the surface, i.e.  $S = S_n \cdot n_s / n_d$ . Here  $n_s$  is the electron (minority) concentration at the surface in the presence of charges, and  $n_d$  is the electron concentration without charges. As the charge increases, the surface concentrations of the charge carriers move towards inversion due to band bending [11], i.e.  $n_s$  and therefore  $S$  is expected to change by orders of magnitude. This so-called polarization effect will have detrimental effects mainly on  $J_{sc}$  and  $V_{oc}$  as modelled and depicted in Fig. 5. The saturation of the degradation effect at high values of  $S$  indicates that the surface recombination is becoming transport limited.

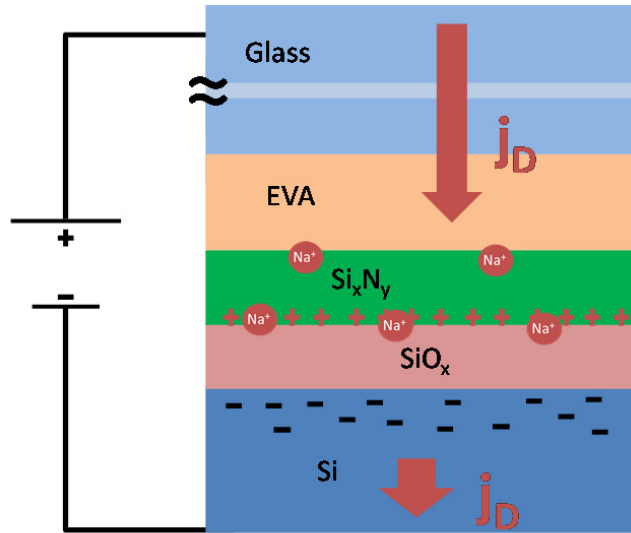


Fig. 4. Schematic drawing of proposed PID mechanisms. In the case of a negative bias, positive charges accumulates at the front side of the cell. These positive charges are either electronic in nature or can result from mobile  $\text{Na}^+$  ions present in the module materials.

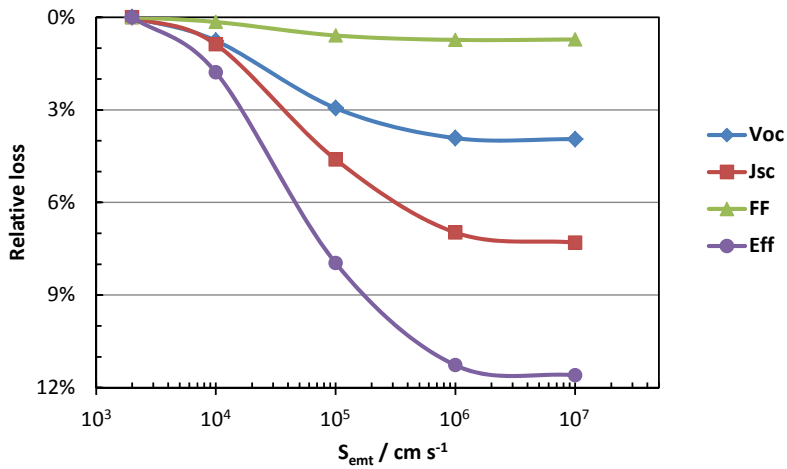


Fig. 5. Modelled effect of passivation loss of the B-emitter on the cell performance.

Modelled degradation values for  $S=10^5 \text{ cm.s}^{-1}$ ,  $S=10^6 \text{ cm.s}^{-1}$  and  $S=10^7 \text{ cm.s}^{-1}$  are shown in Fig. 6, together with the experimentally observed degradation. For the considered case of the modified B-emitter and the modified dielectric B (see Fig. 2), the experimentally observed degradation as presented in Fig. 6 agrees with a strong increase of the effective  $S$ . Thus the proposed model is in line with the observed phenomenological degradation.

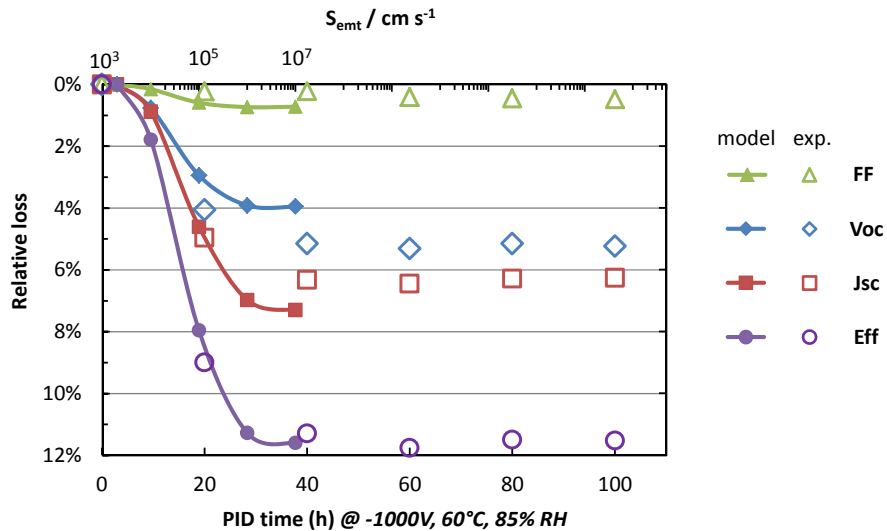


Fig. 6. Comparison of relative losses in  $FF$ ,  $V_{oc}$ ,  $J_{sc}$  and efficiency observed experimentally (PID exposure, open symbols) with modelled passivation loss of the B-emitter (closed symbols). Solid lines are to guide the eye.

PID can be thus avoided by i) preventing transport of positive charges or by ii) reducing the impact of accumulated positive charges. On cell level only the latter can be achieved by a proper configuration of e.g.: a) the dielectric layer properties, b) the interface properties and c) the B-emitter profile. Our stable n-Pasha cells are thus PID-resistant.

#### 4.2. Discussion on UVID mechanisms

The UV-radiation may affect both chemical and field-effect passivation. Interface defect states can be activated by UV-radiation leading to an effective increase of their density ( $D_{it}$ ). This is causing a deterioration of the chemical passivation. The fixed charges  $Q_f$  at the interface may be affected by the UV-radiation leading to a deterioration of the field-effect passivation. Both effects can result in efficiency loss due to deterioration of B-emitter surface passivation, as shown in Fig. 3, consistent with modelling (Fig. 5). UVID can be thus avoided by e.g. a) reducing initial  $D_{it}$  and b) optimizing the boron profile of the emitter. Our stable n-Pasha cells are thus UVID-resistant.

The same mechanisms play a role in our IBC cells with front-floating emitter, which have also demonstrated stable PID and UVID behaviour (data not shown here).

## 5. Conclusions

We report on the high stability of our n-type front junction solar cells (n-Pasha) exposed to potential-induced degradation (PID) and UV-induced degradation (UVID), with a power loss of only ~1% and <0.5% for NREL's proposed PID test [8] and ~20 kWh/m<sup>2</sup> direct UV exposure, respectively. Our n-Pasha cells are PID-free and UVID-free owing to a controlled processing based on a thorough understanding of the interaction between induced degradation and cell production. Based on intentional modifications of the B-emitter and/or the dielectric layer in our PID-free and UVID-free n-PERT solar cells we are able to reproduce degradation effects reported by others, and study the mechanisms behind it. A combination of tuning the boron profile and the dielectric properties together with decreasing the interface defect density  $D_{it}$  is beneficial for reducing the degradation. Therefore, the UV radiation and polarisation have negligible effect on our n-PERT cell performance.

The PID- and UVID-free n-PERT cells presented in this paper can be integrated in modules without the necessity of using non-standard (and more expensive) encapsulants, and without restrictions on the system voltage range and the choice or absence of grounding, providing a low-cost solution to manufacture UVID and PID resistant modules.

## References

- [1] Berghold J, Frank O, Hoehne H., Pingel S, Richardson B, Winkler M. Potential induced degradation of solar cells and panels. Proc. 25th EUPVSEC, Valencia, Spain, 2010, p. 3753-3759.
- [2] Naumann V, Lausch D, Graff A, Werner M, Swatek S, Bauer J, Hähnel A, Breitenstein O, Großer S, Bagdahn J, Hagendorf C. The role of stacking faults for the formation of shunts during potential-induced degradation of crystalline Si solar cells. Phys. Status Solidi RRL 2013; 7:5-315.
- [3] Swanson R, Cudzinovic M, DeCeuster D, Desai V, Jürgens J, Kaminar N, Mulligan W, Rodrigues-Barbarosa L, Rose D, Smith D, Terao A, Wilson K. The surface polarization effect in high-efficiency silicon solar cells. Technical Digest of the 15th PVSEC, Shanghai, China, 2005, pp 410-411.
- [4] Pingel S, Janke S, Frank O. Recovery methods for modules affected by potential induced degradation (PID). Proc. 27th EUPVSEC, Frankfurt, Germany, 2012, p. 3379-3383.
- [5] Hara K, Jonai S, Masuda A. Potential-induced degradation in photovoltaic modules based on n-type single crystalline Si solar cells. Solar Energy Materials & Solar Cells 2015; 140 – 361.
- [6] Zhao J, Schmidt J, Wang A, Zhang G, Richards BS, Green MA. Performance instability in n-PERT silicon solar cells. Proc. 3rd World Conference on Photovoltaic Energy Conversion, 2003; pp 1- 923.
- [7] Halm A, Schneider A, Mihailitchi VD, Koduvelikulathu LJ, Popescu LM, Galbiati G, Chu H, Kopecek R. Potential-induced Degradation for Encapsulated n-type IBC Solar Cells with Front Floating Emitter. Energy Procedia 2015; 77 - 356.
- [8] Hacke, P., Smith, R., Terwilliger, K., Perrin, G., Sekulic, B. and Kurtz, S. Development of an IEC test for crystalline silicon modules to qualify their resistance to system voltage stress. Prog. Photovolt: Res. Appl. 2014; 22 - 775.
- [9] Atlas Device Simulator, Silvaco Int. Software., Santa Clara, CA, USA, 2014.
- [10] Fell A, McIntosh KR, Altermatt PP, Janssen GJM, Stangl R, Ho-Baillie A, Steinkemper H, Greulich J, Muller M, Byungsoo M, Fong KC, Hermle M, Romijn IG, and Abbott MD. Input Parameters for the Simulation of Silicon Solar Cells. IEEE Journal of Photovoltaics 2015; 5 - 1250.
- [11] Aberle AG, Crystalline Silicon Solar Cells; Advanced Surface Passivation and Analysis. Center for Photovoltaic Engineering, University of New South Wales, Sydney, Australia; 1999.