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WILEY-VCH

Phys. Status Solidi A **210**, No. 4, 732–736 (2013) / **DOI** 10.1002/pssa.201200568

Part of Special Issue on
Advanced Concepts for Silicon Based Photovoltaics

physica status solidi a
www.pss-a.com
applications and materials science

# Surface passivation for ultrathin $Al_2O_3$ layers grown at low temperature by thermal atomic layer deposition

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Received 9 August 2012, revised 26 September 2012, accepted 12 October 2012
Published online 3 December 2012

**Keywords** $Al_2O_3$, interface states, oxide charge, silicon surface passivation, thermal ALD

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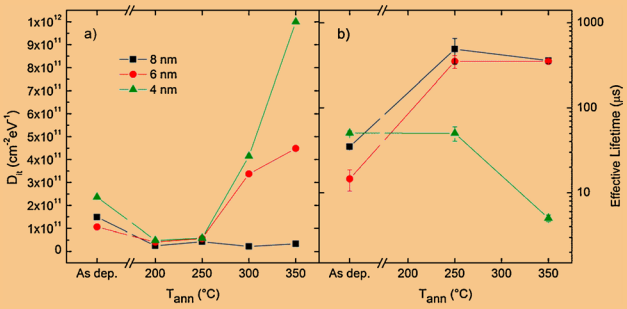
Thin layers of $Al_2O_3$ with thickness $t_{ox} \leq 8$ nm were grown by thermal atomic layer deposition at low temperature of 100 °C and applied to achieve functional surface passivation of crystalline silicon substrates. Measurements of the effective lifetime were performed to characterize the surface passivation effect. Lifetime values in the range of 0.5 ms were obtained for $Al_2O_3$ films with $t_{ox} \geq 6$ nm upon post-deposition annealing (PDA) at 250 °C in $N_2$ atmosphere. However, when the thickness of the $Al_2O_3$ films was reduced to 4 nm, lifetime values well below 0.1 ms were observed even after PDA. Combined capacitance–voltage and conductance–voltage measurements were carried out to extract the amount of charges located near the silicon-oxide interface and the density of electrically active interface states, respectively. The results of the electrical characterization were used to elucidate the intimate physical mechanisms that govern charge recombination at the $Al_2O_3$/Si interface.




Density of interface states (a) and lifetime (b) values are reported as a function of the PDA temperature for $Al_2O_3$ films of three different thickness values: 4, 6, and 8 nm.



**1 Introduction** Surface passivation of crystalline silicon wafers by aluminium oxide processed by atomic layer deposition (ALD) was demonstrated to give very high minority carrier lifetimes and consequently very low surface recombination velocities [1–5]. As a result, those layers were successfully implemented for both p- and n-type solar cell device applications [6–9]. The impressive performance of aluminium oxide layers is related to the combination of excellent chemical surface passivation, lowering the interface defect density, and oxide-trapped charges located near the semiconductor-oxide interface. The latter effect results in building up a high electric field, which is found to shield the minority carriers from the interface [4, 10, 11]. This mechanism is particularly efficient with p-type silicon surfaces since the $Al_2O_3$ oxide charges usually exhibit negative polarity. It is worth noting that annealing is always necessary to achieve the high level of surface passivation reported in the literature.

The low concentration of defects at the $Al_2O_3$/Si interface is attributed to the diffusion of hydrogen from the hydrogen-rich bulk of the oxide film to the interface and thus saturating the silicon dangling bonds. In addition, $Al_2O_3$ can act as a capping layer preventing the loss of hydrogen from the upper surface during annealing [12–14]. The very high carrier lifetime is strongly related to the oxide thickness. Thinner layers can be preferred due to their advantages related, for example, to shorter process durations and possibility of less complicated integration in specific device

structures. However, for $Al_2O_3$ deposited by thermal ALD reducing the layer thickness below 10 nm results in a rapid decrease of the lifetime from about 1 ms to only a few tens of μs [2, 4]. This thickness dependence is explained by a substantial increase of the interface defect states, since the oxide charge is demonstrated to remain constant even for very thin oxides [4, 10]. It should be noted that in the cases mentioned above, samples of different $Al_2O_3$ layer thickness processed with a particular ALD method are annealed at the same temperature in the range typically of 350–425 °C. Duration times of about 10–30 min are usually applied at this stage. In this connection, no detailed investigation has been reported on the correlation between annealing temperature and layer thickness with respect to the surface passivation properties of $Al_2O_3$ layers below 10 nm.

In this work, we focus on the feasibility of a low thermal budget passivation in order to reach a functional compatibility with low temperature solar cell processes [15–17]. We explore the surface passivation behavior of aluminium oxide films thinner than 10 nm by means of combined electrical characterization and lifetime measurements. The layers were grown at 100 °C by thermal ALD. The chosen temperature is significantly lower than the typical value of 200 °C applied for this type of ALD-process. The best passivation performance is achieved after a post-deposition annealing (PDA) at 250 °C for a relatively short time of 5 min. The result is understood in terms of a decrease of the surface defect states in combination with the formation of a negative charge density in the proximity of the $Al_2O_3$/Si interface.

## 2 Experimental details

**2.1 Sample preparation** Single and double polished p-Si 4'' FZ wafers with a resistivity of 1–5 Ωcm and a thickness of $280 \pm 25$ μm were used for electrical characterization and lifetime measurements, respectively. The H-terminated Si(100) surfaces were obtained by standard cleaning in $HCl:H_2O_2:H_2O = 1:1:5$ solution for 10 min at 85 °C followed by 30 s dip in diluted HF ($HF:H_2O = 1:50$) at room temperature.

The $Al_2O_3$ films were grown by thermal ALD (Savannah 200 system by Cambridge NanoTech) at 100 °C using trimethyl-aluminium (TMA) and $H_2O$ as precursors. More details about the deposition conditions are reported in Ref. [18]. In the case of double-sided polished p-Si wafers, the $Al_2O_3$ films were grown in a single process on both sides of the wafer in order to avoid any difference between the two $Al_2O_3$/Si interfaces.

After deposition, the samples underwent a rapid thermal annealing process at temperatures ranging from 200 to 350 °C in $N_2$ ambient for 5 min in order to study the effect of different thermal treatments on the electrical characteristics and passivation properties of the $Al_2O_3$ thin films. The oxide thicknesses were measured before and after the annealing process by means of spectroscopic ellipsometry using an M2000-F (J.A. Woolliam Co., Inc.). A small and constant shrinking (∼7%) of the $Al_2O_3$ films is observed after the anneal irrespective of the temperature. In the following paragraphs, data are reported as function of the film thickness in as deposited state.

**2.2 Capacitance–voltage and conductance–voltage measurements** Metal-oxide-semiconductor capacitors were prepared for electrical testing of the $Al_2O_3$ films. Aluminium dots with a nominal area of 0.078 $mm^2$ were evaporated on the surface of the $Al_2O_3$ using a shadow mask, while the back contacts were fabricated evaporating a uniform layer of aluminium on the back surface of the samples. The actual area of the evaporated dots was afterward measured with an optical microscope.

Multi-frequency capacitance–voltage ($C$–$V$) and conductance–voltage ($G$–$V$) data were extracted from admittance measurements where the parallel capacitance and conductance were derived from its real and imaginary part, respectively. The frequency was varied from 1 kHz to 1 MHz. Series resistance correction was applied to all measurements before the $C$–$V$ and $G$–$V$ data analysis. The measurements were performed from inversion to accumulation and back from accumulation to inversion to check the presence of hysteresis loops in the $C$–$V$ characteristics.

**2.3 Lifetime** Lifetime performance and the surface passivation properties of the aluminium oxide layers were characterized with WCT-120 Silicon Wafer Photoconductance Lifetime Tester from Sinton Instruments. The measurements were carried out on double side-coated samples with a good bulk lifetime (∼1 ms). A general analysis procedure was applied which includes the transient and the quasi-steady state modes as two extremes. The effective lifetime was measured as a function of the excess carrier density $\Delta n$ created by the flash illumination with the lamp. The results are reported for the value of $\Delta n = 10^{15}\,cm^{-3}$.

## 3 Results and discussion

**3.1 Electrical characterization** Multi-frequency $C$–$V$ and $G$–$V$ curves were acquired to check for frequency dependence of the acquired data. The results of this analysis for the 6 nm thick $Al_2O_3$ film are reported in Fig. 1. Beside variations of accumulation capacitance due to increased series resistance contribution at higher frequencies, the main differences can be observed in the range of voltages close to depletion. The corresponding peak in the $G$–$V$ curves let us assign this variation to the electrical response of interface defect states at different frequencies. The density of interface defect states ($D_{it}$) is determined from the analysis of the $G$–$V$ characteristics according to standard electrical characterization procedures [19]. An estimation of the maximum density of traps filled at a gate voltage corresponding to the half of the silicon band gap can be extracted from the $G$–$V$ peak position and height using the Hill–Coleman approximation [20] at a frequency corresponding to the maximum of the $G/\omega$ versus $\omega$ plot. In our measurements, such maximum is observed at a frequency of ∼100 kHz. Moreover, the flat band voltage shift $\Delta V_{fb}$ in the $C$–$V$ characteristics is

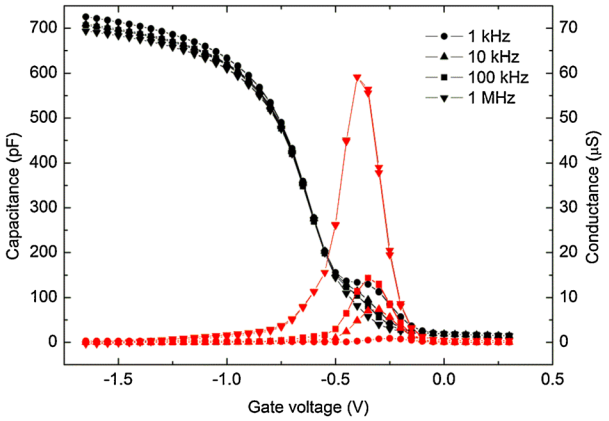



**Figure 1** (online color at: www.pss-a.com) Multi-frequency (1 kHz, 10 kHz, 100 kHz, and 1 MHz) *C–V* (black) and *G–V* (red) measurements for the 6 nm thick oxide sample after annealing at 350 °C for 5 min in $N_2$ ambient.

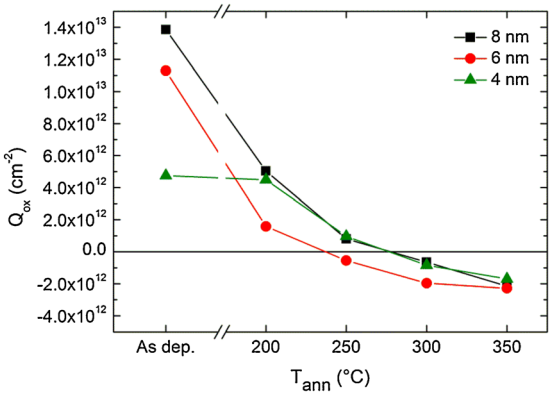



**Figure 3** (online color at: www.pss-a.com) Plot of $Q_{ox}$ derived from *C–V* measurements as a function of annealing temperatures for three different aluminium oxide layer thicknesses. Error bars are comparable or smaller in size than the symbols.

indicative of the oxide charges trapped in the $Al_2O_3$ film. The *C–V* experimental curves were fitted to theoretical-calculated curves including charge quantization at the silicon surface [21]. In this way, a good estimation of substrate doping, flat band shift, and accumulation capacitance could be extracted. No dependence of $\Delta V_{fb}$ on the frequency is observed. For these reasons, all the data analyses, which are reported in the following paragraphs, were carried out at 100 kHz.

**3.2 Oxide trapped charges and surface state density** The *C–V* curves for the as deposited and annealed samples as a function of the oxide thickness are reported in Fig. 2. A flat band voltage evolution is observed in the as deposited samples as function of the oxide thickness. Moreover, in all the samples, a $\Delta V_{fb}$ variation is detected upon thermal treatment. The observed shifts are related to the effective oxide charge according to the following equation $\Delta V_{fb} = \Phi_{ms} - Q_{ox}/C_{ox}$, where $Q_{ox}$ stands for the effective oxide charge, $C_{ox}$ is the accumulation capacitance, and $\Phi_{ms}$ indicates the work function difference between the metal and the semiconductor. It must be pointed out that using this method for calculating the effective oxide charge an error in the work function difference between the oxide and the semiconductor only leads to a systematic error that rigidly shifts the data along the $Q_{ox}$ direction and the general trends are preserved. The *C–V* curves show little hysteresis after the annealing process. The small hysteresis observed in the as deposited samples does not significantly affect the extraction of $Q_{ox}$ data.

In Fig. 3, the $Q_{ox}$ values for different oxide thicknesses as a function of PDA temperatures are shown. The as deposited samples exhibit a positive oxide charge density in accordance with previously reported results for samples grown by thermal ALD with a substrate temperature of 100 °C [22]. The amount of positive charges accumulated in the as deposited samples increases with oxide thickness, suggesting that either the positive charges are uniformly distributed within the oxide layer or a progressive charge accumulation close to the interface occurs during the deposition. Upon annealing in $N_2$ ambient a progressive reduction of the positive charges within the oxide is observed until a negative build-up charge is induced in all the samples for annealing temperatures $T_{ann} \geq 300$ °C. The negative

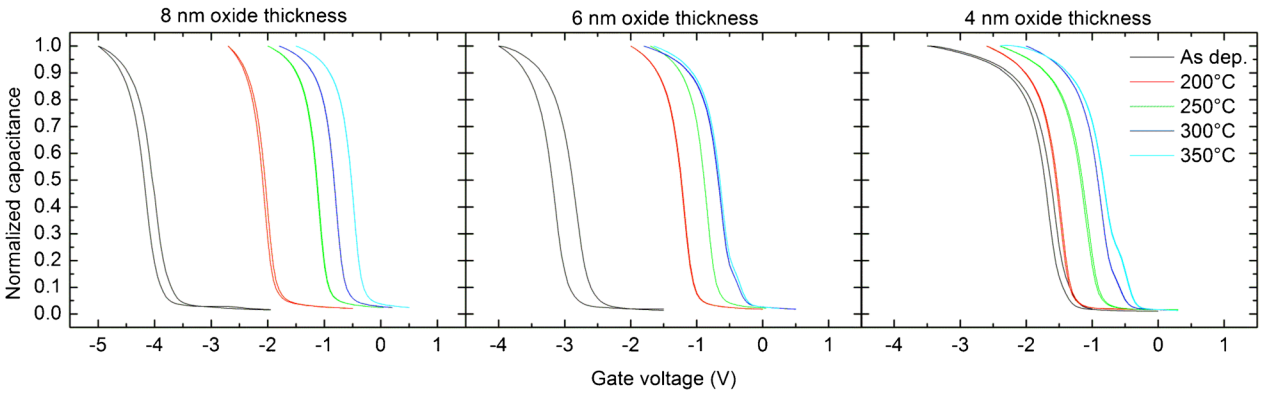



**Figure 2** (online color at: www.pss-a.com) Normalized capacitance–voltage measures acquired at 100 kHz for different annealing temperatures and oxide thicknesses.

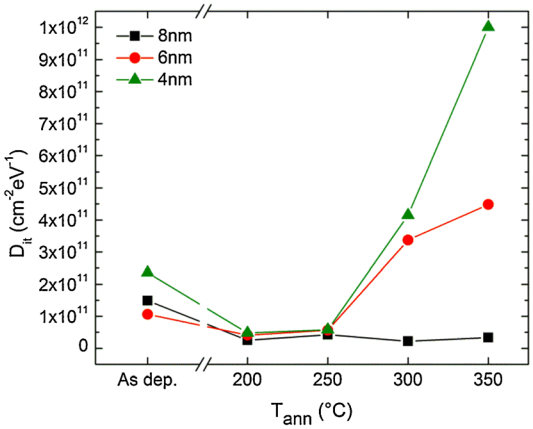



**Figure 4** (online color at: www.pss-a.com) Plot of $D_{it}$ derived from $G$–$V$ measurements as a function of annealing temperatures for three different aluminium oxide layer thicknesses. Error bars are comparable or smaller in size than the symbols.

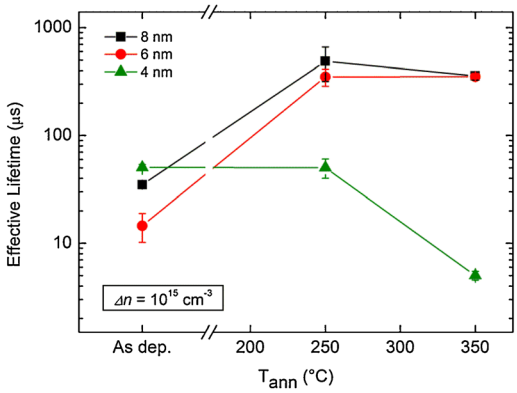



**Figure 5** (online color at: www.pss-a.com) Lifetime values for different oxide thicknesses as a function of annealing temperatures.

charge accumulation upon annealing at 350 °C is comparable to previously reported data for thermal ALD-grown samples [23]. Since the amount of effective negative charge accumulated in the $Al_2O_3$ films after the 350 °C PDA treatments does not change with the oxide thickness, we can conclude that the negative charges are located close to the oxide-semiconductor interface, which is inline with other reports [10].

It is worth noting that the $C$–$V$ measurements of 4 and 6 nm thick $Al_2O_3$ films show a bump near the depletion region of the curves after thermal treatment at $T_{ann} \geq 300$ °C. As previously discussed, these features in the $C$–$V$ curves measurements indicate the presence of electrically active interface traps. The analysis of the $G$–$V$ characteristics allows a proper quantifying of the corresponding $D_{it}$ values. In Fig. 4, the $D_{it}$ values for different oxide thicknesses as a function of PDA temperatures are shown. A slight reduction of $D_{it}$ is observed upon annealing at 200–250 °C. However, a strong increase in the $D_{it}$ values is observed after the 300 °C thermal treatment for the samples thinner than 8 nm. The effect is most pronounced for the lowest layer thickness of 4 nm. This behavior suggests a loss of chemical passivation in the thinnest oxides at $T_{ann} \geq 300$ °C.

**3.3 Surface passivation** In Fig. 5, we report the effective lifetime data for different aluminum oxide thicknesses as a function of PDA temperatures. A significant improvement is observed upon thermal treatment of the 6 and 8 nm thick $Al_2O_3$ passivation films. The increase is about one order of magnitude compared to the as-deposited state, due to the reduction of the $D_{it}$ and the changing of the $Q_{ox}$ from high positive values to a substantially neutral condition. Effective lifetimes of 0.5 ms have been reached for 8 nm thick $Al_2O_3$ passivating layers after anneal at 250 °C. The best result achieved is 0.66 ms which corresponds to effective surface recombination velocity (SRV) $S_{eff} \sim 8\,cm\,s^{-1}$. This passivation performance is within the range suitable for low temperature solar cell device applications [16]. However, the 4 nm thick $Al_2O_3$ films do not change significantly in passivation properties when temperature of 250 °C is used. Upon further increase to 350 °C the lifetime decreases by one order of magnitude compared to the initial state. The degradation of the lifetime values in samples thinner than 6 nm is consistent with previously reported data [2, 4]. This effect is usually ascribed to the loss of chemical passivation that the thinner samples experience upon annealing. To fully explain the lifetime results, an interplay between the $D_{it}$ and the $Q_{ox}$ data has to be considered. Surprisingly, the 4 nm thick $Al_2O_3$ film after annealing at 250 °C presents $D_{it}$ and $Q_{ox}$ values which are essentially equivalent to those measured in the 6 and 8 nm thick $Al_2O_3$ samples. These results suggest that, at this annealing temperature, other phenomena have to be considered in order to account for the loss of passivation effect in the 4 nm thick $Al_2O_3$ film. As discussed in the previous paragraph, the samples annealed at $T_{ann} = 350$ °C exhibit the same $Q_{ox}$ values around $-2 \times 10^{12}\,cm^{-2}$ irrespective of the thickness of the film, in agreement with data in the literature [10]. For $Q_{ox} \leq -5 \times 10^{11}\,cm^{-2}$ lifetime scales with $Q_{ox}^2$ and the field effect passivation is expected to be the driving force that determines effective passivation, relaxing the requirements on the $D_{it}$ [11]. For this reason, the increased $D_{it}$ in the 6 nm thick $Al_2O_3$ film does not induce a significant degradation of the lifetime, especially since the $Q_{ox}$ value remains about one order of magnitude higher than $D_{it}$. On the contrary, in the 4 nm thick $Al_2O_3$ film a further increase of the $D_{it} \sim 1 \times 10^{12}\,cm^{-2}eV^{-1}$ strongly affects the lifetime of the minority carriers suggesting that the field-effect passivation induced by the $Q_{ox}$ accumulation in the $Al_2O_3$ film cannot compensate the loss of chemical passivation associated with the increased $D_{it}$. For the 8 nm thick $Al_2O_3$ film, a very low $D_{it}$ value is obtained after annealing at 200–250 °C and this is preserved for $T_{ann} \geq 300$ °C. After the 350 °C PDA the level of negative oxide charge is higher than for the 250 °C PDA. This variation of the $Q_{ox}$ does not correspond to a further increase of the lifetime value. It is worth to notice that the low $D_{it}$ level obtained for the 8 nm

thick oxide sample implies the presence of a very limited number of recombination centers at the interface. Therefore, the reduction of the minority carrier concentration at the semiconductor interface, provided by the field-effect passivation, does not induce a further increase in the overall level of surface passivation.

**4 Conclusions** Crystalline silicon wafers were passivated with $Al_2O_3$ layers of thickness lower than 10 nm grown by thermal ALD at 100 °C. After deposition the samples were annealed using a low thermal budget process and subsequently analyzed to study the passivation performance of the thin ALD films. Even though low anneal temperatures for relatively short duration were applied, both $D_{it}$ and $Q_{ox}$ were influenced by this process. For the lowest applied layer thickness of 4 nm no effective passivation was achieved upon annealing irrespective of the $D_{it}$ and $Q_{ox}$ values. A clear improvement in the lifetime values was observed upon annealing at $T_{ann} \geq 250$ °C in the samples with thickness above 5 nm. The interplay between the $D_{it}$ and the $Q_{ox}$ data has to be considered in order to account for these results. In the case of the 4 nm thick $Al_2O_3$ oxide, the interplay between these two parameters is not enough to explain the low lifetime values and other phenomena have probably to be taken into consideration. In conclusion, SRV values in the range of 10 cm $s^{-1}$ were obtained, which are prerequisites for successful applications in low temperature solar cell devices.

**Acknowledgements** This work was supported by the EU via project NanoPV (FP7-NMP3-SL-2011-246331). Sabina Spiga (MDM) is acknowledged for support in electrical measurements. D. S. and J. vR. gratefully acknowledge Esther Cobussen-Pool (ECN) for the effective lifetime measurements and Petra Manshanden (ECN) for the fruitful discussions.

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