

Broader Perspectives

Crystalline Silicon Solar Module Technology: Towards the 1 € Per Watt-Peak Goal

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Crystalline silicon solar module manufacturing cost is analysed, from feedstock to final product, regarding the equipment, labour, materials, yield losses and fixed cost contributions. Data provided by European industrial partners are used to describe a reference technology and to obtain its cost breakdown. The analysis of the main cost drivers allows to define new generation technologies suitable to reduce module cost towards the short-term goal of 1 € per watt-peak. This goal roughly corresponds with the cost level needed to enable 'grid parity': the situation solar electricity becomes competitive with retail electricity. The new technologies are described and their costs are analysed. Cost reductions due to scale effects in production are also assessed for next generation manufacturing plants with capacities in the range of several hundreds of megawatts to one gigawatt of module power per year, which are to come in the near future. The combined effects of technology development and economies of scale bring the direct manufacturing costs of wafer-based crystalline silicon solar modules down into the range of 0.9–1.3 € per watt-peak, according to current insights and information (the range results from differences between technologies as well as from uncertainties per technology). Copyright © 2008 John Wiley & Sons, Ltd.

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INTRODUCTION

Photovoltaic (PV) solar energy is presented as an alternative source of electricity since it began to be developed in the 1950s and especially after the oil crises of the 1970s. It has a number of clear advantages, its environmentally friendly character being the main one, but also its elegance and simplicity, robustness, modularity, and of course the fact that its 'fuel' – solar

radiation – is widely spread all over the world. So far, manufacturing costs and prices of PV modules and systems have come down by more than an order of magnitude, and at the same time it has been possible to improve impressively the performance and overall reliability of PV systems. This, in combination with successful market incentives in a growing number of countries has enabled an enormous expansion of the PV market in the last decade, with annual growth rates in the range of 40–50%.¹

Although electricity from PV cannot yet compete directly with electricity from conventional sources on the level of wholesale or retail prices, it is already

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competitive during peak power times (usually in the middle of the day),² and according to a recent study by the European PV Technology Platform, it will reach 'grid parity' with retail prices in Southern Europe before 2015 and in most of Europe by 2020, if the tendency of cost decrease is maintained.³

The PV market is so far largely based on wafer crystalline silicon (c-Si) technology, which has a share of more than 90%, and still has a huge potential for further cost reduction, provided technology improvements and innovations continue to be implemented. This represents the main aim of CrystalClear,^a a European Integrated Project carried out in the 6th Framework Programme, which started in 2004 and will continue until the end of 2008. CrystalClear gathers expertise from nine industries, three universities and four research centres, aiming as a first goal at 'research, development, and integration of innovative manufacturing technologies that allow solar modules to be produced at a cost of 1 €/per watt-peak in next generation plants'.

CrystalClear deals with the entire crystalline silicon value chain from silicon feedstock up to module manufacturing. Since many combinations of options for cell and module design, processing and materials may potentially fulfil the project aims, careful prioritisation and selection of research topics is crucial. Moreover, research performed on the different parts of the chain is carefully coordinated and integrated in order to achieve results on a project level. In CrystalClear this process is performed through technology roadmapping, in combination with cost calculations and environmental analyses.

While results on environmental aspects have been presented elsewhere (e.g. see 4,5), as well as the roadmapping approach,⁶ this paper reports on the work performed within CrystalClear to evaluate the potential of alternative c-Si technologies now in the R&D stage to reach the manufacturing cost target of 1 €/watt-peak (Wp),^b revealing the key aspects that influence cost savings.

First, the steps taken to define a reference technology are described, and its cost breakdown is shown. The analysis of the main cost drivers allows inferring the issues that research should address to effectively reduce PV cost. These considerations lead to certain 'technology options', both in device designs

and in manufacturing processes, which should be combined in a specific 'new generation technology'. Six of these new technologies, which are representative of the alternative options currently being considered in R&D on c-Si, are then described and their costs are obtained, revealing their potential to lower the PV cost towards the 1 €/Wp goal. To complete the analysis, the cost saving potential due to large scale production is discussed.

ESTABLISHING A REFERENCE TECHNOLOGY

Industrial partners involved in the CrystalClear project have provided data on the cost structure of their PV technology. Data correspond to direct manufacturing costs by the end of year 2005, and cover silicon crystallisation, wafering, cell fabrication and module assembly. Data from different partners is extrapolated to similar production levels in the range of 30–50 MWp/a.

Note that we are always referring to cost and not price. This will help to make the analysis independent of external and temporary factors influencing PV price, such as the recent shortage of high-purity silicon.

Nine different European industries have participated. Depending on their company structure and business, some of them contributed to the whole value chain from crystallisation to module assembly, while others just covered some of the steps, or just a single one. In some cases, technologies are quite similar (such as wafering techniques, and the module assembly approach), but in others not (for instance, growth of multicrystalline or monocrystalline silicon crystals or cell processing).

Production costs have been distributed in the following categories: equipment (with 10 years for depreciation), labour, materials, yield losses and fixed costs. Energy and maintenance costs are included in equipment category, and consumables in materials. For cells and modules the cost breakdown has been given for the different process steps in which they can be divided. An aggregated figure, in €/kg, is estimated for silicon feedstock cost, since CrystalClear is not working on developing feedstock processes.

After collection, data have been averaged. The total cost of the PV module resulting from the benchmark exercise is in the range 2.0–2.3 €/Wp. This range relates to different technologies used, not to variation from manufacturer to manufacturer.

^aSee www.ipcrystalclear.info and references on that site.

^bThe term watt-peak (Wp) refers to the power that a solar module (or solar cell, or complete system) produces under standard operating conditions, which are, among others, defined as full sun (1000 watt/m² light intensity).

Table I. Description and main parameters of the reference technology Basepower

Overall technology name	Basepower
Feedstock	Electronic grade polysilicon at 40 €/kg
Crystallization	Ingot casting Good Si in/Si out per batch: 75% Recycled Si per batch: 20% Ingot yield: 95%
Wafering	Wafer size: $156 \times 156 \text{ mm}^2$ Wafer thickness: 220 μm Kerf loss: 200 μm Wafer yield: 92%
Cell processing	Front and rear screen-printed electrodes, aluminium back-surface field (Al BSF) Cell efficiency: 15% Cell yield: 93%
Module assembly	Front-to-rear interconnection, soldering, foil lamination, framing Cell efficiency in the module: 14.5% Module yield: 97%

By 'recycled silicon per batch' we refer to the reuse of 'scrap' silicon from a crystallization step in the subsequent run. By 'Cell efficiency in the module' we take into account the loss in output power due to cell interconnection and encapsulation. The other terms are defined as usual in the PV community.

The resulting manufacturing cost is in the range of other published data on manufacturing costs of PV producers,⁷ taking into account that our figures correspond to cost by the end of year 2005.

'Basepower' reference technology

This reference cost has helped in defining a representative technology, for which the most relevant parameters have been quantified. This baseline technology is called hereafter *Basepower*, and its main characteristics are summarised in Table I.

Taking all of these into account, the cost breakdown is shown in Figure 1. It corresponds to a Si usage of 9.1 g/Wp.

As shown in Figure 1b, directions of research are suggested by the analysis of the cost structure; for instance, the following goals should be pursued:^{3,8}

- Reduction of silicon consumption per Wp, or reduction of silicon cost per kg, or both, by means of applying new solar grade silicon feedstocks, improving the ingot growth, increasing the number of wafers per ingot and diminishing or completely

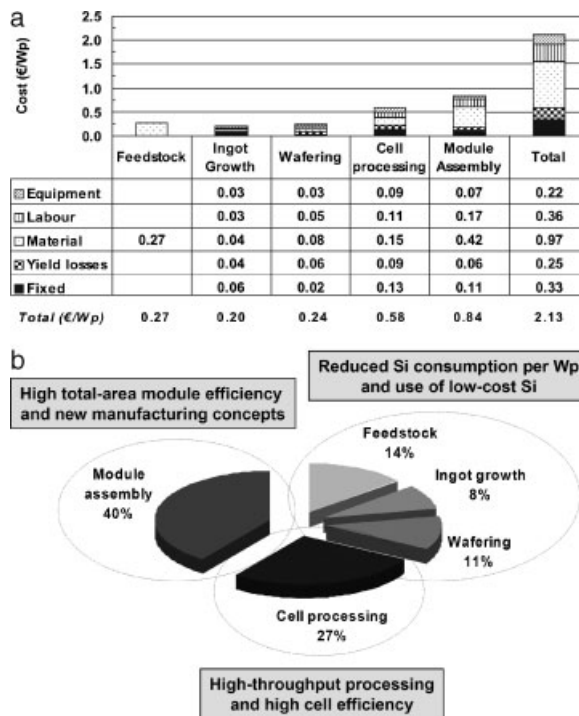


Figure 1. Cost structure of *Basepower* technology. (a) Breakdown by process step and by cost category, in €/Wp. (b) Cost breakdown in percentage, with indications on the basic approaches that should be followed for cost reduction

avoiding sawing losses (including silicon ribbon growth and the development of so-called thin-film wafer equivalents, i.e. a thin high quality crystalline silicon layer on a low cost substrate). Alternatively or in combination with the previous: the use of lower cost silicon feedstock (taking into account a possible efficiency penalty if it is also lower grade);

- High-throughput, high-efficiency cell processing, including implementing effective front and back surface passivation on thin wafers;
- High throughput, high total-area efficiency and low-cost module manufacturing, which can come by applying rear interconnection schemes for thin wafers and easy module assembly, and new interconnection and encapsulation materials and methods.

Sensitivity analysis

To give more insight in the potential of these lines of research, a sensitivity analysis of the influence of some

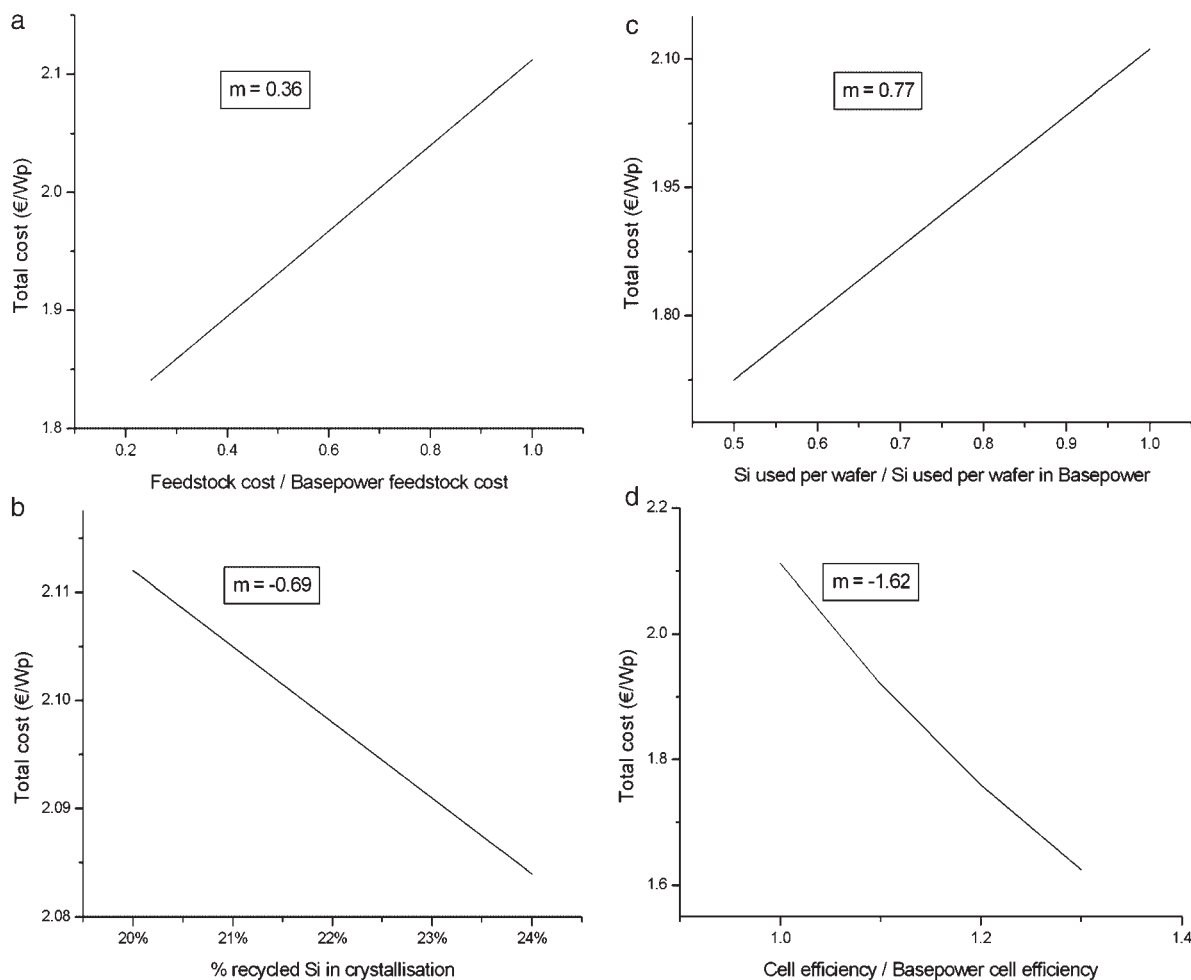


Figure 2. Influence of some cost drivers on the total cost of a PV module. (a) Feedstock cost. (b) Recycling of Si in crystallization. (c) Si thickness used per wafer (i.e. wafer thickness plus kerf width). (d) Encapsulated cell efficiency

of the main cost drivers has been performed, and the tendencies are shown in Figure 2. In particular, the analysis has focused on the impact of feedstock cost, the recycling of Si in the crystallisation step, the better usage of Si in wafering (by reducing wafer thickness and/or cutting loss), and the increase in cell efficiency. The dependencies in the four cases are practically linear, and their slope is indicated.

The analysis helps to quantify the cost reduction that can be expected with an improvement in one of the key parameters when pursuing the approaches mentioned in Figure 1b. Moreover, it points at the need of addressing simultaneously improvements in several parts of the value chain to have significant cost reductions.

PROPOSAL OF ALTERNATIVES: THE CRYSTALCLEAR ROADMAP SCENARIOS

Six technology scenarios have been considered in CrystalClear, combining options for the different steps of the value chain that are known or expected to be effective in terms of cost, manufacturability or efficiency. The combinations were selected to represent the different crystalline silicon technology families (cast multicrystalline silicon, Czochralski-grown (Cz) single crystal silicon, ribbon silicon and thin-film silicon wafer equivalents), and also to cover a range of potentials for cost reduction and corresponding development risk profiles. They are related to the

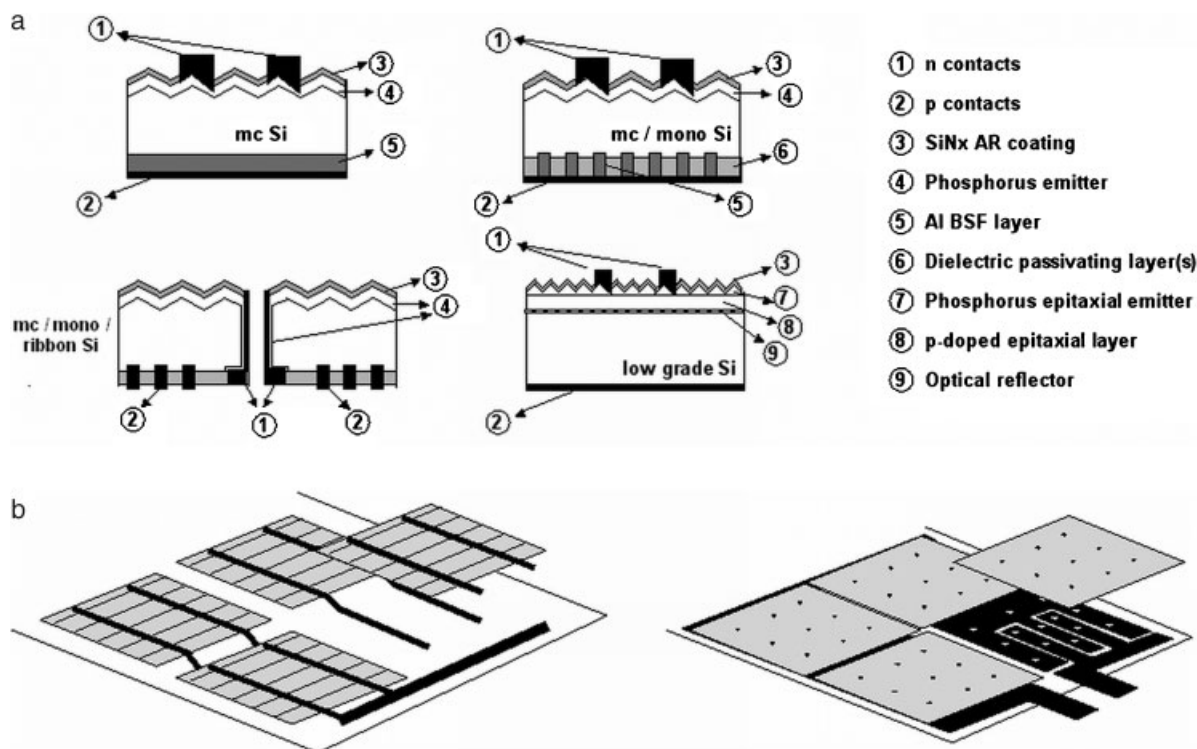


Figure 3. (a) Schematics of the cell structures proposed in the CrystalClear scenarios. Top in the left corresponds to Basepower; top in the right to front-and-rear-contacted Multistar and Superslice; bottom left to the all-rear-contacted MultistarR, SupersliceE and Ribbonchamp; and bottom right to Epi.C. (b) Schematics of the assembly approaches for the front-to-rear-contacted cells (left) and the all-rear-contacted cells (right). In both cases, solder joints are replaced by conductive adhesives

R&D lines being followed within CrystalClear, so that the assumptions related to each of the alternatives and to the prospects of implementation are largely based on the expertise of the CrystalClear partners.

These six technologies are briefly described in the following tables, and some drawings at the cell and module level are also given in Figure 3 to highlight the main innovations they include (additional details are described in the – confidential – CrystalClear Roadmap). They have been given names to facilitate easy identification. Multistar (Table II) is an advanced multicrystalline-silicon based module with medium technology risk profile,⁹ which can be implemented at the industrial level with high probability of success already on the short term. A modified version of Multistar (Table III) features a Metallisation Wrap-Through (MWT) design,^{10,11} enabling an all-rear interconnection scheme in the PV module.¹² Superslice (Table IV) implements a high efficiency cell structure on very thin monocrystalline silicon,^{13,14}

Table II. Description and main parameters of roadmap scenario Multistar

Overall technology name	Multistar
Feedstock	Solar grade polysilicon at 20 €/kg
Crystallization	Ingot casting Ingot yield: 95%
Wafering	Wafer thickness: 120 µm Kerf loss: 140 µm Wafer yield: 90%
Cell processing	Front and rear screen-printed electrodes, passivated rear side Cell yield: 96% Cell efficiency: 17%
Module assembly	Front-to-rear, low-stress interconnects, foil lamination, frameless Module yield: 98% Cell efficiency in the module: 16.7%
Technology risk	Medium
Industrial implementation	2009

Table III. Description and main parameters of roadmap scenario MultistaR (modified Multistar)

Overall technology name	MultistaR (modified version of Multistar)
Feedstock	Solar grade polysilicon at 20 €/kg
Crystallization	Ingot casting Ingot yield: 95%
Wafering	Wafer thickness: 120 µm Kerf loss: 140 µm Wafer yield: 90%
Cell processing	Metallised-Wrap-Through design, passivated rear side Cell yield: 96% Cell efficiency: 17%
Module assembly	All-rear, low-stress interconnects, foil lamination, frameless Module yield: 98% Cell efficiency in the module: 16.9%
Technology risk	Medium
Industrial implementation	2010

Table V. Description and main parameters of roadmap scenario SuperslicE (modified Superslice)

Overall technology name	SuperslicE (modified version of Superslice)
Feedstock	Near semiconductor grade polysilicon at 30 €/kg
Crystallization	Cz monocrystalline Ingot yield: 95%
Wafering	Wafer thickness: 120 µm Kerf loss: 140 µm Wafer yield 92%
Cell processing	Emitter-Wrap-Through design Cell yield: 95% Cell efficiency: 18.5%
Module assembly	All-rear low stress interconnects, conductive pattern integrated at the back sheet, foil lamination, frameless Cell efficiency in the module: 18.5%
Technology risk	High
Industrial implementation	2012

having a medium risk profile for industrialisation on the short term. There is also a modified version of Superslice (Table V), based on an Emitter Wrap-Through (EWT) design¹⁵ which allows for all-rear interconnection, and is categorised as having medium-

Table IV. Description and main parameters of roadmap scenario Superslice

Overall technology name	Superslice
Feedstock	Near semiconductor grade polysilicon at 30 €/kg
Crystallization	Cz monocrystalline Ingot yield: 95%
Wafering	Wafer thickness: 120 µm Kerf loss: 140 µm Wafer yield: 92%
Cell processing	Rear side passivated with dielectric stack, laser fired local rear contacts Cell yield: 96% Cell efficiency: 18.5%
Module assembly	Front-to-rear, low-stress interconnects, foil lamination, frameless Module yield: 98% Cell efficiency in the module: 18.2%
Technology risk	Medium
Industrial implementation	2010

to-high technology risk: it needs a few more years of research and especially development to be ready for industrial implementation with similar production performance as that of more conventional technologies. Ribbonchamp (Table VI) is an advanced silicon ribbon,^{16,17} based module with an all-rear contacting scheme, whose technology risk is also medium-to-high, as high efficiencies on very thin substrates have to be achieved with relatively low quality material. Also this technology needs a few more years of R&D to become ready for industrial use. Finally, Epi.C (Table VII) implements a wafer-equivalent based module^{18–20} for which a sufficiently high throughput in Si film deposition and a high efficiency should be accomplished, so that it is classified as having a high technology risk profile, with a higher time-to-industry than the previous technology options.

It is noted that the use of all-rear interconnection schemes (in three of the six technologies) is consistent with the need for high efficiencies and considered attractive or even necessary for high-yield module manufacturing using very thin cells.

It should also be taken into account that because the generation cost of solar electricity is determined by the system price (i.e. the sum of the module price and Balance-of-System-price), the optimum solar module is not necessarily the cheapest module (in €/Wp).

Table VI. Description and main parameters of roadmap scenario Ribbonchamp

Overall technology name	Ribbonchamp
Feedstock	Solar grade polysilicon at 20 €/kg
Crystallization	Ribbon technology
Wafering	Wafer thickness: 120 µm Wafer yield: 93%
Cell processing	Metallised-Wrap-Through design, passivated rear side Cell yield: 96% Cell efficiency: 16%
Module assembly	All-rear interconnects, integrated conductive pattern, foil lamination, frameless Module yield: 98% Cell efficiency in the module: 16%
Technology risk	Medium-high
Industrial implementation	2012

Table VII. Description and main parameters of roadmap scenario Epi.C

Overall technology name	Epi.C
Feedstock	Upgraded metallurgical (UMG) silicon at 4 €/kg
Crystallization	Ingot casting of the UMG substrate Ingot yield: 95%
Wafering	UMG wafer thickness: 120 µm Kerf loss: 140 µm Wafer yield: 95%
Epitaxy	In situ pn epitaxy (≈20 µm Si film) by Chemical Vapor Deposition Yield of the epitaxial growth: 95%
Cell processing	Front and rear screen-printed electrodes, internal optical reflector Cell yield: 96% Cell efficiency: 16%
Module assembly	Front-to-rear, low-stress interconnects, foil lamination, frameless Module yield: 98% Cell efficiency in the module: 15.8%
Technology risk	High
Industrial implementation	2015

Modules with a higher efficiency and somewhat higher price may lead to a lower turn-key system price because of lower area-related Balance-of-System costs. Although this issue is beyond the analysis being reported, it is an additional argument supporting the interest in defining different routes for crystalline silicon PV technology.

ESTIMATE OF SAVINGS DUE TO SCALING TO THE GWp RANGE

As already explained, baseline figures refer to a 30–50 MWp/a factory, typical size of PV plants in 2005–2006. A cost study was performed under the APAS^c programme of the European Commission in the late 1990s, evaluating the feasibility of a 500 MWp crystalline silicon module manufacture plant and the potential cost savings.^{21,22} That size was out of reach ten years ago, but due to the growth of the PV industry, 500 MWp–1 GWp plants will surely be a reality in the short to medium term, making relevant the analysis of additional cost savings in the roadmap scenarios of Proposal of Alternatives: The CrystalClear Roadmap Scenarios Section due to large scale production.

An analysis of cost reductions in thin-film photovoltaics due to very large scale integrated manufacturing has been performed recently by Hewlett Packard.²³ Although these findings cannot be directly applied to crystalline silicon photovoltaics due to differences in technology, some of the assumptions can be adapted to our case. In the aforementioned study,²³ the total cost reduction for thin-film photovoltaics because economies of scale is more than 70%, mainly because of the reduction of complexity and cost of installation, and the reduction of module manufacturing cost. We have assumed quite modest economies of scale for wafer-based photovoltaics compared to thin-film photovoltaics (roughly a 30% reduction), since the installation and module manufacturing are more complex for wafer-based technologies. Our calculations are therefore considered to give an upper limit of costs for very large scale manufacturing.

This is complemented by input from the industrial partners in CrystalClear, who have shared their estimates through a questionnaire collecting their approaches and figures associated to expansion to the

^cAPAS stands for Actions de Préparation, d'Accompagnement et de Suivi, it was a programme funded by the European Commission in the 4th Framework Programme focused on studies and analyses.

Table VIII. Reduction in % from the baseline figures of CrystalClear cost model due to large scale production

	Ingot	Wafer	Cell	Module
Equipment	−20%/−30%	−20%/−30%	−20%/−30%	−20%/−30%
Labour	−30%/−40%	−30%/−40%	−30%/−40%	−30%/−40%
Materials and consumables	Crucible, −30%/−40% Rest, −10%/−20%	−10%/−20%	Pastes, −30%/−40% Rest, −10%/−20%	−10%/−20%
Yield	+1%/+2% (abs)	+0.5%/+1.5% (abs)	+1%/+2% (abs)	+0.5%/+1.5% (abs)
Fixed costs	−40%/−50%	−40%/−50%	−40%/−50%	−40%/−50%

A range of values is given to accommodate the uncertainties in the estimation of cost reductions at these volume production levels.

GWp scale. The following considerations have been made to support in the quantification of cost savings:

- The 1 GWp factory will comprise the whole value chain from ingot production to module manufacturing, while silicon feedstock is assumed to be produced elsewhere. This approach will have benefits from reduced handling, shared infrastructure and improved quality control.
- Following the arguments of reference,²³ using a large number of systems similar to the ones used in the fabrication lines of today results in cost reduction. Most of the cost is the engineering to design and develop the process for the system, and once the system is working well the cost of replicating the system is much lower.
- Reductions in labour due to further automation.
- Due to the volume considered, some materials and consumables may be produced on site, reducing substantially their cost by eliminating distributors, wholesalers, retailers and manufacturers with their transportation, handling and marketing costs, and their profit margins. For example, the analysis of reference²³ argues that building a dedicated on-line glass production plant can make cost go down to 20% of current values. We propose to apply a similar philosophy to include subplants for crucible production and for screen printing pastes, although with a smaller cost reduction.
- The prices of the rest of the materials and consumables, not produced on-site, decrease when enlarging the size of the plant, and therefore the size of purchases.
- Yield increase due to reduction in transportation and handling and improvement in equipment.
- Regarding fixed costs, some of them will increase with increased volume production (like those related to footprint, sales department, for example), and others (those related to administrative services,

R&D department, for instance) will not change significantly as compared to the 30 MWp plant, so that we foresee an important cost reduction in relative terms (per Wp).

The estimated reduction for the different process steps and categories is shown in Table VIII, expressed as a percentage of the baseline figures for current volume productions of 30–50 MWp/a. A range of values is given to accommodate the uncertainties in the estimations, giving two extreme scenarios: a more ‘pessimistic’ one with the lowest estimated cost reductions, and a more ‘optimistic’ one with the largest potential cost savings.

Note that potential cost reductions in Si feedstock are not included, due to the fact that no industrial producer is involved in CrystalClear. In that sense, our cost results could be further reduced, as it is expected that the profound changes that the silicon feedstock market is experiencing, with a big expansion of production capacity from polysilicon traditional producers, the entry of a number of new comers and the development of alternative purification routes will result in significant cost savings.²⁴

RESULTS

The cost modelling of each technology has been performed by describing it in terms of the impact of technological improvements, with respect to the Basepower technology, in the cost structure.

Since the information provided by the research groups and their partners is based on laboratory experience and current insights it contains inherent uncertainties. In other words, commercial manufacturing may turn out to be (or may have to be) different from what is expected. Also the costs related to the use of new materials may be different than currently

Table IX. Cost breakdown of the CC scenarios at current volume production levels

€/Wp	Basepower	Multistar	MultistaR	Superslice	SuperslicE	Ribbonchamp	Epi.C
Feedstock	0.27	0.07	0.07	0.10	0.10	0.04	0.01 + 0.13
Ingot growth	0.20	0.10	0.10	0.15	0.15	—	0.09
Wafering	0.24	0.13	0.13	0.12	0.12	0.16	0.11
Cell process	0.58	0.48	0.60	0.51	0.58	0.61	0.44
Module	0.84	0.64	0.64	0.60	0.65	0.68	0.66
Total €/Wp	2.13	1.41	1.51	1.46	1.60	1.48	1.45
g/W	9.1	4.8	4.7	4.3	4.3	2.2	—

For the Epi.C scenario, epitaxial growth cost is included in feedstock cost. The figure of merit g/W has not been included in this case due to the difficulty of its definition for this technology. Note that all numbers are subject to change in a continuous process of updating, taking into account new insights and information as well as new research results.

Table X. Cost breakdown of the CC scenarios at large volume production levels (500 MWp–1 GWp/a)

€/Wp	Basepower		Multistar		MultistaR		Superslice		SuperslicE		Ribbonchamp		Epi.C	
Feedstock	0.27		0.07		0.07		0.10		0.10		0.04		0.01 + 0.13	
Ingot growth	0.14	0.12	0.07	0.06	0.07	0.06	0.11	0.09	0.11	0.09	—		0.06	0.05
Wafering	0.20	0.18	0.11	0.10	0.11	0.10	0.10	0.09	0.10	0.09	0.11	0.10	0.09	0.09
Cell process	0.41	0.35	0.34	0.29	0.42	0.35	0.37	0.31	0.42	0.35	0.43	0.37	0.31	0.26
Module	0.67	0.59	0.52	0.45	0.52	0.45	0.48	0.41	0.53	0.47	0.54	0.47	0.53	0.46
Total €/Wp	1.70	1.51	1.10	0.96	1.17	1.02	1.14	1.00	1.25	1.10	1.13	0.98	1.14	1.00
g/W	8.8	8.5	4.6	4.5	4.6	4.4	4.2	4.0	4.2	4.0	2.1	1.7	—	—

A range of values is given to accommodate the uncertainties in the estimation of cost reductions at these volume production levels. Note that all numbers are subject to change in a continuous process of updating, taking into account new insights and information as well as new research results.

foreseen. In general, we have used conservative estimates in all cases where clear uncertainties exist, meaning that our cost calculations give upper values. Therefore the results presented in this paper should be regarded as indicative only.

For each of the technology options, we present the breakdown of costs in the following tables, considering only technology improvements at the current volume production of 30–50 MWp/a (Table IX), and in the case of very large scale production (Table X).

It can be seen that costs can be reduced by 28–35% just by technology improvements. The 1 €/Wp goal is within reach provided these technology improvements are accompanied by savings due to large scale production.

CONCLUSIONS

Direct manufacturing costs for crystalline silicon PV modules have been calculated for the whole value chain, regarding the equipment, labour, material, yield losses and fixed cost contributions. Data provided by PV manufacturing companies involved in the Euro-

pean CrystalClear Integrated Project have shown costs to be in the range of 2.0–2.3 €/Wp by the end of 2005, for a 30–50 MWp/a level production.

Some scenarios have been described, which can serve as guidelines of the technological goals needed to achieve substantial cost reduction. They refer to the different crystalline silicon technology families (cast multicrystalline silicon, Cz single crystal silicon, ribbon silicon and thin-film silicon wafer equivalents), and have been defined to cover a range of potentials for cost reduction and corresponding development risk profiles.

The figures show that by the combined effects of technology development and economies of scale the direct manufacturing costs of wafer-based crystalline silicon PV modules can be brought down into the range of 0.9–1.3 €/Wp, depending on the technology considered. By comparing the total cost figures for Basepower (the 2005 reference technology) with the other technologies it becomes clear that the reduction obtained by technology development is roughly 0.5 €/Wp, while economies of scale add another 0.5 €/Wp. Although we have separated the effects of technology develop-

ment and economies of scale in the cost calculations, they are actually quite closed interlinked. The reason for this is that many of the manufacturing processes and design concepts used for the new technologies have been especially selected to enable or facilitate high-throughput (large scale) production at high yield.

It is emphasised that the lower end of the 0.9–1.3 €/Wp range corresponds to medium to high risk technologies. The feasibility of these technologies for large-scale production needs to be demonstrated. Particular challenges are to achieve a high overall process yield (from wafer manufacturing to module assembly) for very thin wafers, and to obtain the efficiency levels indicated in a production environment. On the other hand, the economies of scale we have assumed for very large scale manufacturing are rather modest. CrystalClear partners are therefore confident that the cost target of 1 €/Wp for modules can be reached with crystalline silicon technology.

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