LPCVD polysilicon passivating contacts

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Abstract

This paper presents progress by ECN and Tempress in developing and integrating processing of polysilicon passivating contacts aimed at use for low-cost industrial cell production. The polysilicon ("poly") is deposited by low pressure chemical vapour deposition (LPCVD), and we present results with in-situ as well as ex-situ doping processes. We demonstrate synergy and compatibility with industrial cell processing; for example applying hydrogenation from silicon nitride coating layers, and metallization by screen printed fire-through paste. We analyze the relation between surface recombination current prefactor J_o and the processing of the polysilicon. For n-type poly ("n-poly") we obtain J_o down to ~0.8 fA/cm2 and ~3 fA/cm2 on planar and textured surface, respectively; for p-poly J_o down to ~6 fA/cm2 on planar surface (results on textured surface are pending). We have fabricated 6 inch screen printed bifacial n-type cells with a diffused boron emitter and an n-poly back contact (called PERPoly cell), with an efficiency of 20.9%, representing an industrially relevant application of the polysilicon technology. In the presentation we will also consider other variations of cSi cells with poly passivating contacts.

Introduction

Good contacts to solar cells should extract one type of charge carrier with low series resistance while avoiding recombination of the other type of charge carrier. This is usually accomplished by enhancing carrier density of one type near the surface and depleting the other type. Still, contacting a diffused junction with metal results in an imperfect contact with significant recombination: the recombination current prefactor J_o is at least hundreds of fA/cm^2. Alternatives for diffused junctions directly contacted by metal, have been described and investigated for many years. Reviews of the need and potential benefit of passivating contacts, and several approaches, were given e.g. by Green in 1995 [1] and Swanson in 2005 [2].

The combination of a thin oxide and doped polycrystalline silicon (polysilicon or poly) to obtain low recombination junctions was demonstrated in the 1980s to be a viable candidate for creating passivating contacts to cSi solar cells [3]. In recent years variations and innovations on this technology have seen intense development and rapid progress to demonstrating ~25% cell efficiency [4]. This paper will describe our progress and cell results with such poly passivating contacts. Specifically, the poly is deposited by Low Pressure Chemical Vapour Deposition (LPCVD).

While conventional high performance contacts based on local diffusion with metal point contacts can also yield low recombination at cell level by reducing the contact area, these suffer from spreading resistance as a negative side-effect. This is a fundamental disadvantage compared to poly passivating contacts. In addition, the J_o achieved by poly passivating contacts is extremely low and hard to beat by alternative processes even in the absence of metal contacts.

A simple modeling approach to the polysilicon passivating contact

Recently, detailed modeling efforts on polysilicon passivating contacts have been presented [5]. It may be possible to evaluate recombination properties quite generally also in PC1D, as follows. We assume a layer with low carrier transmission, e.g. a tunnel oxide with low transmission factor T, at the interface between the wafer and the poly. We surmise that the effective recombination velocity at the interface then becomes $S_i + T \cdot S_s$. If T is small enough, a high S_s (like the thermal velocity, ~10^7 cm/s in

case of a metal contact) will not significantly increase the recombination at the interface. Replacing the tunnel oxide by a layer of small mobility, a thicker oxide with pinholes, etc., will likely give a similar effect. PC1D allows stacking of semiconductor layers with defined interface recombination velocities, but not definition of a small transmission or small mobility at the interface. We therefore substitute the effect of the small transmission of minority carriers into the polysilicon by a zero S_s, which should be roughly equivalent in causing recombination in or on the polysilicon (apart from Auger recombination) to be negligible. Alternative to PC1D, perhaps an analytical result for this simplified model is also possible.
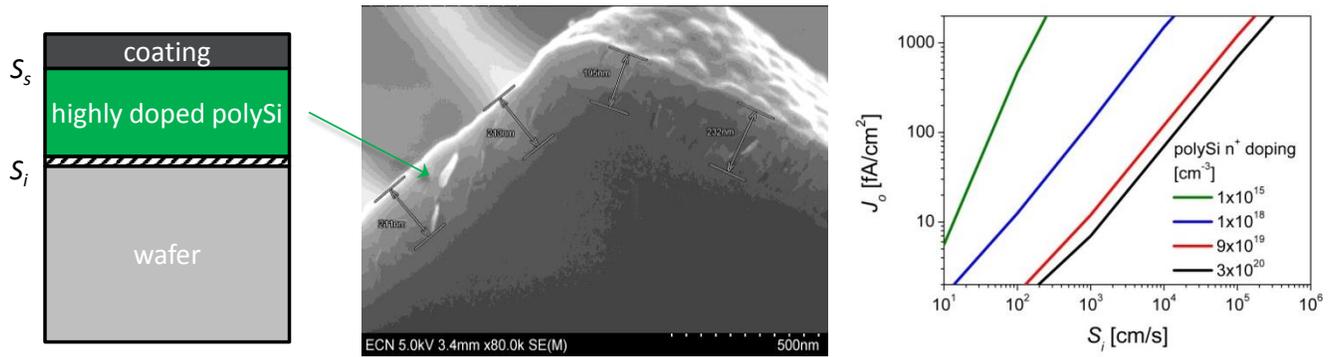

Fig. 1 . Left: Schematic structure of a polysilicon passivating contact. A stack of a thin dielectric (hashed) and doped polysilicon is grown on a silicon wafer. The polysilicon may be coated with metal (for contacting) or dielectric (for antireflection coating, or hydrogenation). The interface recombination velocity S_i is low. The surface recombination velocity S_s does not affect the contact passivating properties and may be high. Middle: a SEM image of one of our polysilicon stacks on a textured wafer. Right: J_o modeled in PC1D as a function of phosphorus dopant concentration in the polysilicon and S_i.

Fig. 1 shows the outcome of such PC1D modeling. The dependence on doping level is illustrative and we will at least qualitatively observe this in experimental results later. The dependence on S_i shows that while 10^3 to 10^4 cm/s already allow good J_o, the recently obtained extremely low J_o (see also later in this paper), suggest that S_i can be of order 10-100 cm/s.

It seems logical (and PC1D results confirm this) that for passivation quality, there is no fundamental need for a polysilicon thickness much greater than the Debye length (only a few nm in highly doped silicon).

This modeling approach does not immediately allow to evaluate series resistance for majority carrier extraction. Probably further assumptions about the transport mechanism at the interface will be necessary. E.g., when assuming a specific (e.g., SiO_2) tunnel barrier at the interface, T can be related to passivation (as described above) as well as to majority carrier transport. Interestingly, in our cells, even for a thin oxide (nominally 13 Å thick) we measured contact resistances by TLM which appear to be inconsistent with a tunneling model for carrier transport. For simultaneously processed p-type poly (p-poly) contacts and overcompensated n-poly contacts, with identical oxide, polysilicon deposition, and thermal budget, we found a contact resistivity ρ_{co} of polysilicon to wafer of about 30 m$\Omega \cdot$cm^2 for n-poly, and 5 m$\Omega \cdot$cm^2 for p-poly. If tunneling dominated, a higher ρ_{co} should have been observed for p- poly than for n-poly.

Industrial LPCVD of polysilicon passivating contacts

We employ polysilicon layers grown in a high-throughput LPCVD furnace. An LPCVD process has the benefit of creating very conformal and pinhole-free layers. This ensures that the underlying interfacial oxide is protected against subsequent doping steps and chemical treatments. For mass production, batches of up to a few hundred wafers can be processed, with excellent process uniformity. The thin oxide is produced by thermal oxidation (Th.Ox) or wet chemical oxidation (NAOS: Nitric Acid Oxidation of Silicon). A reliable absolute thickness measurement is not well feasible. In our work the thickness was

estimated from spectroscopic ellipsometry on mirror polished wafers, with resulting typical values of 13 to 15 Å correlating to good performance. A slightly higher thickness can result in noticeably reduced FF, while a slightly lower thickness can result in increased dopant diffusion into the wafer.

The LPCVD layer can be intrinsic, subsequently doped by $POCl_3$ or BBr_3 diffusion, or by implant and anneal. $POCl_3$ or phosphorus implant doping result in fast deposition, tunable doping level, low diffusion into the wafer, and excellent J_o. We have also investigated in-situ p-type doped polysilicon for cell processing. In-situ phosphorus doping during LPCVD is reported to reduce deposition speed [6]. In view of the use of fire-through metallization, we investigated, so far, relatively thick layers of polysilicon.

Dependence of J_o on doping level and hydrogenation

We have investigated varying thicknesses of polysilicon, doped with varying implantation doses; dopant diffusion recipes; and in-situ doping recipes. In general there is a qualitative correspondence between dopant concentration and J_o (higher dopant concentration generally results in better J_o, cf. Fig. 1). J_o is significantly increased if there is too strong "leakage" of dopants from the poly into the wafer, which may occur at high diffusion temperatures or too thin oxide or for other process reasons ([7]).

Apart from the doping level, another important process that influences J_o is hydrogenation. We have found that hydrogenation by PECVD deposition of SiNx on samples is very effective. We have not studied *what* is hydrogenated; probably defects at the interface are passivated resulting in a reduction of S_i. In the following figures we present J_o of lifetime test samples in relation to doping profiles from ECV (electrochemical capacitance-voltage profiling), and SiNx coating and firing steps. The ECV curves have not been calibrated by SIMS, but the thicknesses have been checked against SEM cross sections, which are mostly roughly consistent.
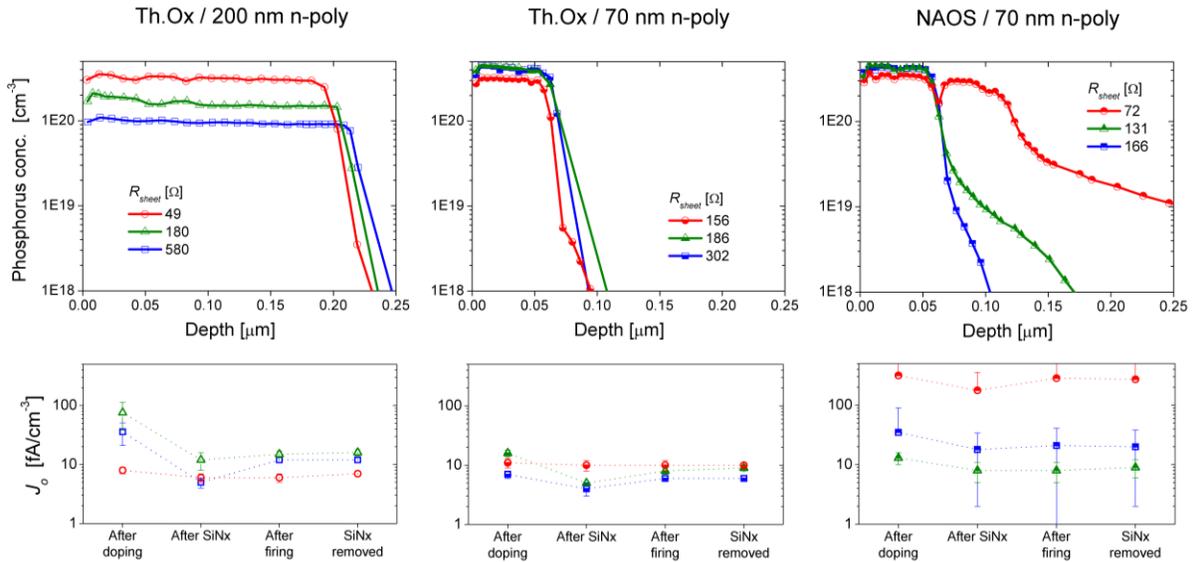

Fig. 2. Top: Doping profiles of several n-poly stacks with the corresponding R_{sheet} values, on polished Cz wafers. Three different $POCl_3$ diffusion temperatures (the same for all stacks) were used for doping, with high to low temperature corresponding to low to high R_{sheet}. Bottom: Evolution of surface passivation quality, in a sequence of process steps. J_o was derived from lifetime measurements with the Sinton WCT-120 tool.

Fig. 2 shows results of n-poly layers doped by $POCl_3$ diffusion at three different temperatures, between 830 and 870 °C. It is striking that the thin oxide can be an excellent diffusion barrier. However, a high diffusion temperature together with the use of NAOS oxide resulted in significant diffusion into the wafer. Judged from R_{sheet} and doping profile, the majority carrier mobility is at best about 2-3 times lower than in monocrystalline silicon, and can be somewhat enhanced by hydrogenation. There is a stronger

dependence of sheet resistance on the diffusion temperature than can be explained from dopant concentration, indicating that the mobility depends on the diffusion temperature, perhaps related to continued crystallization of the polysilicon during the diffusion. After the lowest diffusion temperatures, the apparent mobility is much lower ($\sim$0.1$\times$) than in monocrystalline silicon.

Fig. 2 also presents the evolution of J_o, after doping, with plasma-enhanced chemical vapor deposition (PECVD) SiNx:H deposition, firing, and SiNx:H removal. In the 200 nm layers before hydrogenation, J_o depends on doping level. For the 70 nm layers with Th.Ox, doping level and J_o are in the same range as for the heaviest doped 200 nm layer. For the 70 nm polysilicon / NAOS stacks, the J_o is probably dominated by effects of the phosphorus leakage through the oxide. For the 70 nm / NAOS stack diffused at highest temperature, J_o is very high, which cannot be explained by Auger recombination alone so there probably is a significantly increased interface defect density.

J_o is reduced by PECVD SiNx:H deposition, in particular for the n-poly layers with low doping level (200 nm thickness). The hydrogenation did not completely equilibrate the J_o values. Firing of the SiNx:H layer did not significantly change J_o. Removal of the SiNx layer by wet chemical etching did not change J_o, as expected since this should not change the hydrogen passivation of defects at the SiOx/wafer interface, protected by the polysilicon top layer.
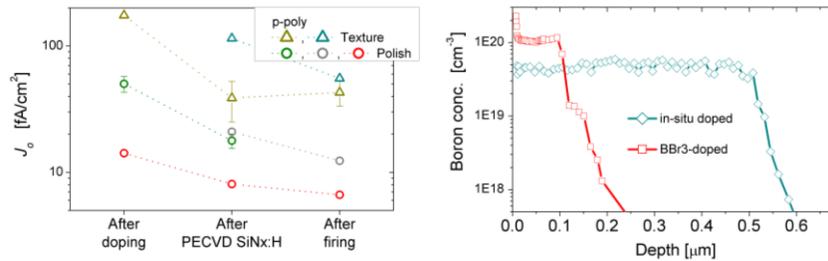

Fig. 3. Development of average J_o with SiNx deposition and firing, and ECV doping profiles for p-poly passivating layers. Data from several runs. Blue-green: in-situ doped. Red: BBr$_3$-diffused.

Fig. 3 shows results for p-poly. Tempress has developed in-situ boron doped polysilicon growth in an industrial LPCVD furnace. Optimization of hardware and growth process results in a uniform doped polysilicon. A mild anneal temperature can be used to activate the dopant, avoiding damage to the underlying interfacial oxide. Nevertheless, good doping with little dopant leakage into the wafer can also be obtained with BBr$_3$ diffusion. So far we have obtained higher doping concentrations with BBr$_3$ diffusion, and, presumably, therefore better J_o.

The J_o of p-poly seems to be more dependent on interface properties than n-poly, and hydrogenation can have a large beneficial impact in particular if interface properties are imperfect (i.e., high J_o as-doped). A J_o of $\sim$6 fA/cm^2 was obtained on a polished surface with 1×10^{20} cm^{-3} doping level after hydrogenation by PECVD SiNx:H. The lower-doped p-poly on textured surface shows significantly higher J_o; results with higher doping level are pending.

Interestingly, these p-poly layers can be compensated to n-type by either implant or POCl$_3$ diffusion, resulting in J_o and iV_{oc} as good as for non-compensated n-poly ([8]). In this way, in preliminary tests we have obtained textured asymmetric samples (compensated n-poly on one side, p-poly on the other side), with implied V_{oc} of 701 mV. However, a polysilicon layer on the front will give rise to optical losses (carriers generated in the polysilicon do not noticeably contribute to J_{sc}).

TABLE 1. Best passivation characteristics of polysilicon passivating contacts on PV-grade Czochralski lifetime test samples. Phosphorus doping level ~4×10^{20} cm^{-3}; boron doping level ~1×10^{20} cm^{-3}

Wafer surface = polished (saw damage removed)	iV_{oc} (mV)	$J_{oe\,n\text{-}poly}$ (fA/cm^2)
n-type, after doping	~732	~1.6
n-type after SiNx	~744	~0.8
n-type after SiNx and firing	~741	~1.7
p-type, after doping	~704	~15
p-type after SiNx	~726	~6.5
p-type, after SiNx and firing	~728	~6
Wafer surface = textured		
n-type, after SiNx and firing	~736	~3.1

Application in industrial bifacial n-type cells

Various cSi cell design variations are possible, using the polysilicon for one or two of the contact polarities. A uniform polysilicon layer can be used at the back of a cell as emitter or base contact. We have focused on processing an n-type cell with front diffused boron emitter and an n-poly back contact (Fig. 4), using only industrial tools. In recent years the cell with n-poly back contact has been investigated by several groups [9]. Our development discerns itself by employing a bifacial metallization. Also we present full size 6 inch cells employing LPCVD for the polysilicon deposition. With an eye on the application in industrial cell processing, we used:
- hydrogenation from PECVD SiNx:H coating layers;
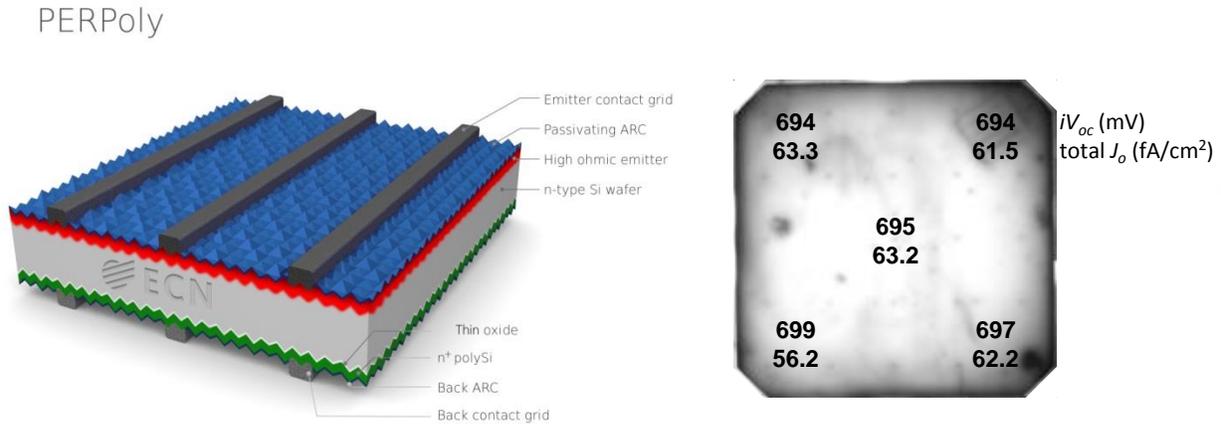- contacting by firing-through screen-printed metallization.

Fig. 4. Schematic drawing of the bifacial n-type solar cell with n-poly back contact. Right: PL of the solar cell before metallization, with iV_{oc} and J_o obtained on 5 locations.

Hydrogenation of polysilicon contacts is often performed by forming gas anneal, but hydrogenation from SiNx:H removes the necessity for this step. Contacting by screen-printed metallization has the potential benefit for industrial application as basically a drop-in replacement for a diffused back surface field. With a screen printed metallization grid an additional benefit is that a bifacial cell is possible. The reduction of bifaciality compared to standard bifacial n-PERT cells is limited. We are using a designation for this general type of cell design with polysilicon back contact, in line with the PERT, PERC, and PERL acronyms, as PERPoly (Passivated Emitter and Rear Polysilicon).

Fig. 5 shows the evolution of average Jo of n-poly, on a textured wafer surface. The J_o of the n-poly with metal fire-through contact grid was determined by QSSPC which is an approach that sometimes, but

not generally, seems to work, and results have to be treated with caution. We are moving to cell-level test structures for determination of contact J_o on poly in addition to these QSSPC measurements.

After doping, the J_o for textured surfaces is larger than for polished surfaces by more than the surface area ratio, but after PECVD SiNx:H deposition, the J_o are comparable. After fire-through of a metal contact grid some degradation of J_o occurred, depending on firing parameters and paste.
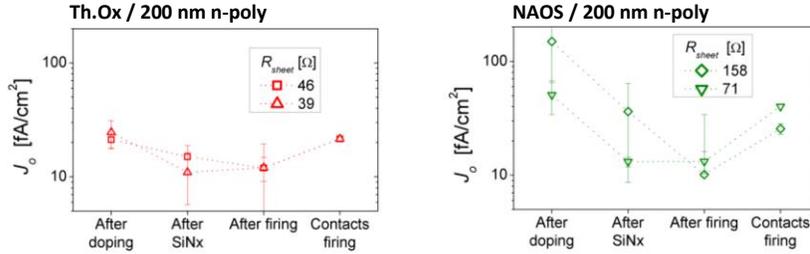

Fig. 5. Evolution of J_o through steps relevant for cell production, for textured wafers with 200 nm n-poly, in several test runs. The highest diffusion temperature of Fig. 2 was used for Th.Ox., the middle temperature for NAOS..

Our cell process is expected to be feasible with a comparable number of process tools as used for PERC cells, although presently we still use some more elaborate chemistry. A BBr_3-diffused industrial type uniform emitter with a sheet resistance of 70 or 80 Ω/sq was employed on the front side, 140-200 nm thick polysilicon coated with SiNx:H on the back side. The implied V_{oc} before metallization is approximately 700 mV (Fig 4). In recent tests using higher emitter sheet resistance, the iV_{oc} has been increased to slightly higher than 700 mV, and the total J_o before metallization reduced to less than 45 fA/cm^2.

TABLE 2. PERPoly cell results as well as best J_o, iV_{oc} and bulk lifetime on half-fabricates.

	J_{oe} n-poly w/o contacts[*]	J_o F+B half-fab. w/o contacts[*]	J_o F+B cell w/ contacts[*#]	Bulk lifetime	iV_{oc} half-fab. w/o contacts[*]	iV_{oc} cell w/ contacts[*#]	V_{oc}	J_{sc}	FF	pFF	η
	(fA/cm^2)	(fA/cm^2)	(fA/cm^2)	(ms)	(mV)	(mV)	(mV)	(mA/cm^2)	(%)	(%)	(%)
70 Ω emitter, 200 nm n-poly	7.7	56.2	~98	6.68	699	~680	675	38.8	79.1	82.8	20.72
rear response							669	31.3	79.6		16.66
group ave. (6 cells)							674	38.8	79.1		20.67
80 Ω emitter, 200 nm n-poly							673	38.9	79.9		20.9

F=front, B=back, [*]best spot, [#]photoconductance measurements with metal grid

Table 2 presents results of the PERPoly cells. With 70 Ω emitter, we obtained a best cell efficiency of 20.72% [10] with a V_{oc} of 675 mV, which is to be compared to a V_{oc} of our comparable nPERT cells with diffused BSF of approx. 665 mV. Recently, we have achieved a cell efficiency of 20.9% with 80 Ω emitter and Th.Ox / 200 nm n-poly (spectral mismatch correction pending).

Cell losses and outlook for improvements

V_{oc} is mostly limited due to the diffused boron emitter and its contact at the front side. The bulk lifetime of the cell half-fabs before metallization is about ~3 ms, the total J_o close to 60 fA/cm^2, together resulting in an average iV_{oc} of ~693 mV. After contact firing the cell V_{oc} decreases to 675 mV. After applying the fire-through grid, the J_o of the n-poly back contact was estimated based on Fig. 5 to be ~20 fA/cm^2, and the front contact grid is known to contribute about 60 fA/cm^2, due to a specific J_o of 2500 fA/cm^2 for the fire-through metallization. This results in the following break-down of J_o (Table 3).

TABLE 3. Estimated distribution of recombination losses in the cells of Table 2 in fA/cm^2.

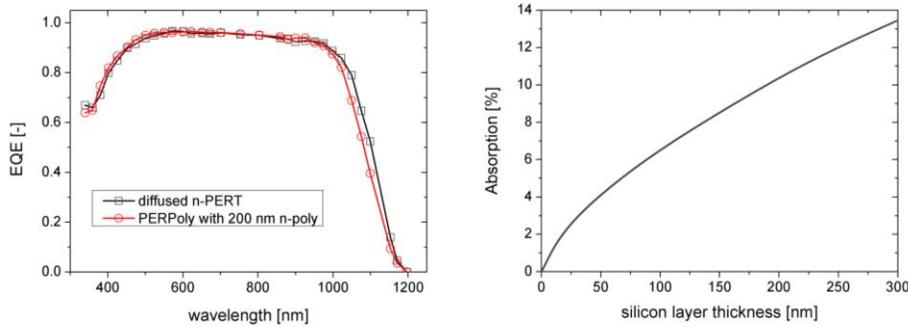| Back n-poly	Back metal grid	Emitter	Emitter contact	Bulk	Total
7	13	50	60	8	138

Fig. 6. Left: EQE of PERPoly cell compared to n-PERT cell, showing in particular the difference due to free carrier absorption in the range from 1000 to 1200 nm. Right: Absorption of AM1.5 spectrum in thin crystalline silicon as approximation for the loss in a polysilicon layer when used at the light-incident side of a solar cell.

In addition to the usual reflection losses, some J_{sc} loss is due to free carrier absorption (FCA), and absorption with carrier generation in the polysilicon. Since the n-poly back contact is quite heavily doped to a low sheet resistance, FCA is significant compared to bifacial n-PERT cells with a diffused BSF, as visible in the EQE of Fig. 6. The total FCA in the n-poly was evaluated by ray tracing analysis to be approx. 0.9 mA/cm^2 for 200 nm thickness and 3×10^{20} cm^{-3} doping level. This FCA can be significantly reduced by decreasing the polysilicon thickness or doping level, if the contact metallization allows. However, due to the reduced carrier mobility in the polysilicon, the FCA in a bifacial PERPoly cell will probably always be somewhat higher than in a corresponding nPERT cell with diffused BSF.

Our PERPoly cells have about 80-85% bifacial performance. This is about 10% less than for equivalent n-PERT cells with diffused BSF. This extra 10% loss is in agreement with the estimated absorption of short wavelength photons in the polysilicon, approximated as the absorption of regular crystalline silicon, see Fig. 6.

The FF of the PERPoly cells is similar to typical FF for equivalent n-PERT cells with diffused BSF, and it seems there is no significant series resistance loss (not more than about 0.1 $\Omega \cdot$cm^2) in the poly/oxide/wafer junction. This is in agreement with our TLM measurements.

Achieving a cell efficiency of 22% will require, in particular, improvement of the front J_o. We expect the total J_o can be reduced to 50 fA/cm^2 by implementing a higher R_{sheet} emitter (25 fA/cm^2 or less should be possible even for an industrial type of boron emitter), and less penetrating fire-through pastes or a selective emitter. Depending on feasible contact area, a specific contact J_o below ~1000 fA/cm^2 will probably be required. Also, the parasitic absorption in polysilicon has to be reduced by making the layer thinner or less doped. Finally, the FF has to be improved which may involve further optimization of the thin interfacial oxide and doping process.

Conclusions

We presented studies of polysilicon passivating contacts, produced with an LPCVD-based process, and their application on the back side of a high-performance bifacial n-type solar cell with fire-through screen-printed metallization, processed on 6 inch Cz wafers. The cell design is called PERPoly (Passivated Emitter and Rear Polysilicon). A best efficiency of 20.9% (mismatch correction pending) was achieved together with an average cell V_{oc} of 674 mV. As an added benefit, the cells are bifacial with bifaciality factor >0.8. Excellent passivation has been obtained with n-poly both on polished and textured surfaces with recombination current densities J_o of <1 fA/cm^2 and ~3 fA/cm^2, respectively. p-poly demonstrated J_o of ~6 fA/cm^2 on polished surface, with results on texture for similarly high doping level pending. The effect of a fire-through contact grid on 200 nm n-poly contact was evaluated to be in the range of 10-20 fA/cm^2. These results show the high potential of this technology to augment current cell processes, with large performance headroom for the future.

Acknowledgements

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