N-TYPE POLYSILICON PASSIVATING CONTACTS FOR INDUSTRIAL BIFACIAL N-PERT CELLS

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ABSTRACT: We present a high-performance bifacial n-type solar cell with n^+ polysilicon (polySi) back side passivating contacts and fire-through screen-printed metallization, processed on 6" Cz wafers. The cells were manufactured with low-cost industrial process steps yielding a best efficiency of 20.7%, and an average V_{oc} of 674 mV. We analysed effects of variation of doping level, thickness, and oxide properties of the n-type polySi/SiO_x layers, as well as hydrogenation from a PECVD SiN_x:H coating, which led to recombination current densities down to ~2 fA/cm^2 and ~4 fA/cm^2 on planar and textured surface, respectively. The results are novel in four aspects: the cells are bifacial, they are full 6" size while employing LPCVD for the polySi deposition, the polySi passivating contact is metallized by fire-through screen printing paste, and hydrogenation is done by PECVD-deposited and fired SiN_x:H. Analysis shows that the wafer bulk lifetime in the cell is high and that the V_{oc} of the cell is limited by the J_o of the uniform diffused boron emitter and its contacts. Ways to improve the efficiency of the cell to > 22% are indicated.
Keywords: polysilicon, passivating contact, carrier selective contact, LPCVD, n-type solar cell, bifacial

1 INTRODUCTION

The combination of a thin oxide (SiO_x) and doped polysilicon (polySi) to obtain low recombination junctions, originating from early work on bipolar transistors [1], was demonstrated in the 1990s to be a viable candidate for creating passivating contacts to crystalline silicon (cSi) solar cells [2,3].

A key element in the passivating contact structure is the thin oxide layer which has a reasonably low interface recombination velocity, supported by a hydrogenation step (typical models estimate that a recombination velocity (S) of ~10^3-10^4 cm/s is sufficiently low [4, 4b]). This thin oxide layer serves also as a tuneable (e.g., by thickness) diffusion barrier, which is indispensable for keeping most of the dopant within the polySi layer thus avoiding creation of a typical diffused junction in the wafer. The doped polySi layer, due to the induced field effect, reduces minority carrier density at the interface with the wafer while providing good conductance for the majority carriers to the contacts applied on the polySi.

The combination of the interfacial thin oxide with doped polySi provides a low transmission of minority carriers assuring therefore a minimal recombination in polySi and at the metal contact. Together with the low level penetration of dopants in the wafer, this results in excellent passivation [4c, 4b]. The oxide/polySi stacks can be contacted by metal, which is in principle possible without increasing the recombination of minority carriers generated in the cSi wafer, although increase of recombination can in practice occur due to various effects [4d].

Recent progress on cells with such contacts, achieving conversion efficiencies above 25% on small area cells [4,5], and demonstrating in excess of 21% cell efficiency on 6" monofacial cells [6], merit the need to investigate industrialization of the concept.

The purpose of the work in the present paper is to understand practical optimization routes, using solely high volume production proven equipment, for the n-type polySi passivating contact as well as to demonstrate potential industrial cells with such a back contact. In this work we employ a polySi layer grown in a low pressure chemical vapor deposition (LPCVD) furnace which is subsequently doped by means of $POCl_3$ diffusion.

Specifically, optimization of the thin oxide properties, polySi thickness and phosphorous (Ph) doping level, hydrogenation from SiN_x:H, and contacting of the polySi are investigated. The evaluation of the feasibility of firing-through screen-printed metallization on polySi (without adding significant contact recombination) is included. The n-type polySi with screen printed contacts is integrated on the back of a cell with a boron emitter made by an industrial diffusion process, thus leading to a novel low-cost but high performance solar cell concept.

High efficiency solar cells made with LPCVD based polySi layers and screen printed fire-through contacts have several advantages, amongst others they can be realized by modest adaptation of conventional screen-print solar cell processes. LPCVD is a well-established high-throughput industrial process that can be easily implemented in state of the art solar cell manufacturing lines.

2 EXPERIMENTAL

2.1 LPCVD polySi layers

PolySi layers were produced in a high-throughput industrial LPCVD furnace and subsequently doped by means of $POCl_3$ diffusion [7]. An LPCVD process has the benefit of creating very conformal and pinhole-free layers. This ensures that the underlying interfacial oxide is protected against subsequent doping steps and chemical treatments. For mass production, batches of up to a few hundred wafers can be processed simultaneously with excellent process uniformity. The thin oxide was produced by thermal oxidation (called Th.Ox) or wet chemical oxidation (Nitric Acid Oxidation of Silicon, called NAOS). A reliable absolute thickness measurement is not well feasible, but the thickness was estimated from spectroscopic ellipsometry on mirror polished wafers to be 13 to 15 Å. The high repeatability and tuning of this thickness at the single Å level is possible as well as necessary and will be addressed in the near future.

The effect of variations of process parameters on the recombination parameter J_o (the dark saturation current) was characterized at lifetime level by photoconductance measurements (Sinton WCT-120 tool) and photoluminescence (PL), and related to the dopant profile

measured by ECV (electrochemical capacitance-voltage). The best process parameters in terms of resulting J_o were applied at cell level.

2.2 Investigation of polySi doping and passivation

Symmetrical lifetime samples were fabricated on 5 Ω·cm n-type 6" Czochralski (Cz) wafers. The thickness of chemically polished wafers was 150 µm and of textured wafers 175 µm. After the wet-chemical oxide or thermal oxide was grown on both sides, a 70 or 200 nm thick intrinsic polySi layer was deposited by LPCVD, followed by $POCl_3$ diffusions at 3 different temperatures ranging from 830°C to 870°C, resulting in polySi layers with different dopant concentrations and sheet resistances (R_{sheet}, measured using a Sherescan tool), as well as different phosphorous leakage through the thin oxide into the wafer (measured using ECV). The polysilicon thickness determined by ECV profiling compares well with scanning electron microscope (SEM) images. For textured surfaces, the polysilicon thickness is best determined from SEM images.

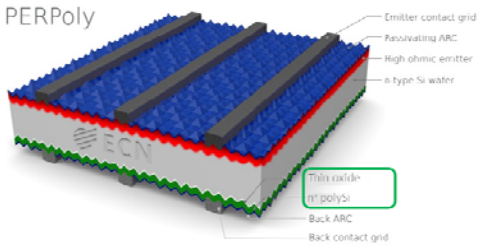

Figure 1: Schematic drawing of the bifacial n-type solar cell design of this paper, featuring n-polySi\SiO_x contacts, named PERPoly (Passivated Emitter and Rear Polysilicon)

2.3 Application in industrial bifacial n-type cells

239 cm^2 n-type solar cells were produced according to standard industrial process steps with the exception of replacing a diffused Back Surface Field (BSF) with n-type doped polySi/SiO_x contacts, as shown in Fig.1. Such device can be called PERPoly (Passivated Emitter and Rear Polysilicon). In the cell process tests we have so far only employed the 200 nm polySi thickness. The cell processes stay close to existing industrial n-type technology, by employing only PV process tools that are proven for low-cost high-throughput production.
n-type cells were produced on 6" Cz wafers of 5 Ohm·cm. An industrial type uniform diffused emitter with a sheet resistance of 70 Ohm/sq was employed on the front side. The emitter was passivated with Al_2O_3 deposited by ALD (Atomic Layer Deposition (Levitrack tool from Levitech)), coated with PECVD SiN_x:H. The back side polySi was also coated with SiN_x:H. The metal grid was screen-printed using fire-through pastes both to contact the B-emitter on front and polySi on back. The co-firing process was optimized and the settings are similar to the industrial standards.

3 RESULTS AND DISCUSSION

3.1 PolySi doping and passivation

Fig. 2. shows the resulting active phosphorus concentration profiles, measured with ECV on the chemically polished samples, for three different diffusion

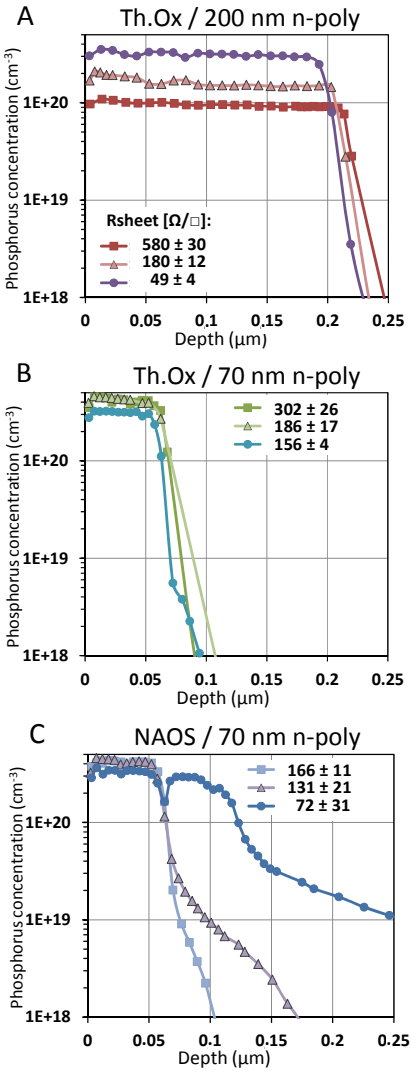

Figure 2: Phosphorus doping profiles investigated for the polySi/SiO_x/Cz-Si carrier selective structures with the corresponding R_{sheet} values, on polished wafers

runs. Increasing diffusion temperature (from 830 to 870°C) resulted in higher active phosphorus concentration within the polySi layer with an abrupt drop indicating the location of the Th.Ox, but with noticeable phosphorous-indiffusion especially in case of NAOS (we call this a 'leaky profile'). Fig. 2 also shows the corresponding R_{sheet} values. For the thickest (200 nm) polySi increasing the temperature of the diffusion resulted in an increased dopant concentration. However, for the thinner (70 nm) polySi similar concentrations were found for all diffusion processes applied, despite the varying temperature. This leads us to believe the doping level in the thick polySi layers is limited due to the amount of phosphorus available, e.g. in the phosphosilicate glass. Despite similar active dopant concentrations, the thin polySi layers still show a decrease in sheet resistance (from 302 to 156 Ω/sq) with increasing temperature. This indicates that higher diffusion temperatures are resulting in higher charge carrier mobilities, which is likely due to continued

crystallization of the polySi during the diffusion. We note that the ECV measurements on polysilicon may be subject to effects from the granular structure not observed in monocrystalline silicon, and the ECV measurements have not been compared with other measurements, e.g. SIMS.

Fig. 3 presents the evolution of the recombination parameter J_o (the dark saturation current) for the investigated n-polySi/SiO_x structures through various subsequent processing steps, again for chemically *polished* wafers. All J_o, iV_{oc} (implied open circuit voltage) and lifetime measurements presented here were obtained with the Sinton WCT-120 tester on symmetric lifetime samples.

Average J_o per side <10 fA/cm^2 was achieved already without any particular hydrogenation steps, i.e. right after doping. We attribute the higher initial J_o of the 200 nm thick high R_{sheet} layers at least partly to the lower doping level which increases sensitivity to the interfacial $D_{it,}$ which was also suggested in other study [8]. For the 70 nm layers with Th.Ox there is little variation of doping level, and therefore little variation of initial J_o. The doping level for all those layers is in the same range as the heaviest doped 200 nm layer. As expected from the Debye length of only a few nm in the polySi, no difference in J_o is observed for 70 and 200 nm polySi layer thickness. For the 70 nm thick layers on top of the NAOS oxide, the initial J_o (before hydrogenation) is probably dominated by effects of the phosphorus leakage through the thin oxide. A significant 'leaky diffusion profile' in the case of structures with the NAOS interfacial oxide and $POCl_3$ diffusion at highest temperature (72 Ω/sq) resulted in high J_o. This is partly due to a significant Auger recombination in the wafer near to the surface (we calculated about 70 fA/cm^2 for the ECV profile shown in Fig. 2) and the effect of the damaged oxide increasing the amount of interface defect states, which could result in at most about 275 fA/cm^2. Interestingly, the moderate 'leaky diffusion profiles' of NAOS/polySi with R_{sheet} of 131 and 166 Ω/sq showed still relatively low J_o values.

Improvements in J_o were observed after SiN_x:H deposition. PECVD (plasma enhanced chemical vapour deposition) SiN_x:H resulted in improved J_o in particular for the 200 nm n-poly layers with low doping level and R_{sheet} of 580 and 180 Ω/sq. We attribute this to hydrogenation of the SiO_x/wafer interface. However, the hydrogenation from SiN_x:H did not completely mask effects from variations in D_{it} or doping level. Firing of the SiN_x:H layer did not significantly change J_o. Removal of the SiN_x layer by wet chemical etching did not change J_o, as might be expected since this should not change the hydrogen passivation of defects at the SiO_x/wafer interface, protected by the polySi top layer. This indicates that the passivation of the outer surface of the polySi is irrelevant, validating the concept of the passivating contact.

In conclusion, it should be noted that low sheet resistances could be combined with excellent J_o for some of the investigated thin polySi layers. This allows us to use a partially contacted back (open grid on the back of the cell, resulting in a bifacial cell) which is a practically useful novelty in the field of polySi.

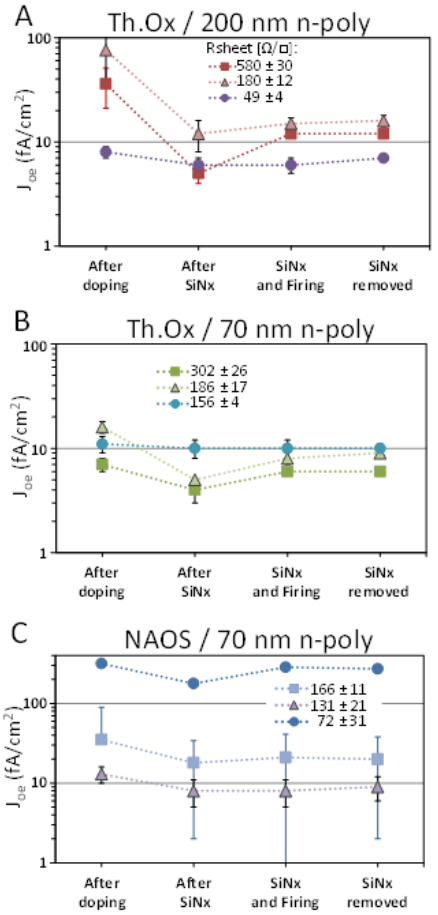

Figure 3: Evolution of surface passivation quality of studied polySi/SiO_x carrier selective structures on *polished* Cz-wafers in a sequence of process steps. All J_o values per side are average of up to 15 points on 3 wafers and error bars depict standard deviations

Table I: Best passivation characteristics obtained on *polished* wafers. Symmetric wafer structures with n-polySi/SiO_x on both sides. "Lifetime"= effective minority carrier recombination lifetime (@$\Delta n=10^{15}$ cm^{-3})

Cell type (polished, Th.Ox)	iV_{oc} (mV)	$J_{oe\ n\text{-}poly}$ (fA/cm^2)	*Lifetime* (ms)
After doping (200 nm, 49 Ω/sq)	~731	~3.4	~5.0
After SiN_x (70 nm, 186 Ω/sq)	~743	~2.2	~6.6
After SiN_x and Firing (200 nm, 49 Ω/sq)	~734	~5.2	~9.4
After SiN_x removed (200 nm, 49 Ω/sq)	~732	~3.0	~12.3

Table I shows a summary of the best passivation characteristics measured after these industrially relevant process steps on chemically *polished* wafers (note that table I gives best single measurement results, not best average results). After the phosphorus doping to 3×10^{20} cm^{-3} already a very low J_o of ~3 fA/cm^2 was achieved without any particular hydrogenation steps. Deposition of SiN_x:H reduced the best value of J_o further to ~2 fA/cm^2. Firing seemed to improve the effective lifetime but somewhat increased the best value of J_o to ~5 fA/cm^2.
Fig. 4 shows the evolution of average J_o per side on *textured* wafers through industrial process steps relevant for a solar cell production. The n-polySi/SiO_x capped with SiN_x:H was highly robust and showed on average J_o~10-20 fA/cm^2 per side after firing, thus proving that a direct implementation of n-poly into an industrial solar cell production is feasible. Some degradation of J_o after fire-through of the contact grid on the n-polySi is visible, which will be discussed in section 3.3.

Table II shows the best passivation characteristics measured on *textured* wafers (again, please note these are best single measurements, not averages). Similar results were obtained for Th.Ox and NAOS, with 200 nm thick polySi layers after firing of SiN_x. The achieved recombination currents of ~4 fA/cm^2 are to our knowledge the best n-polySi passivation results on textured Cz-wafers so far reported.

Table II: Best passivation characteristics obtained on *textured* wafers. Symmetric wafer structures with n-polySi/SiO_x on both sides. "Lifetime"= effective minority carrier recombination lifetime (@$\Delta n=10^{15}$ cm^{-3})

Cell type (polished, Th.Ox)	iV_{oc} (mV)	$J_{oe\ n\text{-}poly}$ (fA/cm^2)	*Lifetime* (ms)
After SiN_x and Firing (Th.Ox/200 nm, 39 Ω/sq)	~732	~4.2	~6.2
After SiN_x and Firing (NAOS/200 nm,71 Ω/sq)	~731	~4.3	~5.6

3.1 Application of polySi in industrial bifacial n-type cells

Table III presents an overview of the best *I-V* results of screen-printed H-pattern contacts on both sides of bifacial cells obtained in two consecutive experimental runs.

The cells showed ~82% bifacial performance (with back full area 200 nm thick n-poly; 46 Ω/sq). This bifacial ratio is about 10% less than for equivalent n-PERT cells with diffused BSF [9], and this loss is in agreement with the estimated absorption of short wavelength photons in the polySi.

Analysis of the half-fabricates (cells without metallization) and cells shown in Table III indicated that performance limitations due to the diffused B-emitter and contact at the front side were dominant in both runs. In Run1 the sub-optimal bulk lifetime (~750 µs on average, possibly due to lack of phosphorus gettering) also played a role, resulting in an average iV_{oc} for half fabricated cells without contacts $iV_{oc}^{(\text{half-fab. without contacts})}$ of ~680 mV. In contrast, in Run2 the bulk lifetime was greatly improved (~3 ms on average) resulting in an average $iV_{oc}^{(\text{half-fab. without contacts})}$ of ~693 mV. Optimization of the cell process was carried out in Run2 to further exploit the excellent potential of the n-doped polySi/SiO_x back contact, yielding the best cell efficiency of 20.72% (spectral mismatch corrected, FhG ISE calibrated n-PERT reference cell, AAA Wacom system, in house) with cell V_{oc} of 675 mV. The cell efficiency distribution over the 6 cells with NAOS/n-polySi (71 Ω/sq) was 20.68 with a standard deviation of 0.05. In Run2 the Th.Ox was apparently slightly thicker than in Run1 as the FF was ~1% abs. lower than in Run1. Lower FF in Run 1 with NAOS/n-polySi may be attributed to high Rsheet (158 Ω/sq).The FF with NAOS/n-poly back contact in Run 2 (71 Ω/sq) is similar to typical *FF* for equivalent n-PERT cells with diffused BSF, and it seems there is no significant series resistance loss (more than about 0.1 Ohm·cm^2) in the polySi/NAOS/wafer junction. However, a full series resistance breakdown analysis is not yet completed for these cells.

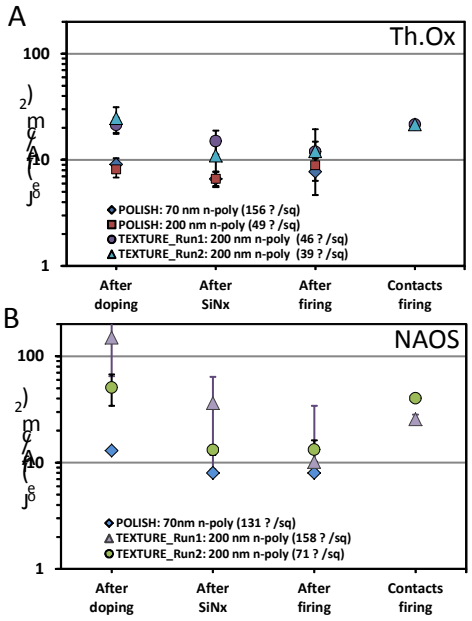

Figure 4: Evolution of average J_o per side of studied polySi/SiO_x carrier selective structures on *textured* as well as chemically polished wafers for cell production relevant steps. All J_o values are average of up to 15 points on 3 wafers and error bars depict standard deviations

Comparing J_o or iV_{oc} of 'half-fab. without contacts' with J_o or iV_{oc} of 'cell with contacts' in Table III and with the J_o with contacts in Fig. 4, shows that the losses related to the diffused B-emitter front side and front contact were dominant. Note that the J_o and iV_{oc} values given in Table III are best values (i.e., for best location on the wafer), while the V_{oc} for the cells with contacts are an average over the wafer due to the contact grids.

Furthermore some J_{sc} loss is due to non-contributing interband and free carrier absorption (FCA) in the polySi. The FCA in the n-polySi was evaluated by ray tracing analysis to be approx. 0.9 mA/cm^2 for 200 nm thickness and 3×10^{20} cm^{-3} phosphorus doping level. We intend to reduce this FCA by decreasing the polySi thickness and doping level. Table III illustrates the opportunity, through

the experimental variation of J_{sc} as a function of the polySi doping level.

Table III: Parameters of textured bifacial solar cells with 200 nm rear polySi. Best cell results are shown as well as best J_o, iV_{oc} and best bulk lifetime obtained on half-fabricates (obtained from Quasi-steady state photoconductivity decay QSSPCD, light I-V and SunsVoc measurements)

A	J_{oe} *n-poly w/o contacts*[*] (fA/cm^2)	J_o F+B *half-fab. w/o contacts*[*] (fA/cm^2)	J_o F+B *cell w/ contacts*[*#] (fA/cm^2)	iV_{oc} *half-fab. w/o contacts*[*] (mV)	iV_{oc} *cell w/ contacts*[*#] (mV)
Run1_Th.Ox 46 Ω/sq	9.7	64.7	~88	689	~679
Run1_NAOS 158 Ω/sq	7.9	63.9	~96	691	~672
Run2_Th.Ox 39 Ω/sq	5.1	58.9	~94	697	~675
Run2_NAOS 71 Ω/sq	7.7	56.2	~98	699	~680

B	V_{oc} (mV)	J_{sc} (mA/cm^2)	*FF* (%)	*pFF* (%)	η (%)
Run1_Th.Ox 46 Ω/sq	669	37.5	78.7	81.4	19.75
Run1_NAOS 158 Ω/sq	665	38.2	77.8	81.9	19.77
Run2_Th.Ox 39 Ω/sq	673	38.4	77.8	82.8	20.09
Run2_NAOS 71 Ω/sq	675	38.8	79.1	82.8	20.72

3.3 Outlook

Based on the obtained experimental results a qualitative description of key features of the passivating contact structures can be given.

The thin interfacial oxide layer needs to be thin enough not to limit the transmission of the majority carriers (allowing high *FF*) but should be dense/close enough to serve as a diffusion barrier, such that most of the doping is realized in the polySi layer. Slight dopant in-diffusion into the c-Si wafer (such as in the moderately leaky profile from Fig. 2c) is not harmful for the passivation properties and can be additionally beneficial for the transport of the majority carriers (perhaps avoiding transport via a tunneling mechanism only, allowing transport partially via less restrictive pinholes/percolation pathways [2]).

The polySi layer needs to be sufficiently high doped to allow adequate lateral transport for the application of bifacial grid metallization and also to provide a passivation boost by reducing the minority carrier density through the "field effect passivation". The thickness of polySi needs to be sufficient to block the penetration of the fire-through paste to the thin oxide interface. In our case 200 nm was sufficient, but we expect that thinner polySi will also be suitable. We have not yet attempted to make cells with the 70 nm polySi layers reported in this work. Also, the polySi thickness needs to be sufficient to allow the growth of phosphosilicate glass as a phosphorus dopant source, which is later on removed. On the other hand the thinner and the less doped the polySi layer, the lower parasitic absorption losses.

For the textured samples the hydrogenation of the interface defects is more critical, i.e., necessary for reaching very low J_o, compared to polished surfaces.

Fig. 5 presents a roadmap towards achieving 22%, which we have estimated assuming solely using industrial process equipment and materials. Firstly, the parasitic absorption in polySi can be reduced by making the layer thinner and less doped. Secondly, total J_o can be further reduced to 50 fA/cm^2 by implementing a higher R_{sheet} emitter and less penetrating fire-through pastes. Last but not least, the *FF* may be further improved by optimizing the thin interfacial oxide, and optimizing the front contacting grid design.

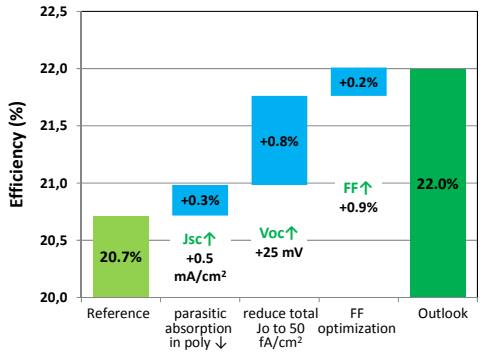

Figure 5: Roadmap towards 22% PERPoly cell

4 CONCLUSIONS

We presented studies of n-type polySi passivating contacts and their application on the back side of a high-performance bifacial n-type solar cell with fire-through screen-printed metallization, processed on 6" Cz wafers. The cell design is tentatively called PERPoly (Passivated Emitter Rear Polysilicon contact). The polySi/SiO_x passivating carrier selective contact structures were produced with a LPCVD-based process. The cell manufacturing further comprised, in addition to the LPCVD step, only processing on a small number of industrial tools, comparable to current n-PERT process

flows on the market. A best efficiency of 20.7% was achieved together with very high average cell V_{oc} of 674 mV. As an added benefit, the cells are bifacial with bifaciality factor >0.8. To our best knowledge these are the first published results on 6" cells employing LPCVD for the polySi, and also the first published results of cells employing a polySi passivating contact with fire-through screen-printed metallization.

The polySi/SiOx passivating contact layers were investigated in detail by varying interfacial thin oxide growth method, polySi thickness and doping profile. Excellent passivation has been obtained both on polished and textured surfaces with recombination current densities J_o of ~2 fA/cm^2 and ~4 fA/cm^2, respectively (after hydrogenation from SiNx). The effect of the fire-through grid on the J_o of the 200 nm thickness n-polySi contact was evaluated to be in the range of 10-30 fA/cm^2. These results show the high potential of this technology to augment current cell processes, with large performance headroom for the future. Reaching 22% seems feasible by a number of improvements, especially on the emitter side. This brings the use of polySi passivating contacts closer to becoming a reality in low-cost industrial solar cell processing.

4.2 Acknowledgements

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