Interdigitated Back-Contacted Silicon Heterojunction Solar Cells using Semi-Industrial Processing Equipment

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***Abstract* — Interdigitated back-contacted a-Si:H/c-Si heterojunction solar cells were made using two different approaches for patterning the a-Si:H layers: screen-printing in combination with wet chemical etching and in-situ mechanical masking. Processing was restricted to semi-industrial, low cost processing equipment on 6" wafers, cut back after processing into nine smaller cells by laser. After active layer patterning, implied V_{OC} values of over 700 mV were measured for both approaches and the best J_{SC} and V_{OC} values on cell level were 39.7 mA/cm^2 and 697 mV, respectively. Efficiencies over 21% are expected, when some metallization issues at the rear are solved.**

***Index Terms* — amorphous silicon, crystalline silicon, heterojunction, interdigitated back-contacted solar cells.**

I. Introduction

The 4 cm^2 25% efficient 'PERL' cell by Zhao et al. in 1999 [1] has been a long-standing record for wafer-based crystalline silicon solar cells. Nevertheless, industrial cells have been continuously approaching this record. In June 2010, SunPower reported a 24.2% full scale interdigitated back contact (IBC) cell [2] and in February 2013, Panasonic reported a lab cell efficiency of 24.7% for their 102 cm² heterojunction (HIT) solar cell. Finally, in April 2014 Panasonic surpassed the 25% barrier by combining the strengths of both concepts: an IBC-HIT cell, with on the rear side patterned a-Si:H layers forming local heterojunctions. The certified efficiency of the cell was 25.6% with a cell area of 143.7 cm² [3].

In 2007 and 2008 ENEA and ECN developed and published in collaboration 11% and 15% efficient lab size IBC-HIT cell results [4], employing shadow masking techniques. Here, we report on recent work at ECN on development of the IBC-HIT process with the aim to use only industrial process steps, able to shift the development to higher throughput "pre-pilot" equipment and 6" wafer size.

In this development, apart from ECN's industry-standard pre-pilot scale facilities (screen printers, chemical facilities, etc.), two similar scale HIT-specific tools were involved. Despite a high V_{OC} and a J_{SC} of nearly 40 mA/cm^2, the best cell efficiency was 12.6% on 13.3 cm^2 (9 cells per wafer). The cell efficiencies were limited by a high series resistance, the cause of which will be elaborated in this paper and which is expected to be well avoidable. Additionally, irreversible damage to the passivation of the a-Si:H layers was observed after deposition of the TCO layer, for which some solutions are proposed.

For reference and for better understanding of the industrial process results, in parallel also a cell process based on in-situ mechanical masking was developed, which is also presented.

II. IBC-HIT Solar Cell Process

The aim of this work was to design, develop and test a process flow using only tools from the industrially compatible toolset in ECN's laboratories plus c-Si/a-Si:H heterojunction specific equipment. This specific equipment consisted of an AK1000 tool (Roth & Rau AG) for the deposition of a-Si:H layers by Plasma-Enhanced Chemical Vapor Deposition (PECVD) and a second AK1000 tool for sputtering ITO and Ag layers. All processing was performed on 6" n-type Cz Si wafers of ~180 µm thick. After completion of the cell processing, the wafers were cut into 9 smaller cells by laser.

Emitter and BSF were formed by intrinsic/doped a-Si:H layer stacks. Two different process flows A and B for patterning these stacks were tested, based on wet chemical patterning of the a-Si:H layers (with similarities to e.g. [5]) and mechanical masking (with similarities to e.g. [6]), respectively. The essence of the patterning approaches is depicted schematically in Fig. 1. In process A, a dielectric (etch barrier) layer at the rear is opened locally using a screen-printed resist and wet chemical etching, after which the a-Si:H below is also removed by wet chemical etching (dashed outlined area in Fig. 1a). This sequence is repeated with the second polarity a-Si:H layer.

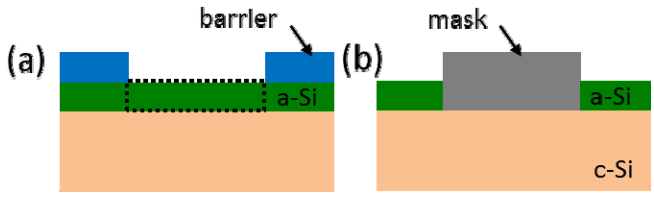

Fig. 1. Tested IBC-HIT process flows: (a) chemical patterning route – process A, (b) mechanical masking route – process B.

In the reference process B, the patterning of the doped amorphous silicon layers is performed by in-situ mechanical masking (Fig. 1b). It was found that the gap between wafer

and mask can be kept small, leading to apparently sharp and well-defined outlines of the deposited layers.

In both processes, metallization of the patterned a-Si:H stacks is achieved by applying PVD ITO and Ag, patterned by screen-printing. In a process denoted as B2, the ITO/Ag stack was replaced by E-beam Ag. In all cases, to lower the metal line-resistance, the metallization was thickened by printing low temperature Ag paste on top of the Ag lines, followed by a curing step. In future development, this could be replaced by a suitable seed layer with a Cu plating process.

III. Results

A. IV-results from Processes Compared

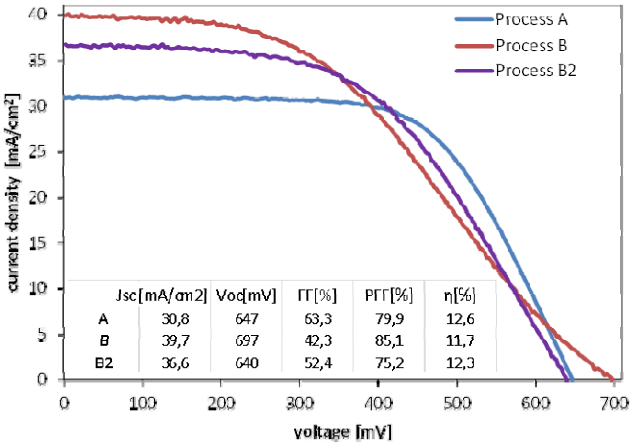

Fig. 2. IV-results of best cells prepared using process A (screen-printing and etching) and B (in-situ masking). Measured cell area was 13.3 cm^2 for all cells.

Fig. 2 shows the IV characteristics under illumination of typical cells produced using process A and B, as well as their performance parameters. Significant IV curve bending and a large difference between FF and PFF points to high series resistance in the order of 10 Ωcm^2 and even non-Ohmic contacts in some cases. The FF of process B is much lower than for process A due to an S-shaped IV-curve. Process A and B have the same PVD ITO/Ag metallization whereas E-beam Ag without ITO was used in process B2, showing no S-shape and higher FF.

B. Monitoring Implied V_{OC} Throughout the Cell Process

In Figure 3 implied V_{OC} values at different stages of the solar cell process are compared. The precursor stage involves a passivated front side and the first a-Si:H intrinsic/doped layer stack deposited on the rear. For both processes the implied V_{OC} is still above 700 mV after a-Si patterning. However, in process A a ~60 mV voltage drop is observed after metallization, which is not observed in process B, suggesting that this drop is related to the chemical processing.

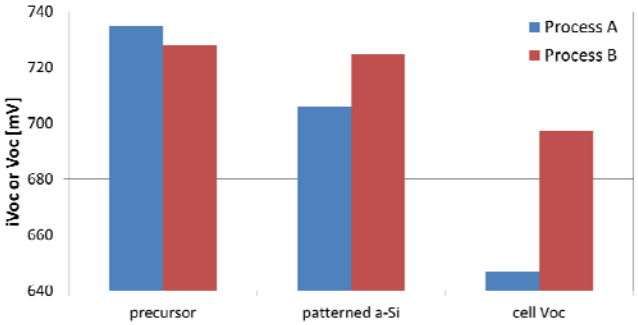

Fig. 3. Implied V_{OC} throughout the cell process compared.

C. Detailed Investigation of the V_{OC} Drop After Metallization in Process A (Industrial-type Process).

The voltage drop observed after metallization of chemically patterned a-Si stacks, was investigated in detail on precursors and patterned half-fabricates. Sputtering of ITO is known to damage surface passivation properties, but can normally be repaired by curing [7]. The chemically patterned intrinsic/doped layer stacks (process A), however, show a V_{OC} drop that cannot be repaired by curing (Fig. 4). For the same layer stacks without chemical patterning (representing process B), the implied V_{OC} remains at a high level after ITO deposition and curing. This suggests that after chemical exposure or a certain thermal history, degradation of the intrinsic/doped layer stacks after sputtering is irreversible. This was observed both for i/n and i/p-layer stacks.

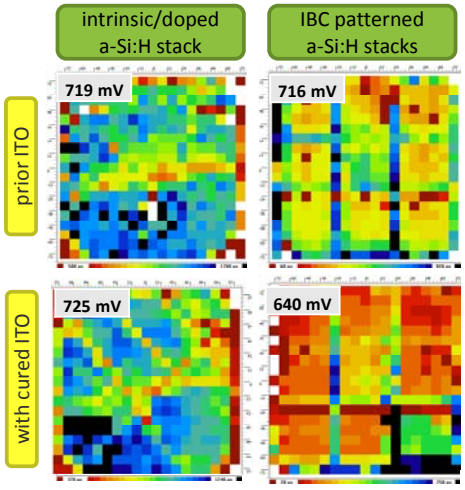

Fig. 4. Lifetime mapping images (microwave PCD) of a-Si fabricates before and after ITO deposition. Color scales are the same.

D. Delamination of Metallization

After curing of the Ag paste, the metal fingers at the rear of the cells were, in some cases, peeling off, indicating poor adhesion and stress. In the cross-sectional SEM images below (Fig. 5) a thin layer of sputtered ITO and silver is clearly visible in the middle of the emitter finger (Fig. 5a), covering the c-Si pyramids and separating the c-Si from a thick mass of Ag paste. At the edge of the finger, the Ag sheet is in many places detached (e.g. at the arrow in Fig. 5b) from the ITO below (slightly less bright region along the surface), locally resulting in very poor contacting properties. Similar local delamination was observed over the full width of the, narrower, BSF finger.

These poorly contacted regions can also be identified in forward electroluminescence images (EL) as dark areas along the edges of the emitter finger (Fig. 5c). It was observed for all cells, indicating that also the cells where the fingers remained on, might suffer from these stress- related issues.

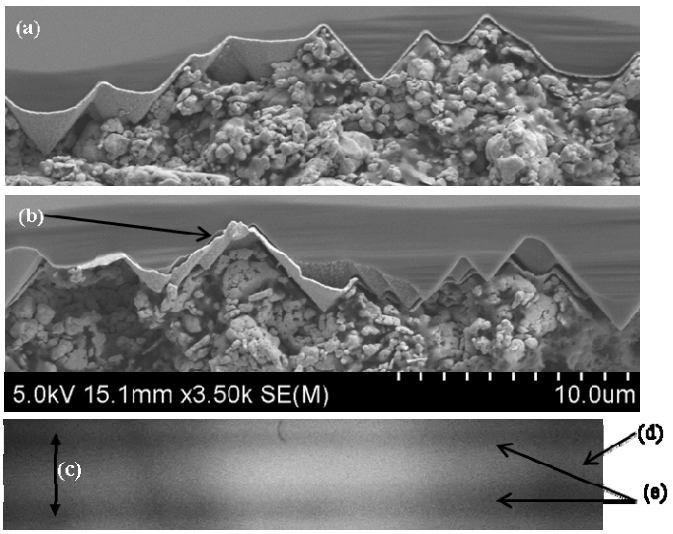

Fig. 5. SEM cross section from the middle (a) and the edge (b) of the emitter finger (top of the image is crystalline wafer, bottom Ag paste). In (b) the arrow indicates delamination. EL image of the emitter finger (c) the bright area in the middle (d) and the dark edges (e).

IV. Discussion

Two processing bottlenecks were identified: an irreversible drop in implied V_{OC} of ~60 mV after ITO deposition and a series resistance in the order of 10 Ohm cm^2.

The irreversible sputtering damage after chemical patterning needs to be analyzed in more detail, and can possibly be resolved by optimization of the chemistry or the thermal history within the process. Another way to solve it is to make use of a so-called 'soft' TCO or use no TCO at the rear at all. Using no TCO below the metal contact can lead, at least for E-beam deposited Ag to a V_{OC} degradation similar to that of ITO deposition, but in the field of alternative TCO's, recently, some promising results have been demonstrated with damage free In_2O_3 deposited by atomic layer deposition (ALD) [8].

The delamination of the metal fingers that we observe is most likely the cause of the very high series resistance in both process flows. Both approaches are limited by a series resistance of the same order. Both share the same metallization method, but have completely different approaches for patterning the a-Si:H layers.

A plausible explanation for the partial delamination of the fingers could be the limited adhesion of sputtered Ag on ITO combined with compressive stress due to cross-linking in the Ag paste during curing. Similar Ag lines are normally printed at the front side of standard HIT cells on a full sheet of ITO and not on Ag, therefore not displaying poor adhesion of the layers below. After resolving the series resistance and sputtering damage and assuming a FF of >78%, solar cell efficiencies well above 21% are expected.

IV. Conclusion

Two different approaches were tested for processing IBC-HIT cells on industrially standard equipment: using wet chemical etching or mechanical masking to pattern the active layers. Very high J_{SC} and V_{OC} values of 39.7 mA/cm^2 and 697 mV were achieved on the best cells. For both approaches, the cell performance was limited by a very high series resistance, which was tentatively attributed to the use of screen-printed Ag paste for contacting, causing stress and resulting in delamination of the emitter fingers. Additionally, the use of wet chemical etching for patterning of the a-Si:H layers can cause irreversibility of ITO sputtering damage, calling either for re-optimization of the process or low damage metallization methods.

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