20.3% MWT silicon heterojunction solar cell – A novel heterojunction integrated concept embedding low Ag consumption and high module efficiency

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***Abstract* — In this paper we present the successful integration of a silicon heterojunction (HJ) solar cell with metal wrap through architecture (MWT). This MWT-HJ cell and module technology combines all the advantages of the individual concepts. With this contribution we demonstrate a record device efficiency of 20.3% achieved using commercial n-type Cz 6 inch wafers. To our knowledge this is the first time that cell results for MWT-HJ architecture have been reported. We put this result in perspective providing a solution for the reduced conductivity of low temperature silver pastes used for HJ cell fabrication. We propose a method to increase the solar cell performance up to 4%$_{rel}$ together with a 50% cost of ownership reduction of the front silver metal including plug and conductive adhesive. This is possible solely by the optimization of the front metal grid in this MWT structure predicting efficiencies above 21%. MWT-HJ is a fully low-temperature integrated cell and module concept and compatible also with next generation thinner wafers.**

***Index Terms* — silicon, metal wrap through, heterojunction, photovoltaic cells.**

I. Introduction and Background

High efficiencies and low materials consumption are the main drivers towards low-cost ($/Wp) silicon PV modules.

Several solar cell technologies have demonstrated the ability to reach more than 20% cell efficiency. In addition, new back contact module technologies are now available to overcome losses caused by the interconnection and due to the limited width of the tabs.

In this contribution we demonstrate the successful combination of Metal Wrap Through (MWT) cell and module technology with Heterojunction (HJ) solar cells.

The vast majority of the market implements module technologies based on interconnection of solar cells in strings by tabs soldered from the front of one cell to the rear of the adjacent one. To limit shading losses caused by these tabs, such interconnection leads to additional resistivity losses in a string of cells thereby reducing the module performance. MWT technology provides a relatively small step from conventional cell technologies and has already demonstrated to increase the module power by 3%, and up to at least 5% is anticipated [1]. This is possible thanks to an integrated cell and module design in which conductive interconnection foil is used to reduce the cell-to-module power loss compared to conventional tabbing technology. Part of this gain is thanks to the reduced metal coverage on the front side, giving the solar cell performance a potential efficiency increase up to about 2.5% relative. Furthermore, thanks to the unit cell concept (the front contact of each unit cell connected to a rear contact by a through-cell via) an MWT cell structure decouples the wafer size from metallization requirements allowing for better cell-to-module power ratio.

Heterojunction solar cells have demonstrated more than 24% cell efficiency achieving excellent surface passivation with Voc exceeding 730 mV [2]. This has an impact on the temperature coefficient as well, resulting in higher module output power under real operating conditions. Nevertheless the low temperature Ag paste required for contact formation in HJ devices is still a challenge as it suffers from low conductivity resulting in high Ag consumption. Solutions such as multi-wire interconnection and multi-busbars have been introduced to tackle this conductivity issue. MWT-HJ architecture provides an alternative solution to the reduced conductivity of low temperature silver pastes while maintaining the above mentioned advantages.

Moreover, the low-temperature process required by heterojunction is perfectly met by the soldering-free MWT module technology which uses conductive adhesive and single step curing for interconnection and encapsulation. MWT and HJ cell technologies are also compatible with next generation thinner wafers resulting in a win-win situation both on cell and module level.

MWT-HJ devices combine all the advantages of the individual concepts in a device with high open circuit voltage, high short circuit current and high module power thanks to reduced power loss. Recent modeling of this cell architecture also predicted these attributes [3, 4]. In this paper, we show first results of this MWT-HJ solar cell architecture which resulted up to now in a record efficiency of 20.3% using commercial n-type Cz 6 inch wafers. To our knowledge this is the first time that cell results for MWT-HJ architecture have been reported.

Figure 1. Image of the MWT-HeteroJunction solar cell as presented in this paper.

II. Cell concept

MWT solar cells have the same architecture of a conventional solar cell with the addition that the front metal contact is wrapped through the wafer through metallised via holes, providing both emitter and base contacts on the rear side (Fig. 1). As the cell interconnection does not require tabbing the busbar can be significantly slimmed down enhancing the light harvesting in comparison to conventional H-pattern cells.

In a *front emitter* MWT-HJ cell structure the possibility of a reduced shunt resistance between the front metal contact and the base exists as shown in Fig. 2 unless the via metal and the rear-side emitter contact pad are stacked on an emitter layer, or isolated from the base in another way. This will result in complex processing requirements. On the other hand a *rear emitter* configuration has the advantage that shunt losses at the via or contact pad are largely avoided as the base does not participate to the hole transport and the a-Si layer has very limited lateral conductivity. However a local dead emitter area exists under the plug and it should be accounted for in the general concept evaluation (this point is addressed in the experimental section 3 and modeling section 4). Fig. 2 shows the *rear emitter* structure adopted for this MWT-HJ solar cell [5]. The two structures are compared from experimental and modeling point of view in this paper.

A *rear emitter* HJ device has other advantages too: placing the p-type a-Si:H layer at the back and removing the constraint of making it a window layer, allows for more freedom in the optimization of its thickness and conductivity. (i) The open circuit voltage can be improved and the field effect surface passivation enhanced by forming a sufficiently doped and thick p-type a-Si:H layer at rear [6] without increasing first pass light absorption. (ii) The cell fill factor is also believed to be further improved by higher doping or increased thickness of the p-type layer, by stronger band bending in favor of charge transport at the n-type c-Si/p-type a-Si:H interface and at the p-type a-Si:H layer/ transparent conductive oxide (TCO) interface [7],[8]. (iii) In addition the conductivity requirements of the front side TCO are reduced thanks to the extra lateral transport provided by the c-Si bulk in a rear emitter architecture [9].

A rear emitter device necessarily has an extra requirement regarding the wafer diffusion length as the majority of the photons are absorbed in the vicinity of the front side and the generated minority carriers have to diffuse to the rear side before to be separated. We fabricated front and rear emitter H-pattern solar cells as baseline process for the MWT-HJ and to verify the material requirements. By solely reversing the device architecture and using commercial Cz wafers we obtained equivalent IQE at longer wavelengths demonstrating that up to now material requirements are fulfilled by commercially available wafer technology. Nevertheless in general high efficiency devices require larger diffusion length than conventional state of the art devices due to the superior surface passivation implemented [10] and this has to be taken into account in any advanced concept.

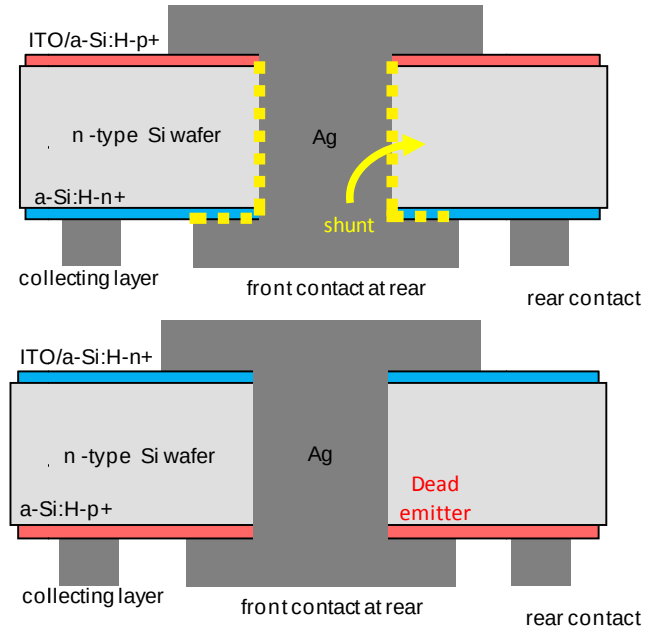

Figure 2. Structure of a front (top) and rear (bottom) emitter MWT-HJ solar cell.

III. Experiment results and process flow

6” industrial n-type Cz monocrystalline silicon wafers were used as substrate for MWT-HJ solar cell fabrication. After texturisation and dedicated surface cleaning, wafers were loaded into an AK1000 tool (manufactured by Roth and Rau AG), in which the intrinsic and doped a-Si:H layers were deposited by plasma enhanced chemical vapor deposition (PECVD). The ITO layers and rear Ag blanket contact were

produced by physical vapor deposition (PVD) in a second AK 1000 tool. Surface passivation quality was controlled by measuring effective lifetime of minority charge carriers and implied Voc on MWT-HJ cell precursors right after PECVD deposition. The metallization was realized by screen printing with low temperature silver paste followed by a curing step. The MWT-HJ solar cell process is the same as the HJ process with adding a few extra steps typical for MWT cell technology [1]: 1) vias drilling, 2) plug filling and 3) plug isolation. The H-pattern lookalike MWT used here is well suited to make loss comparison with H-pattern and is considered just as an intermediate step for the current development phase. We obtained a record efficiency of 20.3% as result of a very fast learning curve, showing the potentiality of this technology (Table I, in house measurement using a class AAA solar simulator and spectral mismatch correction) and Voc's of more than 730 mV on multiple devices. In Fig. 3 the box and whisker plot of the entire processed group of 28 cells is shown. For comparison, we obtained similar Voc in H-pattern front and rear contact *rear emitter* heterojunction solar cells.

Table I. IV-parameters record solar cell.

Record	V_{oc}	J_{sc}	FF	Efficiency
MWT-HJ	734 mV	36.3 mA/cm^2	76.3 %	20.3 %

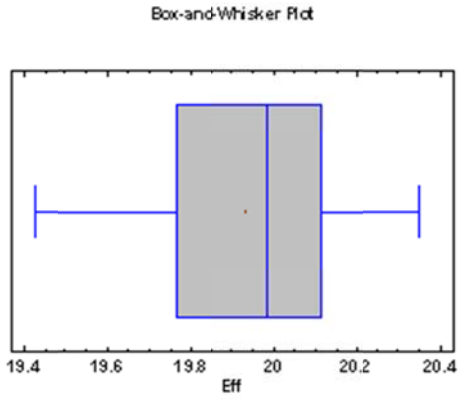

Figure 3. Box and whisker plot over the entire processed group of 28 cells.

We measured a current of about 3 A at -10 V (I_{rev}), a relatively high value for module manufacturing. However, as determined by LIT, the heat dissipation is restricted to the edges of the cells and not at the vias [11]. This proves that the edge isolation needs to be improved for this *rear emitter* cell and that the MWT structure is not responsible for the high current under reverse voltage. In addition, we have demonstrated on front and rear contact *rear emitter* devices that the I_{rev} becomes less than <0.1A after improving the edge isolation. This can be easily implemented on the MWT-HJ process.

We also manufactured *front emitter* MWT-HJ cells to verify our initial hypothesis of the different behavior with respect to shunts. These *front emitter* MWT-HJ cells are indeed strongly limited by shunt formation at the vias resulting up to now in 2% absolute lower efficiency. In Fig. 4 Lock in Thermography images of the *front* and *rear emitter* cell are reported. The advantage of the *rear emitter* MWT-HJ architecture with respect to the *front emitter* is shown on the ohmic shunt patterns around the vias.

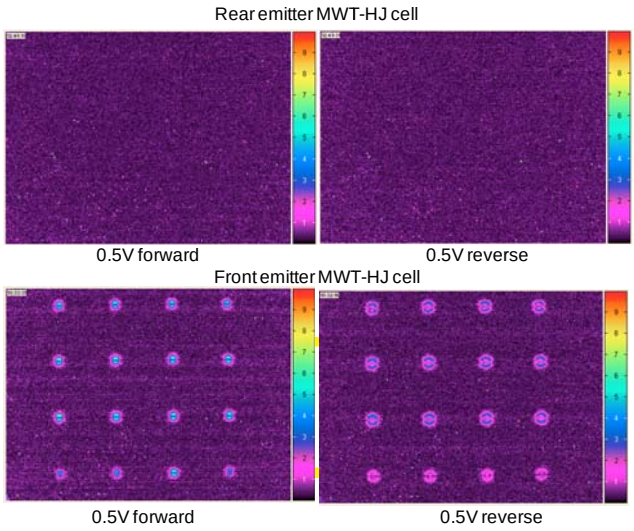

Figure 4. Lock In Thermography of a *front emitter* and *rear emitter* solar cell in forward and reverse currents. The advantage of the *rear emitter* configuration with respect to the absence of shunts at the vias is clear.

IV. Challenges and Potentiality of the Device Architecture

Heterojunction devices are fabricated using low temperature PECVD and PVD processes and do not tolerate high temperature steps. This requirement is perfectly met by soldering-free MWT module interconnection technology which uses single step curing for interconnection (using conductive adhesive) and encapsulation [12,13]. Nevertheless the metallization using low temperature Ag paste is still a challenge for HJ. The reason is that the low temperature Ag line conductivity is about 3 times lower than the one for conventional fired pastes [14] and only few paste suppliers are currently available. As solutions, Cu plating and multi-busbar approaches in order to reduce the finger length have been investigated [15, 16, 17]. The latter has the double advantage to reduce both the Ag consumption and the series resistance losses on cell level at the same time. Here we propose the

MWT cell design as an alternative method to reduce the resistive power losses and the silver consumption in heterojunction solar cells, matching with an integrated module technology, and relying on industrially proven screen printing technology for cell metallization.

The MWT solar cell structure is based on the concept of unit cells [18]. The advantage here is that the area of the unit cell can be optimized separately from the wafer size and replicated to cover the full cell area [19]. By reducing the unit cell area the resistive power losses are reduced, in principle, quadratically, therefore allowing for less metal coverage and giving more freedom to optimize the metal consumption versus cell performance. Increasing the number of vias not only reduces the finger length, but also the length of the BB in this H-pattern lookalike MWT front grid, and therefore reduces the impact of the lack of interconnection tabs on the front side. On the other hand this effect is reduced using star-alike patterns since they are designed for nearly optimum metal usage in a MWT unit cell [20].

We calculated the impact of the unit cell area reduction, by increasing the number of vias without changing the full cell area. The effect for paste reduction and cell performance is similar to increasing the number of BBs for H-pattern front-to-back contact cells. However, interconnecting these multi bus bar cells requires machines that become more complex with increasing number of bus bars. On the contrary, MWT-HJ solar cells are perfectly compatible with already existing conductive foil based module technologies and are less dependent on the number of vias.

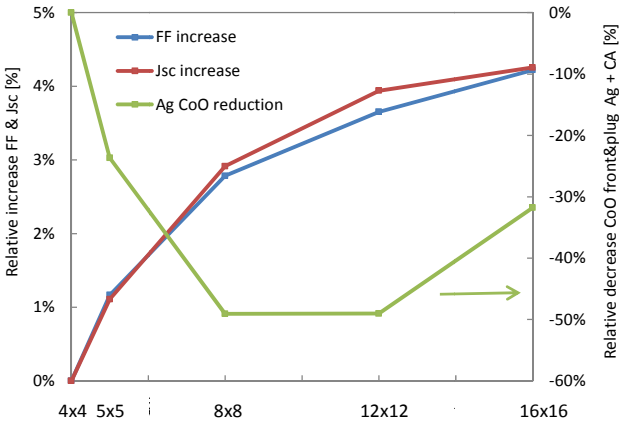

Figure. 5. Calculated relative FF and Jsc variations as a function of the number of vias for MWT-HJ cells. The cost of ownership (CoO) reduction of the front contact silver including plug and conductive adhesive (CA) is also calculated (right axis).

Fig. 5 shows the FF and Jsc variations with the increasing number of vias per cell together with the cost of ownership (CoO) of the front contact silver including plug and conductive adhesive (CA) used for front metallization, plug and module interconnection. For each configuration the finger width has been reduced inversely to the number of vias per length (i.e. 100 µm finger width as base for the 4×4 structure reduced to 50 µm for the 8×8 structure) but keeping the same aspect ratio and optimizing with respect to the number of fingers and (tapered) BB width. The impact of the extra conductive adhesive and plug metallization costs have also been included. Indeed a small unit cell relaxes the requirements for finger cross section and the busbar conductivity (width) of the LT-Ag paste. A front metal+plug+CA CoO reduction of about 50% is calculated with an 8×8 vias configuration leading to about 6% relative efficiency increase with respect to a 4×4 vias configuration. An efficiency potential of over 21% is estimated for the current processes by optimizing the front metallization only. This multi-vias approach enables the front metallization optimization for high efficiency and/or Ag reduction. In addition it has a benefit on the rear Ag consumption for the same reason. The amount of metal in the rear side is expected to decrease resulting in a further Ag CoO reduction. The copper pattern on the conductive foil can easily be adjusted from the standard 4×4 MWT configuration to accommodate the 8×8 vias configuration, with a computer-controlled patterning process, such as pattern milling or laser scribing [12, 13].

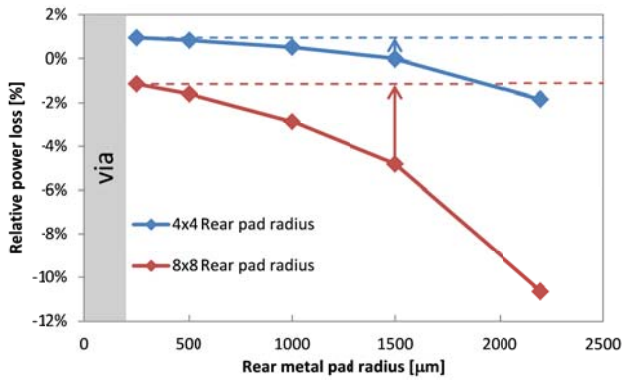

Figure. 6. Calculated relative power losses for a 4×4 and 8×8 configuration as function of the rear pad radius (front metal contact at the rear). The arrows represent an estimate of the gain when isolating the real metal pad, equivalent to the smallest rear metal pad radius, and the dash lines are a guide for the eye. Dead emitter area per via is kept constant. In the experiment reported in this paper we used a 4×4 configuration with a rear metal pad radius of 1.5mm (reference).

Besides to the performance enhancement and cost reduction benefits due to the front grid, the increased number of vias can have a potential negative impact on the recombination current. In the 4x4 device structure the experimental results show the advantage of a *rear emitter* structure over the *front emitter*. We carried out 2D simulations with ATLAS [21] confirming

the large impact of the shunt in a *front emitter* structure in comparison to the recombination currents in the overall volume surrounding the vias (see Fig. 2) in a rear emitter cell. However when the dead emitter area per via is kept constant, increasing the number of vias will increase this recombination due to its increased ratio with respect to the unit cell area. 2D simulation results are reported in Fig.6. For the model a simplified cell geometry was used. The simulation domain was confined to the cell section surrounding one via. Cylindrical coordinates were used to allow for a realistic ratio of the dead and active emitter areas. We modeled the worst case scenario with no via passivation. The model showed very small Voc losses in agreement with the experimental results reported in the previous paragraph while Jsc and FF are affected. This is explained by the reduced active emitter area and by extra recombination in the dead emitter area which is in contact with the metal plug. In Fig.6 we report the model results for a 4×4 and 8×8 device structure as function of the rear side metal plug radius. The dead emitter area is kept constant for simplification. This, however, is not a physical or technological limitation since there is no reason why the dead emitter area cannot be reduced proportionally to the rear metal pad. In the 4×4 configuration the power losses are limited and the sensitivity towards the rear pad radius is very weak. This is because of the relatively low number of vias in the cell. On the contrary in an 8×8 configuration, the ratio of dead versus active emitter in the unit cell increases and therefore the cell performance is more sensitive to the rear pad radius. Another alternative is to isolate the rear metal pad from the dead emitter. This is equivalent to the smallest rear pad in the simulation of Fig. 6. By reducing or isolating the rear metal pad the power loss can be reduced to below $2\%_{rel}$ in this worst case scenario. Combining this with the $6\%_{rel}$ increase due to the front metal optimization (Fig.5) an efficiency increase of up to $4\%_{rel}$ is expected for the 8×8 configuration with respect to the current 4×4 and in addition the front contact silver including plug and conductive adhesive cost reduction of 50%.

It is anticipated that a further benefit is achieved by reducing the dead emitter area.

V. Summary

In this paper we present the successful integration of a silicon heterojunction (HJ) solar cell with metal wrap through architecture (MWT). MWT-HJ devices combine all the advantages of the individual concepts in a device with high open circuit voltage, high short circuit current and high module power thanks to reduced FF power loss and better temperature coefficient. The module technology would perfectly meet the low temperature requirements of HJ cells by implementing soldering-free MWT module technology which uses single-step curing for interconnection and encapsulation. Additionally, MWT and HJ cell technologies are compatible with next generation thinner wafers.

In this contribution we demonstrated a device efficiency of 20.3% achieved in commercial n-type Cz 6 inches wafers and a median efficiency of 20%. We prove the advantages and ease of the *rear emitter* structure to avoid shunt losses. To our knowledge this is the first MWT-HJ solar cell manufactured.

The concept of MWT grid unit cells addresses the normally high Ag consumption of heterojunction cells. By decoupling the cell size from the metallization requirements, resistive power loss in the cell (as well as in the module) is reduced with less silver consumption than in conventional front-to-rear contact heterojunction solar cells. We propose a method to reduce up to 50% the cost of ownership of the total front contact silver including plug and conductive adhesive while predicting efficiency greater than 21% solely by the optimization of the front metal grid and MWT configuration. We anticipated that similarly Ag consumption on the rear side can also be reduced. This concept is also suitable for performance versus CoO optimization in a fully integrated cell and module concept.

The advantage of this combined approach is that any developments in conventional hetero-junction and in conventional MWT technologies are directly and easily transferred to MWT-HJ solar cells. Thereby substantially higher efficiencies are within reach with limited process adaptations.

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