XIS: A Low-Current, High-Voltage Back-Junction Back-Contact Photovoltaic Device

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Abstract — **In this paper we present a low-current, high-voltage back-junction back-contact integrated photovoltaic concept and experimental results of such a device, consisting of strip cells: narrow solar cells instead of conventional square cells. The concept is demonstrated by the successful transformation of a completely finished IBC cell into a XIS (Crystalline Silicon Interconnected Strips) device, leading to a V_{oc} of 8.5 V for a series connection of 14 strip cells. For cell separation, different grooving methods were evaluated with respect to their effect on the quality of the groove surface. The effect of the surface passivation in the grooves, which is regarded as a critical parameter, on the XIS device was simulated to gain a better understanding of the processing requirements.**

Index Terms — **back-junction back-contact, crystalline silicon, high-voltage, passivation.**

I. INTRODUCTION

PV system prices have dropped considerably during the last year, but still a further reduction in costs is required to create a sustainable and competitive alternative in the energy market. An important part of the module costs is in the materials, and therefore it can be understood that a large reduction in the use of materials like metal and silicon will enable a break-through in cost reduction. Minimization of silicon consumption is foreseen by the introduction of very thin (<50 µm) wafers, preferably made with a kerf-free production method. Several publications show the current interest and developments in kerf-free wafering [1-2]. The reduction of metal costs in wafer-based silicon modules requires two modifications, a) replacement of expensive silver by much cheaper materials like copper or aluminum, and b) adaptation of the device architecture into low-current devices, which allows less metal without power loss.

The XIS (Crystalline Silicon Interconnected Strips) device concept addresses both the decrease in material consumption and the device design requirements, which are implemented by reducing the cell dimensions in the direction of the current flow by a factor of typically 50-100. Further cost reduction and easy module fabrication is foreseen by implementation of low-temperature high-efficiency hetero-junction processing and back-contact device design. The recently obtained 23.4% efficiency on small area and 20.7% efficiency on full-size wafers by LG [3] demonstrate that BC-HJ devices can also reach high efficiencies in practice and on large area. Integrated

module concepts on bonded wafers are subject of interest at imec [4], and reliable interconnection of low-cost aluminum metallization for back-contact cells is extensively investigated by ISFH [5].

II. THE XIS CONCEPT

An individual XIS cell can be regarded as a unit cell of an Interdigitated Back Contact (IBC) cell, consisting of a single emitter area next to a BSF area on the rear side. Each unit cell is electrically isolated and connected in series to the adjacent one, rapidly building up the voltage. The current per cell is reduced by the number of unit cells (strips) that are cut from a 156 mm wafer. In this way, low currents and high voltages are realized. In Fig. 1b a schematic XIS structure is presented, deduced from an IBC-HJ structure as shown in Fig. 1a.
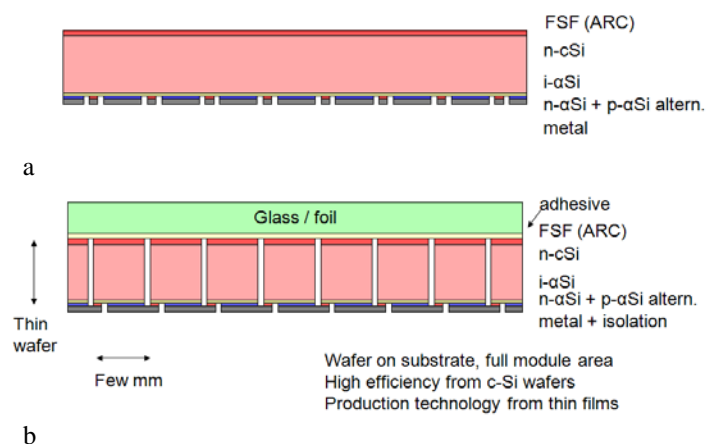

Fig. 1. Schematic cross-sections indicate the similarity of a) IBC and b) XIS. The XIS device consists of a series connection of narrow solar cells.

It has certain advantages to establish the strip formation while the wafer is already attached to a superstrate, instead of handling the individual strips separately. In this case the front side of full-size wafers is processed first, e.g. for texture, FSF formation and passivation. Then, multiple wafers can be bonded to the sun-receiving (glass) superstrate. After bonding, processing can be done on module level, i.e. strip separation,

emitter and BSF formation, cell edge and rear side passivation, metallization and interconnection. After bonding, the processing temperature is restricted to the maximum temperature tolerated by the bonding material, e.g. approximately 200°C in the case of silicones. The use of a-Si:H layers is proposed for XIS device processing, as it is very suitable in terms of deposition temperature and passivation quality. The proposed process flow for the XIS concept is sketched in Fig. 2. The processing steps within each block can be carried out in a different order than suggested here.

One of the consequences of the strip cell design is the increase of the edge area per cm^2 of cell surface, which implies a high sensitivity to edge recombination. Therefore, important aspects of the XIS device processing are the formation of the grooves in the wafer that define the strip cell area, and the passivation of these grooves. In the next section we will focus on these two aspects.
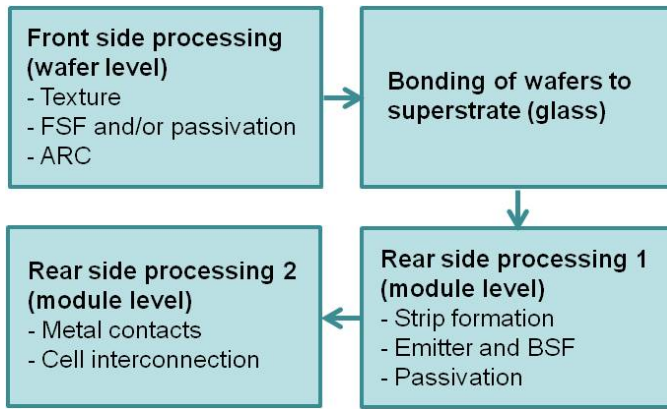

Fig. 2.   Process flow chart of the XIS concept.

A. Groove Formation

The grooves in our first XIS devices, as presented previously [6], were realized by conventional dry laser processing, including an etch step afterwards to remove the laser damage from the grooves, and passivation of the grooves by PECVD SiN$_x$. In general, conventional dry laser scribing results in grooves with considerable damage and debris on the wafer surface. In Fig. 3a the cross-section of a wafer is shown, which was scribed up to half of the wafer thickness, and then broken. The broken part of the wafer reveals a smooth surface for comparison. The grooves in the XIS device are realized by grooving through the complete wafer.

We investigated more advanced techniques for groove formation, which are capable of cutting silicon with minimal damage. The first is a Laser MicroJet (LMJ), which is a water-jet guided pulsed laser beam, producing debris-free grooves in the silicon with very smooth edges, as is shown in Fig. 3b (left). The water cooling results in a very small heat-affected

zone. Therefore, the damage to the silicon will be much smaller. The other investigated method is Thermal Laser Separation (TLS) [7], which is a cleaving technique based on guiding a crack in the silicon by laser-induced mechanical stress. This technique produces a debris-free and smooth cleaved surface, as is shown in a wafer cross-section in Fig. 3b (right). As TLS grooving occurs without kerf loss, care must be taken to physically separate the strip cells, for example by using a stretchable substrate or a pick-and-place mechanism [8]. We investigated these methods in XIS device processing while omitting the etching step before passivation, and even left out the passivation step as well.
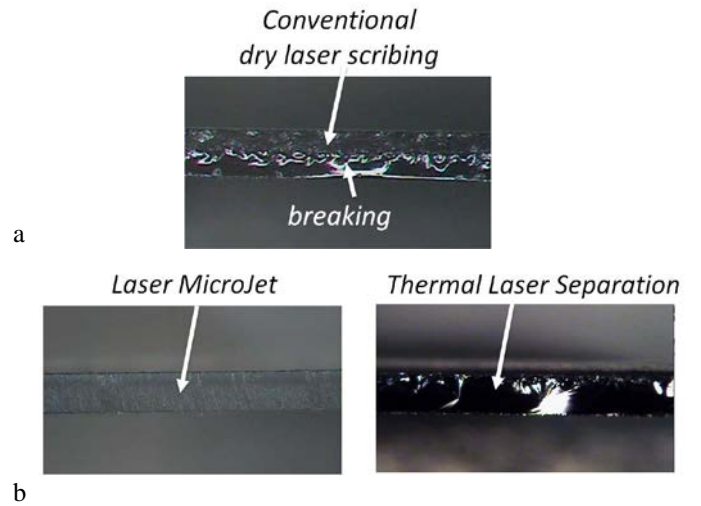

Fig. 3.   Cross-sections of silicon wafers cut with different techniques, namely a) conventional dry laser cutting, half-way, and breaking, b) the advanced techniques: Laser MicroJet (left) and Thermal Laser Separation (right).

B. Edge Passivation

Given the relatively large edge area of the strip cells, i.e. the grooves in the wafer, the passivation of the cell's edges needs to be excellent to prevent a loss in J_{sc} and V_{oc}, as shown in Fig. 4 in a simulation of the XIS device with homo-junctions in the ATLAS simulation software package [9].
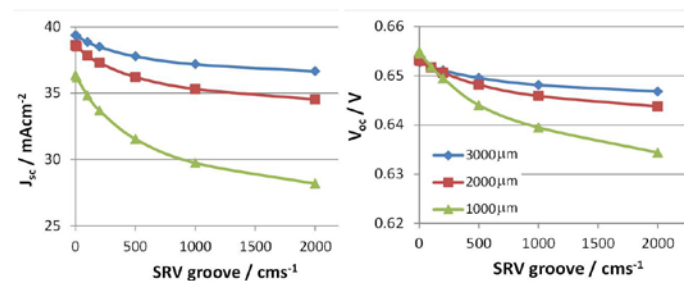
Fig. 4.   XIS device simulation, showing the importance of groove passivation on J_{sc} (left) and V_{oc} (right) for different cell widths (1000, 2000 and 3000 µm).

For three typical values of the cell width and a wide range of groove passivation quality, the resulting cell parameters were calculated. An increased value of the surface recombination velocity (SRV) at the cell edges has a very pronounced effect on especially J_{sc}. As the surface morphology and the amount of defects present are important factors for the edge passivation, the grooving method itself will be of major importance for the passivation. Cells, separated with the different techniques, can be compared in terms of J_{sc} and V_{oc} to reveal the quality of the grooving technique.

In general, XIS devices with hetero-junctions will reveal an even higher sensitivity to the cell edge SRV, as the passivation of a-Si:H emitter and BSF regions is of a much higher level compared to homo-junctions passivated with SiN_x. In this case, however, we have chosen to simulate the homo-junction device, which is based on the experimental devices presented in the following section.

III. IBC-To-XIS Device Transformation

As described before, the architecture of a XIS cell can be regarded as an IBC unit cell. By transforming a finished IBC cell into a XIS device, as schematically drawn in Fig. 5, we are able to demonstrate important aspects of our concept by only applying its essential features that distinguish a XIS device from an IBC cell. These features include electrical separation of the IBC unit cells by making grooves through the wafer, passivation of the grooves, and series connection of several strip cells.
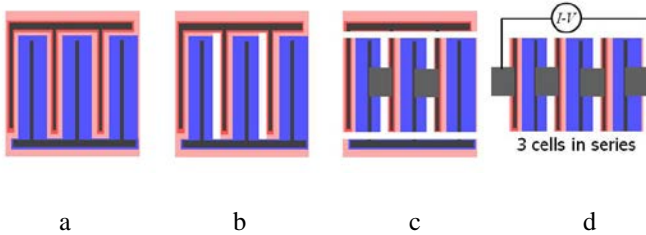

| a | b | c | d |

Fig. 5.   Schematic drawing of the device's rear side during IBC-to-XIS transformation (light pink: base; red: BSF; blue: emitter; dark grey: metal): a) IBC cell, b) IBC cell after groove formation, c) after separation of the strip cells from the IBC busbars and strip cell interconnection, d) XIS device that can be measured.

A. Conventional Dry Laser

We used conventional dry laser processing to make grooves in an IBC cell with diffused junctions. A process description of this IBC cell with homo-junctions can be found in our previous work [10]. The grooves were spaced 2 mm apart, as this was the smallest pitch available in our IBC cells, and the strips were still connected to the IBC busbars. After laser damage etching and groove passivation with SiN_x, the IBC cell was measured again, as shown in Fig. 6. The remarkable result was that the V_{oc} only dropped 4 mV (0.6%). It should be noted that the V_{oc} value of the IBC cell in this experiment was about 20 mV below the value used in the simulation. Both I_{sc} and FF showed a considerable decrease (5-7%), of which the ΔI_{sc} can be explained by active area loss and increased recombination, and ΔFF by an R_{series} increase due to the increased lateral transport length of the majority carriers through the resistive bulk, as the grooves now block one direction of the transport path.
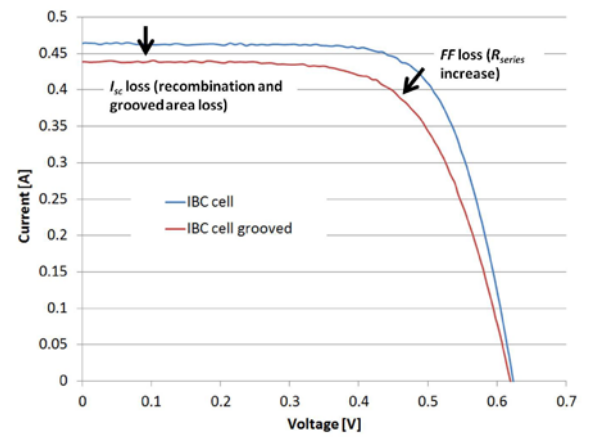

Fig. 6.   I-V curve of an IBC cell before and after formation of grooves.

After measuring the IBC cell with grooves, the strips are cut from the IBC busbars. In this way the strips become completely isolated and act as separate cells. The interconnection of the cells is realized by conducting "bridges" to complete the IBC-to-XIS transformation.

Pictures of the front and the rear side of the device are shown in Fig. 7a. The series of strips resulted in a low-current, high-voltage device with a V_{oc} of 4.3 V over 7 cells. The cells show very similar performance with respect to each other. The I-V curves of this XIS device are shown in Fig. 7b (light blue dashed lines). Compared to the original IBC cell, the XIS cells lose on average 1.9% in V_{oc}. For a hetero-junction device that typically shows much higher V_{oc} values, the need for excellent passivation is even more important. Fortunately, we can see many opportunities for improving the groove passivation, as in the current case the choice of passivation process is limited by the presence of screen-printed metallization on the parent IBC cell. For example, extended chemical treatments may dissolve the glass in the metallization, and were therefore not carried out. Furthermore, metallic particles may have detached from

the screen-printed metallization and could have been deposited on the grooved surface, hindering the SiN_x passivation. Finally, the strip cells are cut from their parent cell only after passivation, interconnection and fixation, which leaves two narrow non-passivated areas at the two ends of each strip cell. For optimal device results, all cutting should be finished before etching and passivation.
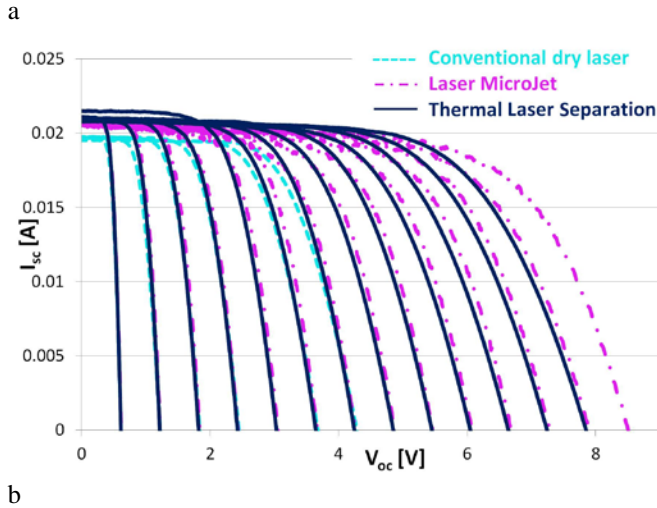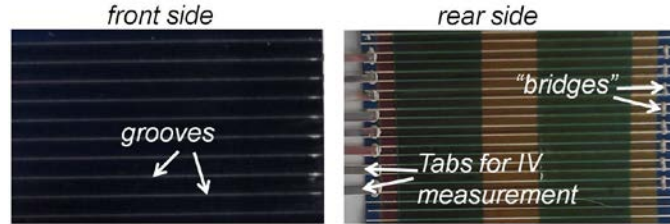

a

b

Fig. 7.   a) Picture of the front and the rear side of a XIS device, b) *I-V* curves of XIS devices consisting of up to 14 series connected strip cells, using different grooving methods to separate the strips from an IBC cell.

B. Laser MicroJet

A Laser MicroJet was used to cut a similar IBC cell, but in this case the etching step was omitted and SiN_x deposition was optionally performed to investigate the quality of the as-cut groove. Up to 14 strips were interconnected, which resulted in a V_{oc} of 8.5 V as shown in Fig. 7b (purple dash-dotted curves). The higher I_{sc} in the graph is due to the higher I_{sc} of this particular IBC cell. The V_{oc} (averaged over 7 strips) is 3.0% for cells separated by as-cut grooves without SiN_x passivation, and 3.3% for cells with SiN_x passivated grooves. This is lower than the original IBC cell, but the results for both LMJ cases are nearly the same. However, in both cases the LMJ technique yields a slightly higher loss compared to the use of a conventional dry laser with damage etching and passivation. Still, the performance of the strip cells that were cut with the LMJ technique is very similar with respect to each other,

which is an indication that this grooving method can be applied in a reproducible way.

C. Thermal Laser Separation

Thermal Laser Separation was used to cut another IBC cell, without additional damage removal or a passivation step. Up to 13 strips were interconnected, which resulted in a V_{oc} of 7.8 V as shown in Fig. 7b (dark blue curves). The V_{oc} loss (2.4%) is slightly lower than for the LMJ cases, and almost as good as the etched and passivated grooves made by conventional dry laser processing. The XIS results for non-passivated grooves made by LMJ and TLS are very promising, but in order to obtain negligible J_{sc} and V_{oc} loss compared to the parent IBC cell, these techniques need additional processing to obtain excellent surface passivation at the edges of the cells. It should be noted that in the cases of LMJ and TLS the strip cells were cut from the busbars by conventional dry laser without further etching or passivation of these two narrow cell edges.

D. Comparison of Techniques

We observe a very similar performance of the neighboring strip cells within each XIS device, which means that the investigated techniques can establish reproducible grooving. The loss in V_{oc} for the XIS devices with respect to the parent IBC cell is 2-3%, depending on the grooving technique, as summarized in Table 1. This corresponds, according to the simulation results, to an average SRV of more than 2000 cm/s at the groove surface for strips of 2 mm width. The considerable loss in J_{sc} confirms the high SRV at the grooves. The *FFs* of the individual *I-V* curves are roughly the same, but lower than the IBC cell from which they originate. As already mentioned, this can be at least partly explained by the increased R_{series} due to extra ohmic losses in the silicon base after the groove application. As the BSF contact is located at the edge of a XIS cell, the majority carriers will, on average, travel a longer distance before being collected compared to the parent IBC cell, in which the majority carriers reach the BSF contact from two directions.

TABLE I
AVERAGE V_{OC} LOSS OF STRIP CELLS

Grooving method	V_{oc} loss
Conventional dry laser	-1.9%
+ damage etching	
+ SiN$_x$ passivation	
Laser MicroJet	-3.0%
Thermal Laser Separation	-2.4%

IV. CONCLUSION AND OUTLOOK

The XIS concept has the potential to achieve a significant cost reduction, cutting down the bill of materials by limiting

the silicon consumption and eliminating the use of expensive metals. The back-contact hetero-junction silicon solar cell technology allows high efficiencies and simplified module technology.

In a proof-of-principle experiment, IBC cells were successfully transformed to XIS devices. Advanced grooving methods have shown very promising results even without any additional treatment for damage removal or passivation. All techniques yield reproducible grooving results, shown by the similar performance of the strip cells. Up to 14 strip cells were interconnected in one series and complete series of *I-V* curves were measured for each grooving technique.

In the future, well-passivated cell edges are expected for advanced grooving techniques in combination with a damage removal and edge passivation step. This will be especially well applicable in the absence of screen-printed metallization, which limits the etching and passivation options and the resulting performance.

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