QUALIFICATION OF MULTI-CRYSTALLINE SILICON WAFERS BY OPTICAL IMAGING FOR INDUSTRIAL USE

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ABSTRACT: We have developed a method to qualify multi-crystalline silicon (mc-Si) wafers that are being used in a production process. An optical image of an etched wafer is made. This etching can be a standard industrial acid etching for mc-Si wafers as is commonly used for saw damage removal and simultaneous iso-texturing. Digital image processing is then applied to identify the number of dislocations and their distribution over the wafer. This information is used as input for a cell performance prediction model, where the performance is characterized by the open circuit voltage (*Voc*) or the efficiency. The model can include various levels of sophistication, i.e. from using an average density of dislocations to the full spatial resolution of the dislocations in a 2D simulation that includes also the metallization pattern on the cell. The predicted performance is then evaluated against pre-selected criteria. The possibility to apply this optical qualification method in an initial stage in the production enables early rejection of the wafers, further tailoring of the cell production process or identification of instabilities in the production process.
Keywords: characterization, qualification and testing, multi-crystalline silicon, modeling, optical imaging.

1 INTRODUCTION

Crystalline wafers contain dislocations, for example as a result of thermal stresses over the ingot during the crystal growth process. Since the dislocation density varies over the whole ingot, the density and spatial distribution of dislocations may vary from wafer to wafer. Dislocations in multi-crystalline silicon (mc-Si) wafers are well known to cause reduced solar (photovoltaic) cell performances [1]. At dislocations the minority charge carriers have a lower lifetime due to the imperfect crystal structure or from enhanced concentration of metal impurities. A cheap method that identifies dislocations in individual wafers and predicts their impact on the cell performance will contribute substantially to improvement of the cost effectiveness of solar cell production. The qualification of individual wafers should take place as early as possible in the solar cell manufacturing process, and should preferably be applied in-line, and be non-intrusive and fast.

The method presented here can be used in-line, directly after the acid etching procedure of the combined saw damage removal and iso-texturing step, without any further pretreatment. Other wafer qualification methods can often not be used in-line. Electroluminescence requires a metallization pattern and hence can only be carried out at the end of the product line. Other optical imaging procedures are destructive since they require dedicated, non-industrial etching [2]. Photoluminescence (PL) can be used in-line at various stages of the production process, including on as-cut wafers [3,4]. However, PL essentially measures the minority carrier density which strongly depends on the prevailing local effective lifetime. The prevailing life-time of the minority charge carriers is an important parameter for the resulting cell performance, but the effective life-time will change upon subsequent gettering and passivation steps. Therefore, as has been demonstrated recently in the literature, the PL images taken at different steps of the manufacturing process show very significant differences [5,6]. This makes the method less attractive for characterization of as-cut wafers.

The method described in this work, for which a patent application was filed, enables tailored processing (e.g. different metallization patterns) or early rejection of low-quality wafer as well as process fault detection [7]. The latter may be implemented in a Manufacturing Information System (MIS), preferably in conjunction with wafer tracking. Adding information of the incoming material quality in the MIS enables a higher level of process optimization.

2 METHOD

2.1 Outline of the approach

After the standard industrial acid etching, an optical image of the wafers is made with a photocopier or flat-bed scanner. A digital image processing algorithm is applied to obtain a 2-dimensional map of the dislocation distribution. This map is input for a performance prediction model. In this model, the dislocation areas are associated with locally inferior cell performance characteristics. A validation and deployment phase are distinguished. In the validation phase image processing and performance prediction is performed on a limited set of optical images to determine the parameters that optimize the correlation with measured PV cell performance characteristics. In the deployment phase, the obtained parameters and models are used to predict the cell performance of a wafer.

2.2 Optical imaging

The wafers are etched by a mixture of HF and HNO_3 and CH_3COOH that is applied in the industrial process to remove saw damage and obtain iso-texture. Subsequently an optical image is taken with a photocopier or a flatbed scanner. This allows fast scanning of the entire surface.

2.3 Digital image processing

An image processing based on edge detection is used to quantify the information in the obtained images. This can include smoothing of the image with numerical filters and selection of thresholds to reduce the number of false edges. Optimization of parameters for the digital processing is part of the validation phase. The processed image is then translated to a map where “good” and “bad” areas are distinguished. Thresholds and grid

resolution are used to construct this map.

2.4 Performance prediction model

The performance of the solar cell is characterized by the open circuit voltage V_{oc} or by the efficiency η. For modeling purposes, the dislocation areas (bad areas) are associated with a high dark saturation current density ($j_{0,b}$). Areas without dislocations (good areas) are associated with a lower value for the dark saturation current ($j_{0,g}$). In the following, the V_{oc} will be used as measure of the performance. The calculation of the V_{oc} is usually faster than of the efficiency, but there is not a fundamental obstacle in the method to calculate the efficiency.

Several models can be used to calculate the V_{oc} from a given dislocation map:

I. A heuristic model. Here a simple linear relation between the V_{oc} of wafer i and the fraction (f_i) of the surface area of wafer of that contains dislocations (bad area):

$$V_{oc,i} = af_i + b \qquad (1)$$

The parameters a and b are optimized for maximum correlation between experimental and calculated V_{oc} values.

II. An analytical model that uses the surface area averaged value

$$j_{0,i}^{av} = j_{0,g} \cdot (1 - f_i) + j_{0,b} \cdot f_i \qquad (2)$$

$$V_{oc,i} = \frac{kT}{q} ln\left(\frac{J_{SC}}{j_{0,i}^{av}} + 1\right) \qquad (3)$$

Here J_{SC} is a fixed value for the short-circuit current density. This method requires that at least $j_{0,b}$ is adapted for maximum correlation. J_{SC} and $j_{0,g}$ are selected such that they match the (extrapolated) V_{oc} of a cell without dislocations.

III. A numerical 2D model that links the spatial resolution of the dislocations to the localization of the metallization pattern. The metallization is represented by the 2D function $S(x,y)$, which has value zero inside the metallization and unity outside the metallization. The sheet conductance $\sigma(x,y)$ is calculated from the emitter sheet resistance R_e and the metallization sheet resistance R_m according to:

$$\sigma(x,y) = \frac{1}{R_e} S(x,y) + \frac{1}{R_m}\left(1 - S(x,y)\right) \qquad (4)$$

The local cell potential u can then be solved from the 2-D Poisson equation:

$$\nabla \cdot (-\sigma(x,y)\nabla u) = J_{ph} S(x,y) - j_0(x,y)\left(exp\frac{uq}{nkT} - 1\right) \qquad (5)$$

In eq. 5 the photon current density J_{ph} is a fixed value and $j_0(x,y)$ is equal to $j_{0,g}$ or to $j_{0,b}$, according to the location.

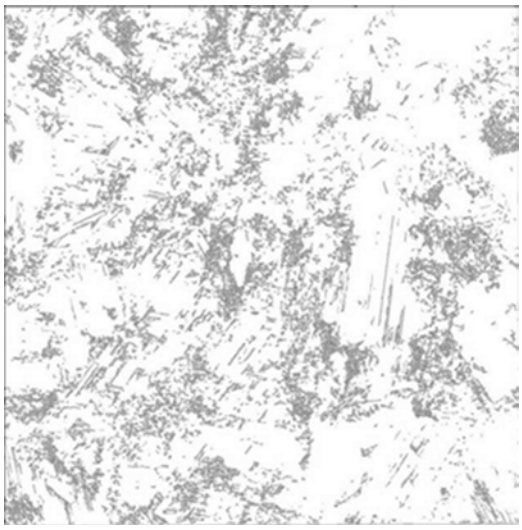

Figure 1: Processed image of a wafer

It is assumed that the busbars have a fixed potential, the applied cell voltage V_{cell}:

$$u\,|_{busbar} = V_{cell} \qquad (6)$$

At the edges of the cell the current (or the gradient in cell voltage normal to the edge) is zero:

$$\frac{\partial u}{\partial n}\,|_{edge} = 0 \qquad (7)$$

The 2D equation can be numerically solved with a Finite Element Method. The total cell current is the integral of the local generated current:

$$I = \int\int \left(J_{ph} S(x,y) - j_0(x,y)\left(exp\frac{uq}{nkT} - 1\right)\right) dxdy \qquad (8)$$

The V_{oc} is the cell voltage (potential at the busbars) for which $I = 0$. Again, at least $j_{0,b}$ is adapted for maximum correlation.

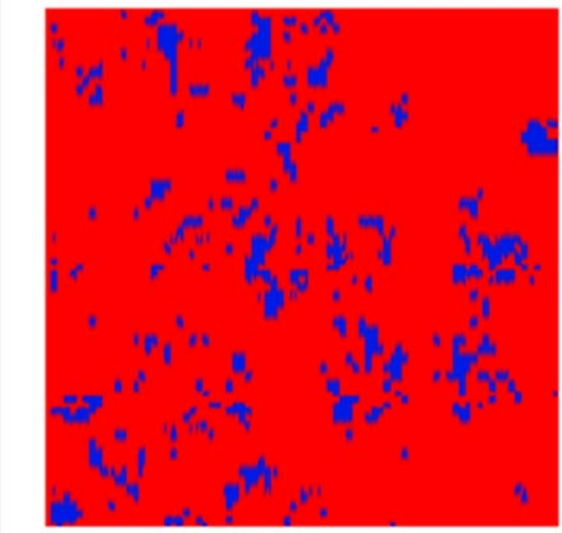

Figure 2: Binary map of dislocations

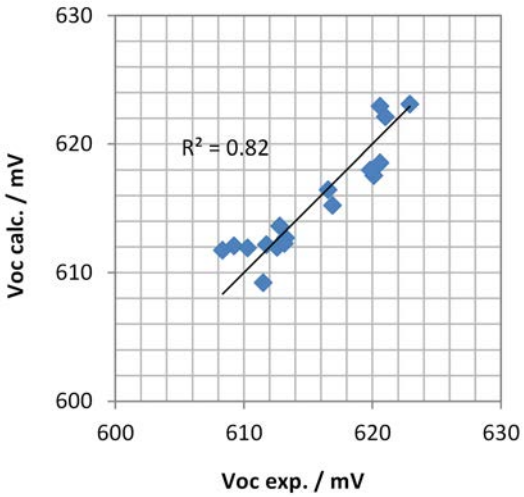

Figure 3: Experimental V_{oc} versus the calculated V_{oc} using method I

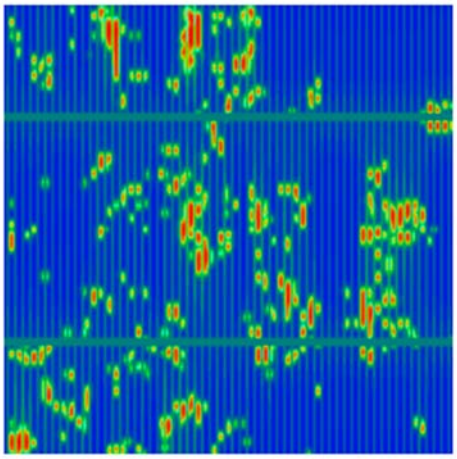

Figure 5: Distribution of the calculated cell potential at open circuit using the dislocation map from Figure 2. Blue: high values, red: low values

3 RESULTS AND DISCUSSION

3.1 The mapping of dislocations

Optical images (photocopies) were made of a set of multi-crystalline wafers, which had undergone the standard industrial acid etching for saw damage removal and iso-texturing. After digital processing a dislocation map as is shown in Figure 1 was obtained. The resulting "binary" map of good and bad areas is shown in Figure 2.

3.2 Performance prediction

In Method I two parameters (a and b) can be adjusted using a linear regression method. As Figure 3 shows, a good correlation between the calculated and experimental V_{oc} and can be found. This implies that surface area covered by dislocations is a good indicator for the resulting performance.

In Method II, only one parameter ($j_{0,b}$) is optimized in a least squares procedure, and still a good, but slightly poorer, correlation can be found as shown in Figure 4, where the calculated V_{oc} is shown versus the experimental value. The optimal $j_{0,b}$ was 5.5 times higher than $j_{0,g,}$

Method III explicitly uses the spatial resolution of the dislocations. As in method II, $j_{0,b}$ is the only parameter adapted. Figure 5 shows the distribution of the cell potential at open circuit condition, which reflects the dislocation map in Figure 2 as well as the metallization pattern. The inclusion of the spatially resolved information slightly improves the correlation between calculated and experimental data (Figures 5 and 6).The optimal $j_{0,b}$ values were very similar for both methods.

3.3 Effect of the position of dislocations

The position of dislocations may not always have a major impact, but it can be significant as the following analysis shows. Even in a solar cell made from a wafer with uniform quality the distributions of the local cell potential and generated current are not uniform. This is caused by the applied metallization pattern. The local cell potential increases with increasing distance from the metallization and the current may be zero or negative

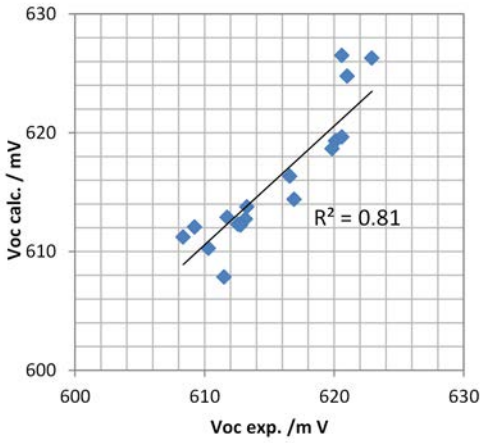

Figure 4: Experimental V_{oc} versus the calculated V_{oc} using method II

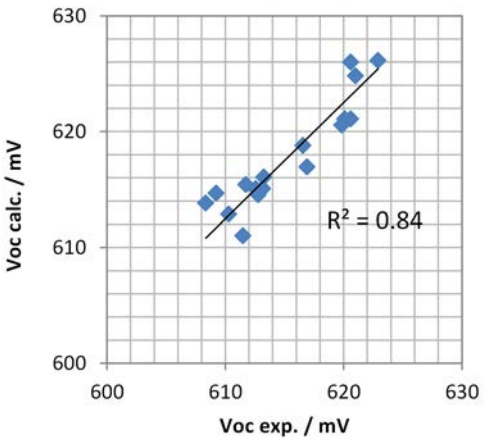

Figure 6: Experimental V_{oc} versus the calculated V_{oc} using method III

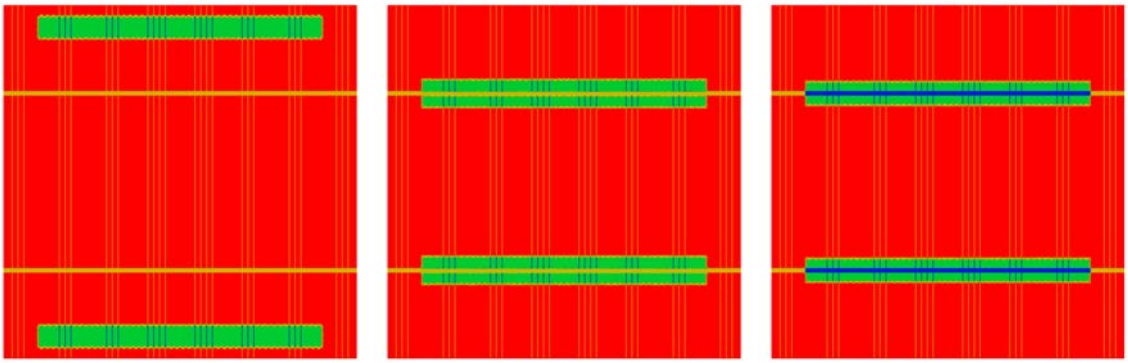

Figure 7: Diode maps of dislocation at different locations. Left: two separate areas close to the edges of the cell, center: four separate areas that are adjacent to the busbars but are not covered by them, and right: two separate areas that are partly (20%) covered by the busbars. Red: good area, green: dislocation, brown: metallization on good area, blue: metallization on dislocation. Due to limited resolution only some of the 60 fingers are visible.

(dissipated) at positions under the metallization.

The non-uniform potential affects the power output of dislocations. The intrinsic maximum power point (MPP) of a dislocation will occur at a lower cell voltage than the intrinsic MPP of the good area. At the MPP of the solar cell, the local cell potential at a dislocation will be a compromise between these two voltages. This means that the dislocations will operate beyond their intrinsic MPP, and that the deviation from their intrinsic MPP is largest in areas where the potential is highest. Therefore, dislocations far from the metallization will contribute less to the cell output than dislocations closer to the metallization. However, at dislocations under the metallization the current dissipation will be enhanced, and this reduces the overall cell output. So we may expect that the position where dislocations are least detrimental is close to the metallization but not right under the metallization.

2D FEM calculations confirm this picture. Three different configurations were examined, all having 10% dislocation or "bad" area. In a cell with a conventional H-metallization pattern the dislocations were chosen to be in 1) two separate areas close to the edges of the cell, 2) four separate areas that are adjacent to the busbars but are not covered by them, and 3) two separate areas that are partly (20%) covered by the busbars. Figure 7 shows the three corresponding dislocation maps with the metallization pattern. The calculated maximum power output as function of the parameter $j_{0,b}$ is displayed in Figure 8. The maximum power output decreases of course with increasing $j_{0,b}$. The power output is significantly lower when the dislocations are in the area of high cell potential, i.e. at the edges further from the busbars. Having 20% of the dislocation positioned under the busbar also has a negative effect on the cell output.

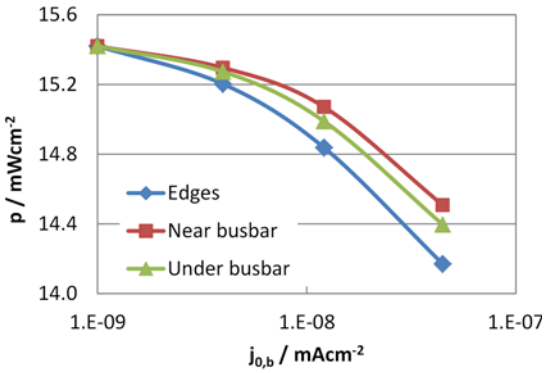

Figure 8: Maximum power output calculated with the 2D FEM model as a function of $j_{0,b}$ for three different distributions of 10% bad area. $j_{0,g}$ =10^{-9} mAcm^{-2}.

In the above three cases the position of the dislocations with respect to the metallization was pronouncedly different. Most multi-crystalline wafers will have a random distribution of dislocations. In the set of 17 wafers studied here, a 90^{o} rotation of the metallization pattern resulted in a maximum change in calculated V_{oc} of less than 2 mV or less than 0.02 % in absolute efficiency. However, for wafers with dislocations at more specific positions, the present method can be used to optimize the metallization either by a simple rotation of the wafer, or by adjusting the metallization pattern, e.g. the number of fingers.

4 CONCLUSIONS

A method to qualify multi-crystalline Si wafers by a very simple optical imaging was presented. The method does not require an additional dedicated etching but can be used with the industrial etching procedures isotexturing. The optical images are digitally processed and translated into dislocation maps which are fed into a performance prediction model. For a set of 17 multi-crystalline wafers, image processing parameters were investigated as well as various levels in the detail of the performance prediction model. This included full 2D simulations of a diode network with a spatial distribution of the dark saturation current density.

It was found that a simple model with a limited set of parameters was sufficient to correlate the performance of these multi-crystalline wafers with the maps of dislocation density, with an accuracy of a few mV in the V_{oc} value. The successful algorithms are computationally fast enough to meet the requirements for industrial applications.

Analytical and 2D FEM analyses showed that the performance is most of all determined by the fraction of

surface area of a wafer containing dislocations. However, some specific, non-random dislocation positions with respect to the metallization pattern can be more detrimental for the solar cell performance than others.

The method can be used for quality control, tailored processing, including metallization pattern optimization, and wafer rejection and classification in industrial solar cell manufacturing lines.

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REFERENCES

[1] B. Sopori, P. Rupnowski, S. Shet, V. Budhraja, N. Call, S. Johnston, M. Seacrist, G. Shi, J. Chen, and A. Deshpande, 35th IEEE Photovoltaic Specialists Conference (2010) 002233-002237.

[2] B. Sopori, P. Rupnowski, D. Guhabiswas, S. Devayajanam, S. Shet, C. P. Khattak, and M. Albert, 35 th IEEE Photovoltaic Specialists Conference (2010) 002238-002241.

[3] T. Trupke, J. Nyhus, and J. Haunschild, Phys.Status Solidi RRL 5 (2011) 131-137.

[4] J. Haunschild, M. Glatthaar, M. Demant, J. Nievendick, M. Motzko, S. Rein, and E. R. Weber, Solar Energy Materials and Solar Cells 94 (2010) 2007-2012.

[5] J. Haunschild, I. E. Reis, J. Geilker, and S. Rein, Phys.Status Solidi RRL 5 (2011) 199-201.

[6] S. Johnston, F. Yan, D. Dorn, K. Zaunbrecher, M. Al-Jassim, O. Sidelkheir, and K. Ounadjela, 38th IEEE Photovoltaic Specialists Conference (2012) in press.

[7] N. J. C. M. van der Borg, P. Manshanden, M. de Bruijne, G. J. M. Janssen, G. Coletti, and E. E. Bende, Dutch patent application 2007941 (2011).