EMITTER PERFORMANCE IMPROVEMENT OF MULTICRYSTALLINE SI SOLAR CELLS BY CONTROLLING THE N^{++} LAYER

Yuji Komatsu[1], John Anker[1], Henri Geerman[2], Peter Venema[2], and Arno F. Stassen[1]
[1]ECN Solar Energy, P.O. Box 1, NL-1755 ZG Petten, the Netherlands, Tel: +31 224 564303; Fax: +31 224 568214;
[2]Tempress Systems BV, Radeweg 31, NL-8171 MD Vaassen, the Netherlands,
Email: komatsu@ecn.nl

ABSTRACT: The phosphorus concentration in the n^{++} layer (top layer of a phosphorus emitter) was lowered by either thinning or thickening the phosphosilicate glass (PSG) film as the dopant source. Reducing the concentration by thickening the PSG combined with oxidation led to the improvement of the solar cell performance. Thinning the PSG by lowering the process temperature hardly showed positive effect. Reducing the sheet resistance from 66 ohm/square to 51-56 ohm/square by deepening the emitter depth itself and lowering the phosphorus concentration in the n^{++} layer resulted in a maximum efficiency gain of $0.3\%_{abs}$ for a uniform emitter structure. A selective emitter was fabricated through a process flow including two separate $POCl_3$ diffusion steps. Significant increase of Voc by 18 mV was obtained resulting in an average efficiency gain of $0.5\%_{abs}$ and the largest of $0.7\%_{abs}$ for the best cell. Our 2 × $POCl_3$ selective emitter process for multicrystalline silicon demonstrated the highest gain in efficiency and Voc, compared with to previously reported selective emitter approaches.
Keywords: Selective Emitter, Diffusion, Multicrystalline Silicon

1 INTRODUCTION

In most cases when a phosphorus emitter is formed by diffusion, the direct source to provide phosphorus atoms to crystalline silicon surface is a phosphosilicate glass (PSG) film [1]. Normally in industrial processing, PSG is saturated by phosphorus because uniform PSG can be easily obtained in a wide and tolerant process window by saturating the precursor for PSG when it is grown. Due to the larger solid solubility limit of phosphorus in PSG than that in crystalline silicon [1], the emitter surface near the PSG, or n^{++} layer as shown in Fig. 1, is over saturated and the excess phosphorus atoms are not electrically activated. These inactive phosphorus atoms cause lower operating voltage and smaller current since they behave as Shockley-Read-Hall (SRH) recombination centers [2]. Most attempts to improve the emitter performance have focused on reducing the excess phosphorus near the surface [3-9].

In this work, the reduction of the excess phosphorus in the n^{++} layer is attempted by thinning the PSG film by lowering the process temperature, or thickening it by combining with an oxidation process.

In addition, a selective emitter structure is fabricated by applying the optimized low-concentration n^{++} emitter with a process flow including two separate $POCl_3$ diffusion steps.

2 EXPERIMENT

Figure 1 shows the simplified model of the phosphorus doping profile of both emitter and PSG formed by diffusion. Besides the interface between PSG and emitter, two layers in the emitter are recognized, with the depth where the phosphorus concentration (N_P) is ~ 3×10^{19} cm^{-3} as the border [3]. Although the majority carrier concentration in the n^{++} layer cannot be higher than ~5×10^{20} cm^{-3} (which is formed at the typical process temperature for the emitter formation [3]), the surface N_P of the n^{++} layer is higher than that due to the over-supplied phosphorus from the PSG. In order to lower the N_P in the n^{++} layer, two different routes can be followed.

One is thinning the formed PSG film. During the $POCl_3$ diffusion process, phosphorus atoms are driven into silicon still after the supply of the $POCl_3$ gas is finished. Although the phosphorus is saturated in PSG while the $POCl_3$ gas is supplied, the grown PSG can be thinned by lowering the process temperature resulting in the slower growing speed, and the total amount of phosphorus fixed in the PSG can be physically reduced. If sufficiently long drive-in is followed, sheet resistance (R_{sheet}) can be tuned at the same level as the conventional process (60~66 ohm/square) while lowering the N_P in the n^{++} layer.

The other is thickening the PSG film by oxidizing it after the supply of the $POCl_3$ gas is finished. This measure is diluting the phosphorus concentration in the PSG film, and indirectly lowering the surface N_P of the n^{++} layer. It also enables to control the depth of n^{++} layer by including the n^{++} layer surface into the PSG.

The diffusion tool is an industry-scale $POCl_3$ tube furnace Tempress TS81003, equipped with 400 slots for loading 156×156 mm² wafers in its temperature flat zone. The doping profiles of the surface-polished wafers were characterized with secondary ion mass spectroscopy (SIMS).

156×156 mm² multicrystalline silicon (mc-Si) wafers were used for manufacturing solar cells and neighboring wafers were equally distributed to each experimental group. Except for the phosphorus diffusion process, all

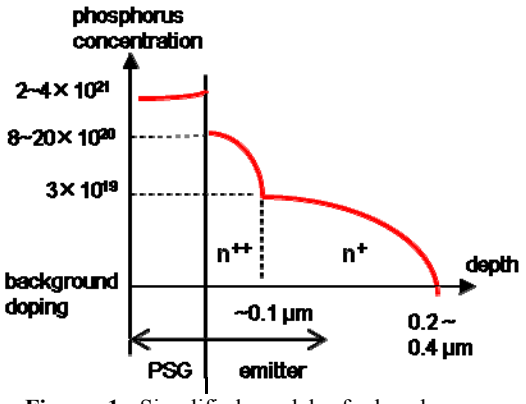

Figure 1: Simplified model of phosphorus doping profile of emitter and PSG, formed by diffusion process.

other process steps —such as texturing, SiN_x deposition, metallization, etc.— were the same for the uniform emitter process. The selective emitter process is described in section 3.4.

3 RESULTS AND DISCUSSION

3.1 Thinning PSG by lower process temperature

The surface N_P of the n^{++} layer was reduced while keeping R_{sheet} = 64 ~ 66 ohm/square. Three experiment groups were defined with different process temperature T_0 (reference), T_1, and T_2, where $T_0 > T_1 > T_2$. With keeping the $POCl_3$ supply time constant, the following drive-in time was tuned to obtain 64-66 ohm/square for all the groups. Figure 2 (a) and (b) show the doping profile characterized by SIMS of each group. Figure 2 (b) focuses on the n^{++} layer.

As seen in Fig. 2 (b), the phosphorus concentration in the n^{++} layer becomes a bit lower at $T = T_2$, while the profiles in n^+ are almost identical as shown in Fig. 2(a). The reduced N_P at the n^{++} layer does not change the R_{sheet} because the reduced phosphorus atoms are all electrically inactive.

Table I shows the average values of short circuit current (Isc), open circuit voltage (Voc), fill factor (FF) and the efficiency (η) with the standard deviations of the manufactured mc-Si solar cells of each group. The front contact metallization was optimized using the group of T_0.

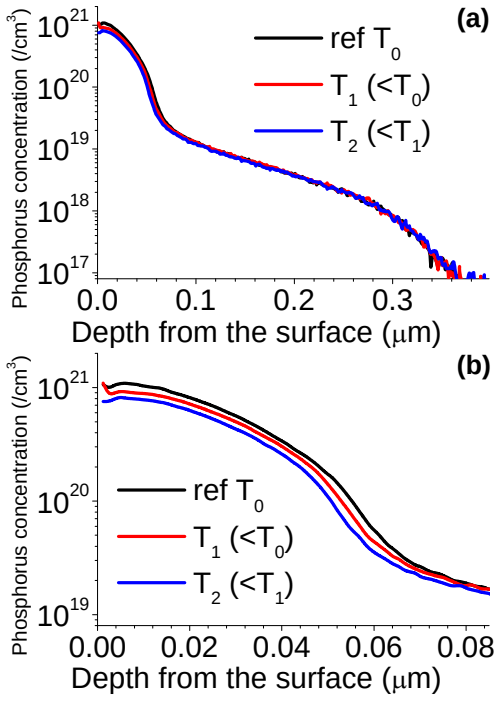

Figure 2: Phosphorus doping profiles of different process temperatures aiming at thinning PSG. (a) Both n^{++} and n^+ layers. (b) Focusing on n^{++} layer.

Table I: mc-Si solar cell properties of different process temperature groups aiming at thinning PSG.

process temp.	Isc (A)	Voc (mV)	FF (%)	η (%)
T_0 (ref)	8.35 ± 0.03	611 ± 1	77.1 ± 0.1	16.2 ± 0.1
T_1 (<T_0)	8.36 ± 0.04	611 ± 1	76.8 ± 0.2	16.1 ± 0.1
T_2 (<T_1)	8.41 ± 0.04	613 ± 1	76.0 ± 0.7	16.1 ± 0.2

The difference is hardly seen between T_0 and T_1 groups, but the T_2 group has a slightly higher Isc and Voc even with the small difference of the n^{++} doping profile seen in Fig. 2 (b). Separately optimizing metallization process of the T_2 group could result in a FF as high as that of T_0 (~77%) and an improvement in the efficiency.

The surface N_P of T_2 group, which is 8×10^{20} cm^{-3} and a bit lower than 1×10^{21} cm^{-3} of T_0 group, is still higher than the solid solubility limit at $T = T_2$ of phosphorus in silicon (~5×10^{20} cm^{-3}) [1]. A non-ignorable amount of electrically inactive phosphorus is still present in the n^{++} layer. A smaller amount of inactive phosphorus could be achieved by an even lower process temperature or shorter $POCl_3$ supply time resulting in thinner PSG, which can go outside the process window for growing a uniform PSG.

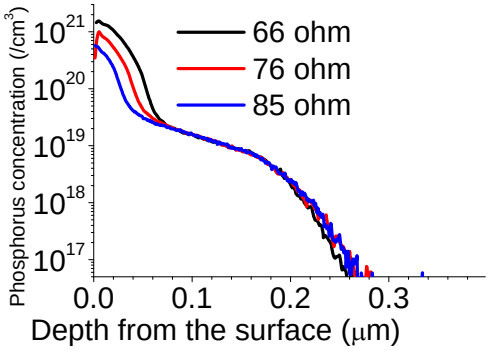

Figure 3: Phosphorus doping profiles of reference (conventional process) 66 ohm/sq., n^{++}-reduced 76 ohm/sq., and 85 ohm/sq. groups.

Table II: mc-Si solar cell properties attempting to reduce n^{++} layer while keeping n^+ layer by oxidizing PSG.

R_{sheet} (Ω/sq.)	Isc (A)	Voc (mV)	FF (%)	η (%)
66 ohm	8.36 ± 0.05	612 ± 1	77.6 ± 0.1	16.3 ± 0.1
76 ohm	8.46 ± 0.04	618 ± 1	77.0 ± 0.4	16.5 ± 0.1
85 ohm	8.56 ± 0.03	621 ± 1	72.8 ± 0.8	15.9 ± 0.2

3.2 Thickening PSG by combining oxidation (I)

In Fig. 3, the doping profile of the reference group with R_{sheet} of 66 ohm/square is displayed, accompanied by two other doping profiles with 76 and 85 ohm/square, respectively. The processes for these profiles were designed with the consideration to lower the peak N_P and thin the n^{++} layer while keeping the profile of the n^+ layer equivalent. This is done by oxidation of the PSG film after the PSG formation. The n^+ profiles of both the red and the blue curves exactly coincide with the reference black curve while peak N_Ps are lowered significantly and the n^{++} layers are thinned. Both the lower peak and the shallower depth of the n^{++} layer resulted in higher sheet resistance.

The average values of Isc, Voc, FF, and η of the manufactured mc-Si solar cells using the profiles depicted in Fig. 3 are shown in Table II. The improvement of Isc and Voc of both 76 and 85 ohm/square cells compared to the reference 66 ohm/square suggests that the electrically inactive phosphorus atoms in the n^{++} layer are reduced effectively

by means of the lower peak and the shallower layer. The average efficiency gain of the 76 ohm/square cells was 0.2%$_{abs}$.

In these experimental groups, the metallization process was optimized using the 85 ohm/square group, but the FF of 85 ohm/square cells went down remarkably while the decrease for 76 ohm/square cells was limited. This means the direction of reducing the n^{++} layer while keeping n^{+} layer hits the peak of efficiency at around the 76 ohm/square group. The doping profile of 85 ohm/square group shown in Fig. 3 looks promising because it hardly contains the layer with $N_P > 5\times10^{20}$ /cm^3, but it caused difficulty in making a good contact.

3.3 Thickening PSG by combining oxidation (II)

In order to improve the contact between metal and emitter from the previous section, we designed a diffusion process resulting in a peak N_P of the n^{++} layer comparable to the 85 ohm/square group, combined with a deeper n^{+} layer also by oxidizing the PSG. Figure 4 shows the representative 2 curves of 51 ohm/square and 56 ohm/square with the reference 66 ohm/square which is same as in Fig. 3. They show deeper n^{+} layers than the reference 66 ohm/square, resulting in a lower R_{sheet}. The impact of the lower peak concentration to R_{sheet} is limited because most of the reduced phosphorus atoms in the n^{++} layer are electrically inactive.

The average values of Isc, Voc, FF, and η of the mc-Si solar cells are shown in Table III. The 51 ohm/square cells show higher Voc and FF, resulting in 0.3%$_{abs}$ average efficiency gain. While the peak N_P of ~7×10^{20} cm^{-3} is comparable to T = T_2 in section 3.1, a larger Voc gain of 5 mV was obtained. The Voc gain is not only due to the reduction of the n^{++} layer but as well as due to the deepened n^{+} layer [5]. The region where N_P is no longer above 5×10^{20} cm^{-3} lies much deeper than for the 76 ohm/square emitter shown in Fig. 3, rendering a better contact for the Ag paste when it penetrates as deep as ~0.05 µm.

The 56 ohm/square cells (Fig. 4: blue) show an increase in both Isc and higher Voc compared to the 51 ohm/square cells, but due to the lower FF, they also result in a comparable 0.3%$_{abs}$ average efficiency gain. The depth tolerance where $N_P > 5\times10^{20}$ cm^{-3} is shallower than the 51 ohm/sq. cells (Fig. 4: red), but equivalent to the reference 66 ohm/sq. cells (Fig. 4: black), explaining why the FF is more comparable to the reference cells.

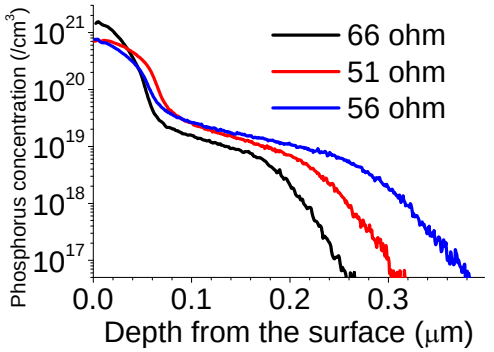

Figure 4: Phosphorus doping profiles of deepened-n^{+} 51 ohm/sq., and 56 ohm/sq., shown together with the reference 66 ohm/sq.

Table III: mc-Si solar cell properties attempting to reduce n^{++} layer and deepening n^{+} layer by oxidizing PSG.

R_{sheet} (Ω/sq.)	Isc (A)	Voc (mV)	FF (%)	η (%)
66 ohm	8.36 ± 0.05	612 ± 1	77.6 ± 0.1	16.3 ± 0.1
51 ohm	8.39 ± 0.03	617 ± 1	77.9 ± 0.2	16.6 ± 0.1
56 ohm	8.40 ± 0.04	619 ± 1	77.6 ± 0.2	16.6 ± 0.1

3.4 Selective emitter with 2 × $POCl_3$ process

Lowering the N_P in the n^{++} layer always results in reducing the process window for the subsequent metallization process as shown in section 3.2. The attempt described in section 3.3 looks promising to reduce the electrically inactive phosphorus while keeping a sufficient conductance with the metal contact, but the impact of Auger recombination is not ignorable where $N_P > 1\times10^{20}$ cm^{-3} [10] and the N_P in the n^{++} layer should still be lowered. Following the direction described in section 3.2 will enable further reduction of the n^{++} layer toward $N_P < 5\times10^{20}$ cm^{-3}. The contact problem should be overcome by selective emitter approach with combining heavily doped n^{++} layer just beneath the metal contact.

We designed and tested several process flows to implement the low N_P n^{++} layer described in section 3.2 into a selective emitter process. Figure 5 shows the processing path which recorded the highest device performance, comparing with the process flows of reference uniform emitter which are the industry standard [3] and the ECN Baseline [11]. The doping profile of the industry standard corresponds to any of the black curves of Figs. 2-4. This process flow includes two separate $POCl_3$ diffusion steps, which is unique compared to other industrialized process flows ever reported [6-9].

In this process flow, the area where no metal contact is designed to be printed upon is selectively etched by screen printable etching paste after the first $POCl_3$ diffusion. The etching depth is 0.2-0.4 µm, which is sufficient to remove the emitter layer formed by the first $POCl_3$ process and hardly damaging the anti-reflective quality of the textured surface. The border of the selectively etched area is clearly visible even after SiN_x is deposited.

Figure 6 shows the three-dimensional expression (3D) of R_{sheet} measured by four-point probe using Sherescan [12] near a busbar contact is crossing to a few

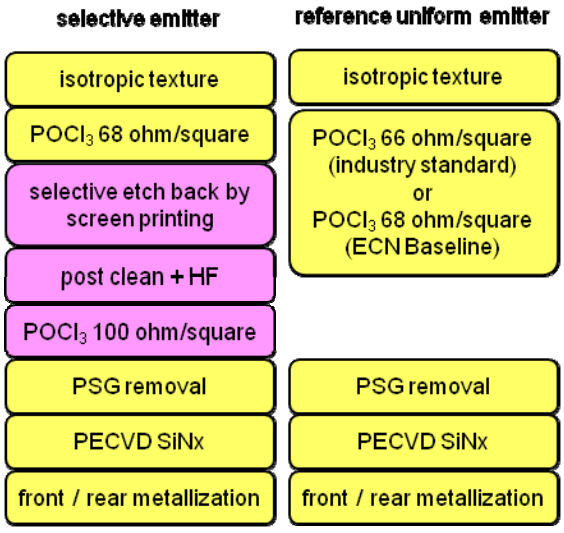

Figure 5: Process flow of the 2 × $POCl_3$ selective emitter comparing with the reference uniform emitter processes.

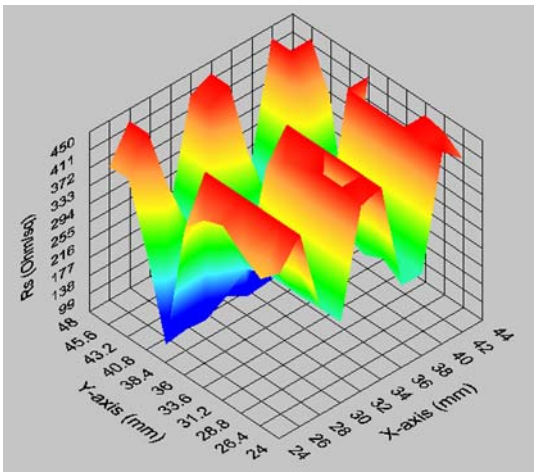

Figure 6: 3D expression of R_{sheet} near a busbar contact is crossing a few finger contacts after the post cleaning of the selective etching back.

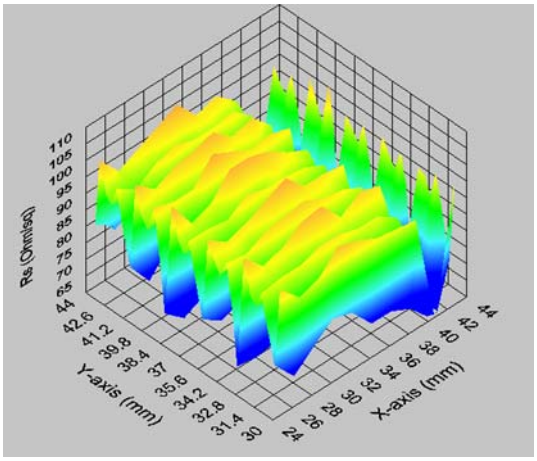

Figure 7: 3D expression of R_{sheet} after the second $POCl_3$ diffusion.

finger contacts after the post cleaning of the selective etching back. The measured minimum R_{sheet} is 75-80 ohm/square where the area is protected from the etching paste although the real value is difficult to identify due to the limited spatial resolution of four-point probe method. The etched area shows R_{sheet} > 300 ohm/square and difficult to identify p- or n-type, which suggests the most of the phosphorus-diffused layer was etched back from the surface.

Figure 7 shows the 3D of R_{sheet} after the second $POCl_3$ diffusion. The etched area shows 90-100 ohm/sq. and the protected area shows 58-65 ohm/sq. A reference wafer processed at the same time without any $POCl_3$ process beforehand also shows 96 ± 4 ohm/square, which suggests the first $POCl_3$ diffusion hardly influences the R_{sheet} after the second $POCl_3$ diffusion.

Table IV: mc-Si solar cells properties of selective emitter fabricated with two separate $POCl_3$ diffusion steps, comparing with the reference uniform emitter of industry standard and ECN Baseline. The property of the best cell is also shown.

	Isc (A)	Voc (mV)	FF (%)	η (%)
industry standard	8.51 ± 0.01	612 ± 1	77.6 ± 0.1	16.6 ± 0.1
ECN Baseline	8.53 ± 0.01	618 ± 1	77.2 ± 0.2	16.7 ± 0.0
selective (average)	8.64 ± 0.01	630 ± 1	76.6 ± 0.3	17.1 ± 0.1
selective (best)	8.64	631	77.0	17.3

Table IV summarizes the Isc, Voc, FF and η of the selective emitters both as the average values and of the best cell, comparing with the reference industry standard [3] and the ECN Baseline . Although the average FF loses $1\%_{abs}$ from the industry standard reference, $0.5\%_{abs}$ efficiency gain in average from the industry standard and $0.4\%_{abs}$ gain from the ECN Baseline [11] is achieved. The best cell whose FF is 77.0% has an efficiency gain as large as $0.7\%_{abs}$. Most significant is the 18 mV gain in Voc, which suggests lowering the N_P in the n^{++} layer successfully led to the reduction of not only inactive phosphorus atoms but also Auger recombination centers. If the first $POCl_3$ diffusion is optimized more appropriately, FF is expected to be improved to 77.0-77.5% in average, resulting in $0.7\text{-}0.8\%_{abs}$ efficiency gain.

Table V shows the comparison with other results of selective emitter approach reported as ever industrialized [6-9]. Our result of $0.5\%_{abs}$ efficiency gain is higher or equivalent to them, and Voc gain of 18 mV is quite significant. On the other hand, others reported larger efficiency gain for mono crystalline wafer like $0.5\text{-}1.0\%_{abs}$ than multi crystalline [6-8]. Although not explicitly described, all most likely use a thermal step with a process temperature higher than the typical $POCl_3$ process temperature for mc-Si. This might cause the deterioration of the bulk quality of mc-Si but not for mono.

Our 2 × $POCl_3$ process does not exceed the typical process temperature for mc-Si, therefore high Voc gain of 18 mV is achievable and more suitable for mc-Si process.

Table V: Comparison of several selective emitter approaches with their reference uniform emitter cells reported as ever industrialized [6-9] with our approach of 2 × $POCl_3$.

Apporach type	emitter	Jsc (mA/cm²)	Voc (mV)	FF (%)	η(%)	Gain	
emitter etch back [6]	ref.	33.1	612	78.2	16.0	Voc:	+ 5 mV
	selective	34.1	617	79.1	16.5	η:	$+ 0.5\%_{abs}$
finger n^{++} by laser doping [7]	ref.	34.0	615	78.8	16.5	Voc	+ 5 mV
	selective	34.4	620	78.2	16.7	η:	$+ 0.2\%_{abs}$
silicon ink [8,9]	ref.	34.0	618	79.0	16.6	Voc	+ 7 mV
	selective	34.9	625	77.8	17.0	η:	$+ 0.4\%_{abs}$
2 × $POCl_3$	**ref.**	**35.0**	**612**	**77.6**	**16.6**	**Voc**	**+ 18 mV**
	selective	**35.6**	**630**	**76.6**	**17.1**	**η:**	**+ $0.5\%_{abs}$**

4 CONCLUSION

By reducing the thickness of PSG film through lowering the process temperature without increasing R_{sheet}, the N_P in the n^{++} layer was slightly lowered until 8×10^{20} cm^{-3}, but the cell performance hardly improved. Thickening the PSG by combining oxidation successfully improved the cell performance. When R_{sheet} is increased to 76 ohm/square from 66 ohm/square by reducing the n^{++} layer while the n^{+} layer is kept equivalent, an efficiency gain by $0.2\%_{abs}$ was achieved with slightly lower FF. Further increase of R_{sheet} results in increases in Isc and Voc, but in a steep reduction of FF, ending up with a lower η. When R_{sheet} is decreased to 51-56 ohm/square by deepening the n^{+} layer while the peak N_P in the n^{++} layer is lowered down to 7×10^{20} cm^{-3}, an efficiency gain of $0.3\%_{abs}$ was achieved. The effective reduction of electrically inactive phosphorus atoms can lead to the cell performance improvement for uniform emitter structure without sacrificing the conductivity between the metal and the emitter.

Further n^{++} layer improvement by reducing the Auger recombination center requires a selective emitter structure. An unique process flow including two times of $POCl_3$ diffusion was introduced to implement the low N_P n^{++} layer into a selective emitter process. An average efficiency gain of $0.5\%_{abs}$ with 18 mV increase of Voc was obtained, and the best cell achieved a $0.7\%_{abs}$ efficiency gain. In comparison with other approaches for selective emitter previously reported as ever industrialized, our 2 × $POCl_3$ process demonstrated the highest gain in η and Voc for a mc-Si selective emitter process.

ACKNOWLEDGEMENT

This work was partly funded by the Dutch Ministry of Economic Affairs, Agriculture and Innovation.

REFERENCES

[1] S.M. Sze, *VLSI technology*, McGraw-Hill, 2nd ed., New York, 1988.

[2] S.M. Sze, *Physics of Semiconductor Devices*, John Wiley & Sons, 2nd ed., New York, 1981.

[3] Y. Komatsu, G. Galbiati, M. Lamers, P. Venema, M. Harris, A.F. Stassen, C. Meyer, M. van den Donker, A. Weeber, *24th EU-Photovoltaic Solar Energy Conference*, Hamburg 2009, 1063-7.

[4] Y. Komatsu, A.F. Stassen, P. Venema, A.H.G. Vlooswijk, C. Meyer, M. Koorn, *25th EU-Photovoltaic Solar Energy Conference*, Valencia 2010, 1924-9.

[5] Y. Komatsu, M. Koorn, A.H.G. Vlooswijk, P.R. Venema, A.F. Stassen, *1st Int'l Conference on Silicon Photovoltaics*, Freiburg 2011.

[6] B. Raabe, F. Book, A. Dastgheib-Shirazi, G. Hahn, *25th EU-Photovoltaic Solar Energy Conference*, Valencia 2010, pp. 1174-1178.

[7] T. Frieß, A. Teppe, J. Olkowska-Oetzel, W. Zimmermann, C. Voyer, A. Esturo-Bretón, J. Isenberg, S. Keller, D. Hammer, M. Schmidt, P. Fath, *25th EU-Photovoltaic Solar Energy Conference*, Valencia 2010, pp. 2164-2167

[8] M. Abbott, D. Poplavskyy, G. Scardera, E. Rosenfeld, X. Chen, M. Terry, S.W. Johnson F. Lemmi, *25th EU-Photovoltaic Solar Energy Conference*, Valencia 2010, pp. 2412-2415

[9] D. Poplavskyy, G. Scardera, M. Abbott, A. Meisel, X. Chen, S. Shah, E. Tai, M. Terry, F. Lemmi, *25th EU-Photovoltaic Solar Energy Conference*, Valencia 2010, pp. 2416-2419

[10] M.S. Tyagi, R. van Overstraeten, *Solid-State Electronics*, 1983, **26**, 577-97

[11] A.F. Stassen, J. Anker, P. Danzl, Y. Komatsu, M Koppes, and E. Kossen, *25th EU-Photovoltaic Solar Energy Conference*, Valencia 2010, pp. 1939-1941

[12] http://www.sunlab.nl