

HOW TO IMPROVE A MULTICRYSTALLINE SOLAR CELL PROCESS WITH MORE THAN ONE PERCENTAGE POINT RESULTING IN AN AVERAGE CELL EFFICIENCY OF 17.2%

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ABSTRACT: By replacing critical solar cell processing steps and optimizing the total process we succeeded in increasing the average cell efficiency by almost 1.5% to 17.2% with a maximum cell efficiency of 17.3%. This improvement is obtained by using industrial processes and equipment. Changes in the processing flow were: tube diffusion instead of inline diffusion, single side etch instead of laser isolation, optimized screen designs for the backside and double print for the front side grid. The most important factor for the increase in cell efficiency was integration of individual process steps into a balanced cell production process.

Keywords: Multicrystalline, Silicon, Solar Cell Efficiencies

1 INTRODUCTION

Currently, the demand for higher cell and module efficiencies is very strong to achieve PV system cost reduction. One way is to replace existing lines for new, ‘state of the art’ lines provided by turnkey suppliers. Another option is to improve the production process by changing or adapting individual production steps, while keeping the majority of the line intact.

The standard baseline process at ECN is characterized as an industrial solar cell fabrication process for multicrystalline silicon wafers. In 2008, we manufactured solar cells with an average efficiency of 15.8% on 156 x 156 mm² [1, 2].

By updating the process parameters, introducing new or improved production steps and continuously tuning of the complete manufacturing process, we succeeded in increasing the average cell efficiency on comparable material quality to 17.2% with top cells of 17.3%. The improved process flow only contains steps and equipment that are already widely used in industry.

2 APPROACH

Neighboring groups of multicrystalline wafers were preselected using a complete, p-type commercial ingot block. In this way over 25 comparable groups have been selected, all with comparable material quality. This also means that the results are representative for this whole block.

For each process step we investigated whether alternative industrial processes resulted in a higher efficiency, higher stability or lower cost. These alternatives are directly compared on neighboring groups of wafers and optimized for the existing process flow.

Changes were made in junction isolation, emitter formation, post-emitter clean, metal pastes and metallization technique. Changes were implemented over a 18 month period (see figure. 1 and 3). All process steps have been optimized for optimum cell efficiency and for stable processing.

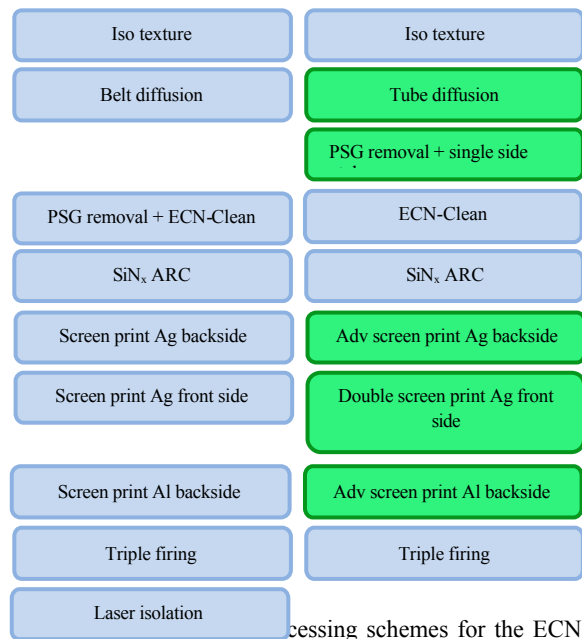


Figure 1: Comparison of processing schemes for the ECN baseline process.

3 RESULTS

3.1 diffusion

Integration of a process in the complete process flow is critical. As example, initially a standard industrial single temperature plateau tube furnace diffusion based on POC₃ as phosphor precursor was tested. From previous results it was known that in combination with laser isolation this emitter would result in an increase in J_{sc}, Voc and FF compared to the standard inline emitter [3].

Table I: tube furnace emitter results in loss in fill factor due to non-optimal integration with complete process flow

	Jsc (mA/cm ²)	Voc (mV)	FF (%)	Eta (%)
Inline	33.8	609	76.1	15.7
tube	34.2	617	74.4	15.7
diff	+0.9%	+1.3%	-2.2%	-0.0%

But in combination with our single side etch process, the emitter was damaged and the gain in J_{sc} and V_{oc} was completely compensated by the loss in FF (table I).

Optimizing the combined process of diffusion and single side etch isolation resulted in a tube furnace process with a multi-plateau temperature profile [3].

In a new comparison where all processing, except the diffusion process step, was identical, a clear improvement is observed going from inline diffusion based on spraying of a H_3PO_4 solution to a tube furnace process based on gaseous $POCl_3$. Gains are in J_{sc} , V_{oc} and fill factor, resulting in a total increase in cell efficiency of 0.3% point (table II).

Table II: difference in efficiency between inline and tube diffusion

	J_{sc} (mA/cm ²)	V_{oc} (mV)	FF (%)	Eff (%)
inline	34.2	611	77.7	16.2
tube	34.4	615	77.9	16.5
diff	+0.7%	+0.7%	+0.3%	+1.7%

3.2 isolation

Junction isolation by laser 200 μ m from the edge reduces the effective surface area of the solar cell by 0.6% and the expected cell efficiency by ~0.1% point. By removing the emitter from the backside by wet chemical etching, the total front area can be used for light collection.

A drawback of single side etching is that the etchant can creep to the front side due to the hydrophilic nature of the PSG. By removing the PSG before the SSE, this can be prevented. A drawback is that the PSG is no longer acting as protecting layer and the emitter is etched by the vapors formed during the etching of the backside. This front side etching can be limited by adjusting the conditions in the wetbench during the etching process. The increase in sheet resistance can be reduced by adjusting the diffusion process.

Table III shows that the gain in efficiency is not only due to an increase in J_{sc} . The controlled etching of the front side results in an increase in V_{oc} of 4 mV.

Table III: increase in efficiency due to single side etch isolation

	J_{sc} (mA/cm ²)	V_{oc} (mV)	FF (%)	η (%)
reference	33.0	608	77.3	15.5
SSE	33.4	612	77.1	15.8
diff	+1.2%	+0.7	-0.3	+1.5

3.3 screen print front

By reducing the metal coverage on the front-side, the amount of light absorbed by the solar cell is increased, resulting in a higher J_{sc} . One method to reduce the metal coverage is by printing narrower fingers. Without changing the aspect ratio between width and height the reduction in conductivity would result in a reduction in fill factor and therefore efficiency.

By printing two lines on top of each other ("double-print"), it was possible to reduce the metal line width from

130 to 90 μ m (see figure 2) and metal coverage from 7.3% to 5.8%. This is accomplished without reducing the cross section and even reducing the busbar to busbar resistance from an average of 24 m Ω to 16 m Ω . The efficiency gain is due to both increases in increase in J_{sc} and FF (see table IV).

Table IV: increase in efficiency due to double screen print

	J_{sc} (mA/cm ²)	V_{oc} (mV)	FF (%)	Eff (%)
single	34.5	613	76.2	16.1
double	34.9	613	77.4	16.6
diff	+1.1%	+0.0%	+1.7%	+2.8%

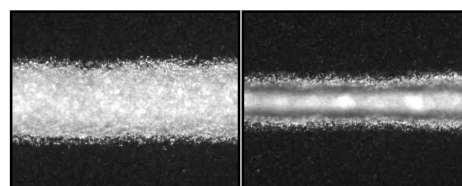


Figure 2, left: single screen print, right: double screen print

3.4 screen print back side

Reducing the area of the silver contact pads on the backside of the wafer results in an increase in the surface of BSF and a reduction in silver usage. The original 12 pads (six for each busbar) were 5x10 mm and has a combined weight (wet) of 110 mg. The new pads are 3x5 mm and only 30 mg of paste is used. This is a reduction of 75%.

3.5 final processing

The final processing flow for the high efficiency process is as described in figure 1. All processes are already in use in industry. Average cell results and the results of the best cell are given in table V.

Table V: average and best cell efficiencies of the ECN baseline process

	J_{sc} (mA/cm ²)	V_{oc} (mV)	FF (%)	η (%)
average	35.3	621	78.5	17.2
Best cell	35.4	622	78.6	17.3

4 DISCUSSION

By gradually updating and adjusting process steps we succeeded in increasing the average efficiency from 15.8% to over 17.2% (see figure 3) using only industrially available processes. All new process steps have to be tested in direct comparison with the standard processing and when needed adjusted for this processing in order to obtain the highest efficiencies.

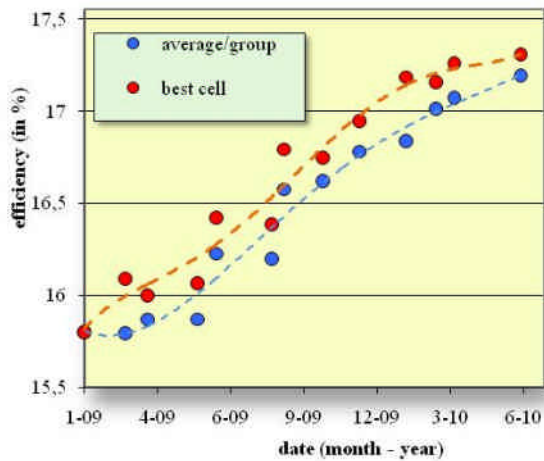


Figure 3: increase in average and maximum efficiency in between January 2009 and June 2010.

5 ACKNOWLEDGEMENTS

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6 REFERENCES

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