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HIGH EFFICIENCY N-TYPE METAL WRAP THROUGH SI SOLAR CELLS FOR LOW-COST INDUSTRIAL PRODUCTION

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ABSTRACT: A high-efficiency industrial cell process for n-type wafers using the conventional H-pattern front contact grid has recently become available. Based on simple industrial process steps, production of low-cost n-type cells has become a real possibility. In order to further reduce processing costs and increase module efficiencies, we have combined the strength of the n-type doped crystalline silicon with ECN's metallisation-wrap-through (MWT) solar cell concept, on n-type silicon wafers. As in p-type MWT (PUM) cells, the processing modifications from H-pattern to MWT are very limited. These cells were manufactured using a process similar to the industrial processes used for n-type H-pattern cells, extended with via-hole drilling. We have measured unconfirmed peak efficiencies of 18.7% on 156mm semi-square CZ n-type wafers (238 cm²). We have observed part of the expected current increase compared to the H-pattern grid. The fill factor needs to be further improved to realize the expected significantly higher efficiencies than for front contact cells.

Keywords: n-type, C-Si, back contact, metal wrap through, high efficiency

1 INTRODUCTION

The majority of solar cell production is presently based on p-type crystalline silicon wafers using a very mature technology. However, to improve competitiveness with other energy sources, wafer-based solar cell manufacturers, in cooperation with researchers, have to focus on the development of a low-cost (cost/Wp) technology to produce higher efficiency devices, preferably combined with lower use of resources and improved environmental footprint. N-type silicon solar cells represent an alternative to the traditional p-type silicon solar cells which, in combination with back-contacted cell technology like the Metal-Wrap-Through (MWT) concept [1], can potentially fulfil this objective with only modest changes to the current wafer and cell production processes. Research and development on solar cells using n-type Si substrates and low-cost screen-printed processing has become active in the last 4-5 years. A high-efficiency industrial cell process for n-type wafers using the conventional H-pattern cell concept has recently become available through ECN [2].

The use of n-type material has several advantages over the use of p-type. Firstly, n-type silicon has been proven to have a higher tolerance to common transition metal impurities, such as those present in silicon produced from quartz and carbon [3,4,5]. Thanks to this feature, n-type material could have a higher tolerance for lower-quality feedstock [6,7]. Also, after gettering and passivation, higher minority carrier diffusion lengths have been observed for n-type material. Secondly, in n-type material boron-oxygen complexes are absent. Therefore it will not suffer from Light Induced Degradation (LID) [8,9].

In parallel to the significant progression of the n-type base silicon solar cell technology, there is much interest in processing back-contacted solar cells for further efficiency improvement. ECN's MWT technology presents several advantages over the standard H-pattern cells concept. In addition to a current gain due to reduced front-side metallization coverage and easier implementation in the module as the cell is fully back-contacted (higher packing density and less breakage and less resistance losses), higher fill factor for larger cells can be obtained thanks to a small unit cell design.

Also, the MWT cell concept presents certain advantages over other high efficiency cell structures such as, for example, Interdigitated Back-Contacted (IBC) or Heterojunction with Intrinsic Thin-layer (HIT) cell concepts. These two concepts require high quality silicon material, and in addition the IBC concept requires high alignment accuracy of the metal contacts on the back. In contrast, The MWT cell structure comprises a front side emitter and therefore will be less sensitive to material quality variations. Also, the simplicity of the rear-side contact pattern allows large flexibility regarding alignment of the prints.

In order to further lower processing costs and increase module efficiencies, we have combined the strength of the n-type doped crystalline silicon with the development of our MWT solar cell concept.

In this paper, results from a simple process designed for high-efficiency n-type MWT crystalline silicon solar cells, comparable to the industrial processes used for n-type H-pattern front contact cells, will be presented with cell characterisation results. Cell efficiencies up to 18.7% on large area wafers and possible improvements will be discussed.

2 ECN's MWT CONCEPT ADAPTED TO N-TYPE CRYSTALLINE SILICON MATERIAL

In order to keep future production costs as low as possible, the process under investigation is very similar to our industrial processes used for n-type H-pattern cells. Laser processing is used to form via-holes by which the front side metal grid will be wrapped through the wafer. Like the n-type H-pattern cells, the cell structure comprises a boron emitter and an open rear side metallisation suitable for thin wafers. The passivation process of the highly-doped boron emitter uses industrial

equipment and provides on industrial emitters an excellent passivation quality. Metallization is applied using screen-printing and is fired through the passivating layers.

Only basic process steps that are used in industrial cell processes are applied: laser drilling, texturing, diffusion, passivation, SiN_x anti-reflective coating (ARC), metallisation, firing. The processing scheme to make n-type MWT silicon solar cells is illustrated in figure 1

Figure 1: Process scheme of n-type MWT silicon solar cells.

The printing process of the metal contacts, based on conventional screen printing, is very similar to the printing process used in the n-type H-pattern industrial process and has no further requirements regarding alignment. The contacts are formed during a co-firing step. The front side metal grid pattern is based on the PUM concept designed to significantly reduce metal coverage and series resistance losses [10]. The total metallisation related losses are 3-4% less than the total metallisation related losses of a conventional H-pattern grid design. On p-type MWT cells (PUM), it has been demonstrated that the PUM metal grid design leads to a 2% relative gain in short-circuit current compared to a conventional p-type H-pattern cells (2 busbars) [11]. The rear side metallization has an open structure which improves the internal quantum efficiency in the long wavelength and enhances the internal reflection. As a consequence, current and voltage are enhanced compared to cell structures comprising a full aluminium back surface field. Also, at module level, an open rear side metallisation can increase the annual energy yield by employing bifacial modules.

The front and rear sides of the cells made according to this process sequence can be seen in Figure 2.

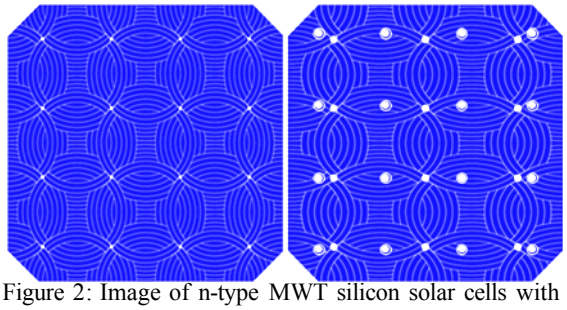

Figure 2: Image of n-type MWT silicon solar cells with the ECN unit cell design: front side (left picture) and rear side (right picture). The particular unit cell pattern shown is an example and can be varied.

3 RESULTS AND DISCUSSION

Cells were prepared from 200 µm thin n-type Cz wafers (238 cm²) according to the process described above. Random pyramid texture is formed by alkaline etching. The characterisation of the cells was carried out at ECN and the I/V results are shown in table I.

20 cells	J_{SC} (mA/cm²)	V_{OC} (mV)	*FF*	η (%)	*Rse* (Ω)
Average	38	636	.765	18.5	$6.4E^{-3}$
Best cell η	38.3	638	.766	**18.7**	$6.2E^{-3}$

Table I: I/V characteristics of n-type MWT cells measured at ECN (Rse obtained from a fit to the 2nd diode model)

The average current density (Jsc) value reaches 38.0 mA/cm² which already outperforms Jsc measured on H-pattern cells manufactured with the corresponding process [12]. The highest current density measured so far approaches 38.3 mA/cm². Open-circuit voltage (Voc) measured on n-type MWT cells is comparable to n-type H-pattern cells. However, a Voc increase is expected as contacts-related recombination should be reduced due to lower metallisation coverage. Series resistance is, in these initial test results, higher than series resistance measured on n-type H-pattern cells. Correspondingly, fill factor (FF) values so far are relatively low which significantly limits cell efficiency.

4 POTENTIAL FOR FURTHER IMPROVEMENT

According to I/V parameters presented in table I, at the moment, fill factor and series resistance are the main limiting factors to overall performance of n-type MWT solar cells. By improving front and rear side metal grid design and metal paste properties, series resistance and current are expected to be significantly improved and typical FF values of H-pattern cells should be reached. Figure 3 illustrates that for optimal metallisation pattern a slight improvement of Rseries is expected.

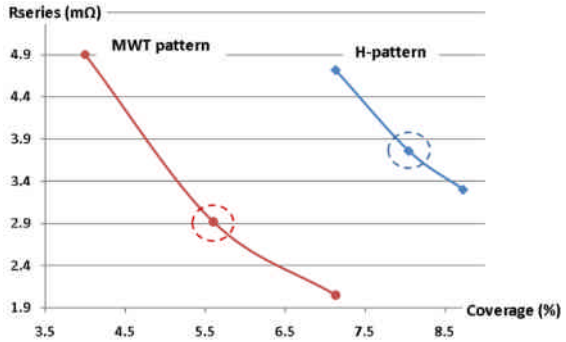

Figure 3: Calculation of Rseries versus shadow loss for H-pattern (2 busbars) and MWT cells with same characteristic properties of front side metallisation.

For optimal metallisation coverage, marked in figure 3 by dashed circles for both types of patterns, the Rseries is 15% lower for the MWT cell leading to a FF gain of 0.9%. The series resistance difference shown is calculated for a specific case and will be dependent on grid pattern and metal paste properties optimisation. The main advantage of the MWT cell remains in the improved shadow loss as shown in the figure 3. In this specific case, the shadow loss reduction results in a 2.5% Jsc gain.

5 CONCLUSION

We have developed metal-wrap-through (MWT) silicon solar cells on n-type monocrystalline Czochralski (Cz) silicon wafers, leading to high efficiencies. Based on industrial cell processes including screen-printed metallization, we have reached 18.7% cell efficiency, measured at ECN, on large area wafers (238 cm²), with clear potential for further improvement. Simple optimisations regarding metallisation (metal grid design and paste properties) are expected to boost the efficiency. Overall, by process and material optimization efficiencies higher than 19% are certainly within reach. To our knowledge this is the first demonstration of an industrial low-cost and high-efficiency n-type back-contact cell process suitable for mono-crystalline as well as multi-crystalline silicon wafers with a large quality range.

6 ACKNOWLEDGEMENTS

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