WAFER-BASED CRYSTALLINE SILICON MODULES AT 1 €/WP: FINAL RESULTS FROM THE CRYSTALCLEAR INTEGRATED PROJECT

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ABSTRACT: CrystalClear was an EU co-financed Integrated Project aimed at developing technology for wafer-based silicon solar modules at 1 € per watt-peak manufacturing costs and a strongly improved environmental profile. The project consortium has selected a number of technologies that potentially comply with these aims as well as research that serves as basis for further developments (beyond the project aims). These technologies have been demonstrated in the form of demonstrators, i.e. full-size modules featuring all innovations necessary to comply with the aims. The project has shown that wafer-based multicrystalline-silicon solar modules can be produced at 1 € per watt-peak at a world-record efficiency of 16% and an energy pay-back time of less than 2 years in Southern Europe.
Keywords: back contact, c-Si, cost reduction, manufacturing and processing, module manufacturing, multicrystalline silicon, silicon solar cell, LCA, energy pay-back time.

1 GENERAL PROJECT OVERVIEW

CrystalClear [1-4] was a 5½-year Integrated Project carried out in the 6th Framework Program of the EU. It started in January 2004 and was finished in June 2009. The project was a joint effort of a consortium of 16 European companies, research institutes and university groups involved in wafer-based crystalline silicon PV technology.
Companies: BP Solar (ES), Deutsche Cell (DE), Deutsche Solar (DE), Isofotón (ES), Photowatt (FR), REC (NO), REC Wafer Norway (NO), SCHOTT Solar (DE), SolarWorld Industries (DE).
Universities: Utrecht (NL), Konstanz (DE), UPM-IES (ES);
Research institutes: InESS-CNRS (FR), ECN (NL, project coordinator), FhG-ISE (DE), IMEC (BE).

Within CrystalClear an average of over 50 researchers from 6 European countries have worked together.

The project aims have been divided in three main blocks.
1. Availability of innovative manufacturing technologies which allow solar modules to be produced at a cost of 1 €/watt-peak (which is a reduction by more than 50% compared to state-of-the-art at the start of the project). This objective is very ambitious, but essential to get world-class technology. Manufacturing cost reduction is essential to bring prices of modules and turn-key complete systems down.
2. Improved environmental profile of solar modules by reduction of materials consumption, replacement of undesired materials and designing for recycling. This will strengthen the position of solar energy as a clean and sustainable alternative to conventional electricity generation.
3. Enhanced applicability of modules by tailoring to customer needs and by improving product lifetime and reliability. Since solar modules will be used in very different situations (e.g. on buildings) flexibility of use is crucial. Assured quality is a prerequisite for large-scale, professional use.

The CrystalClear project has tackled all aspects from the raw materials up to the completed solar module. Key activities concerned:
- strongly reducing the consumption of expensive materials (especially silicon, but also others) as well as introducing the use of cheaper materials;
- increasing the electricity output of solar modules;
- developing highly automated, high-throughput, low-cost manufacturing processes;
- screening materials, processes and products in relation to sustainability and suitability for large-scale use.

Since many combinations of options for cell and module design, processing and materials potentially fulfill the project aims, a selection of 6 distinctly different overall technologies has been developed, underlining the many faces of wafer-based silicon PV and the variety of approaches found within the industry. The feasibility of these technologies to comply with the projects aims has been verified by detailed cost and environmental analyses. CrystalClear has chosen technologies which might be demonstrated as full-scale modules already at the end of the project as well as technologies which still need to be developed further after the project.

The project has been organized in Subprojects (SPs), covering the parts of the value chain as well as integrating aspects (environmental analyses, cost calculations, etc.), see Figure 1. In the following, the final project results achieved are summarized per Subproject:

1. Feedstock;
2. Wafers;
3. Wafer-equivalent approaches;
4. Cells;
5. Modules;
6. Environmental sustainability;
7. Integration.

This summary is based on the official Public Project Summary that was published on the occasion of the Project Final Event. A list of project publications providing more, and more detailed information is available on the project website [5].

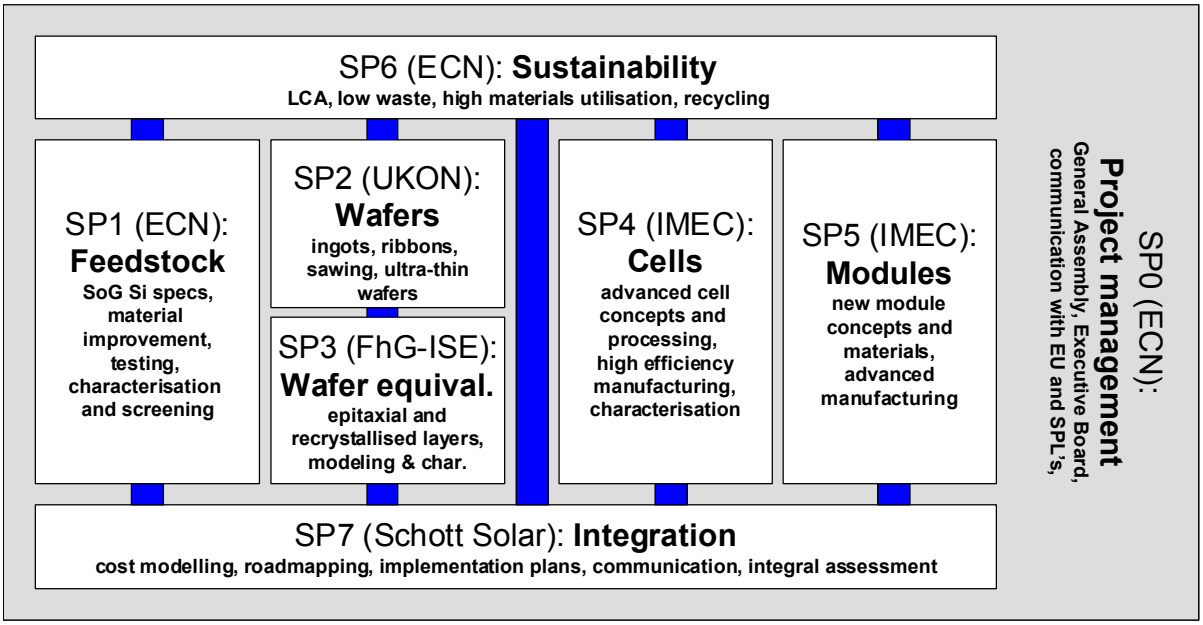

Figure 1: CrystalClear project structure, Subprojects (SP) with responsible partner, and main research topics.

2 PROJECT RESULTS SUMMARISED

2.1 Feedstock

Among all Subprojects of the CrystalClear project, SP1 (feedstock) is probably the one for which the business environment has gone through the most dramatic changes in the span of the 7 years from the planning to the project conclusion.

At the time of planning (2002-2003), the PV market was strongly growing, but it was still much below the GW size, silicon consumption was significantly lower than the polysilicon installed production capacity, semiconductor market was weak, feedstock had been predominantly made of reclaims from semiconductor industry and virgin polysilicon had just started to be extensively mixed as a supplement to the reclaims. Silicon was affordable at a price in average below 20 US$/kg, virgin polysilicon specifically made for solar or not was traded at just above 20 $/kg.

A major shift occurred during 2004 a few months after the official kick-off of CrystalClear. Because of a strong concomitant demand from both semiconductor and PV industry offer and demand of polysilicon appeared quite in balance and it became more evident – although not for everyone - that a potential shortage of silicon feedstock might occur in a near future. Polysilicon prices strengthened and recovered levels as of before the last downturn of 1998. But silicon remained still both available and affordable.

Boosted by the remarkable growth of the PV industry silicon demand continued to increase. At the midterm assessment of the CrystalClear program in June 2006, shortage had become a reality and that year the consumption of virgin polysilicon by the solar industry sector was for the first time equivalent or had even surpassed the consumption by the semiconductor market. Both the polysilicon and the PV industry had to face this historical shift and measure the consequences of it. That triggered numerous initiatives on both immediate expansions and accelerated R&D projects on new solar grade (SoG) silicon processes. Beside polysilicon, upgraded metallurgical silicon (UMG-Si) became more widely and seriously considered as a long term solution. In addition to that, other forms of SoG silicon have been investigated as alternatives. Meantime, silicon prices had started escalating.

This trend continued until the 4th quarter of 2008, when the world wide financial crisis hit all sectors of the world's economy, semiconductor, PV and silicon industry included. The following slowdown in the PV activities reflected in the trade of modules and other materials. A useful indicator is the spot price of polysilicon which was down to 120-150 $/kg in March 2009.

In the following we will focus on the learning by the industry from the SP1 activities. We will also enlighten why and how the goals and priorities had to be changed in the course of the program.

2.1.1 Goals

The goals of SP1 were twofold:

- to assess new feedstock materials, which were supposed to soon come onto the market;
- to assess the role and the limit acceptable for various frequent impurities, as it was assumed that new silicon sources may include higher concentrations than virgin polysilicon.

To develop new silicon processes was not a goal; at the time of planning several companies and research groups were strongly involved in proprietary confidential projects and it was assumed that new materials were just about to emerge and enter into the commercialization phase.

The methodology chosen was:
- produce ingots from baseline-, new- and synthetic- (virgin polysilicon contaminated on purpose by a controlled level of impurity) feedstock;
- make wafers and cells from ingots according to a standard defined procedure;
- characterize wafers and cells by all chemical and physical methods available to the consortium.

2.1.2 Results and learning

2.1.2.1 New feedstock candidates: selection, acquisition

Several new types of feedstock were about to emerge. It was mainly granular polysilicon made by the Fluidised Bed Reactor (FBR) technique for the thermal decomposition of silane (REC) or chlorosilane (Wacker), instead of hot filament deposition as in the conventional Siemens reactor. Another interesting process was the Vapour-to-Liquid Deposition process of Tokuyama, in which chlorosilane is decomposed at higher temperature on a liquid surface of silicon. Free Space Reactor (FSR) technique decomposing silane into powder silicon (Joint Solar Silicon, a joint venture German company) was also a promising alternative. Upgrade Metallurgical Grade Silicon (UMG-Si) was first not envisaged as a candidate material to SP1 as it was perceived as a more long term alternative. Developments in the industry made us to change our mind in course of the project. Other new (or revitalized) processes were brought to our knowledge during the project, but at a stage too late to allow serious assessment. The acquisition of new feedstock trial materials appeared to be more difficult than anticipated. There are several reasons for that: one is that both producers and users preferred to work on a bilateral and confidential than a semi-open multilateral basis; another one is that the development at the companies was not as advanced as supposed, this has been later confirmed by delays of many of these projects. Overall, companies were very reluctant to communicate any information, not only on the process but also on analytical values.

2.1.2.2 New feedstock tested

Because of the difficulties and limitations mentioned above, only two new feedstock materials were extensively studied by SP1, i.e. Wacker and REC granular polysilicon, both being produced in pilot plants but assumed representative of the forthcoming commercial process. Granular polysilicon from MEMC is an already established process and material, which has gained recognition by the industry and can provide a good model for similar granular materials. Therefore, some but less extensive studies were carried out with an ingot made of MEMC granules acquired commercially by one of the industrial partners.

The intention was for the industry to learn how to use, to handle and to melt the new feedstock and to understand the long term consequences of using it. Learning from ingoting and wafering on one side and cell characteristics on the other side should induce process adjustments and eventually defect engineering at some points of the value chain.

The industry (3 partners of SP1 and one partner of SP2) reported that they could use the granular material 100% in the charge, without noticing advantages or disadvantages on the cycle time and yield of melting-solidification as compared to their normal charges. Issues brought up were the longer melting time and the oxygen content.

No quantified information was given by the partners on these issues which seemed to have been solved by learning-through-practicing. Analysis of oxygen in ingots made of granular silicon did not show significant deviation with baseline material. Since granular and lumpy polysilicon will co-exist in the future we understand that a mix of both materials should be beneficial to the overall yield and cycle time of the process.

Cell characterization at the institutes showed also that the cells produced according to the same standard procedure as for the base line perform as base line cells. The conclusion of the SP1 team and the industrial partners is therefore that granular material from a purity point of view can totally replace lumpy (chunks) polysilicon.

2.1.2.3 Impurity understanding and change in priorities

An important aspect of the SP1 work was to study the role and the acceptable limit to individual or groups of impurities [6]. The program started with an ambitious activity plan involving specifically “contaminated” float zone wafers and cells. Surprising results were achieved with the two first selected impurities, i.e. iron (Fe) and molybdenum (Mo). The results taught that fairly high amounts of these metals can be tolerated as single impurity (far higher than the current assumed specification). The results showed also major differences in the respective impact of each element on the final performances of the cells. Unfortunately, further investigations with float zone material and other impurities were stopped by the withdrawal of the ingot supplier. Meantime, because of persistent material shortage the interest for UMG-Si was strengthened. Industry made in-house evaluations and influenced the consortium (SP1) to look at specific issues, which might arise when using such materials. We assumed metallic impurity levels above the parts per million by weight (ppm(w)) and we could evaluate in multicrystalline ingots a long series of individual impurities i.e. Ni, Cr, Ti, Al, Cu and their combination. The selection of these impurities was debated within SP1. Criterions of selection were both academically and industrially relevant. Particular attention was put on the industrial sources of contamination (e.g. raw materials, equipment, process, handling, etc), see Figure 2.

The results confirmed the surprises from the float zone studies, and enlightened the impact of other impurities on the solar cell performances.

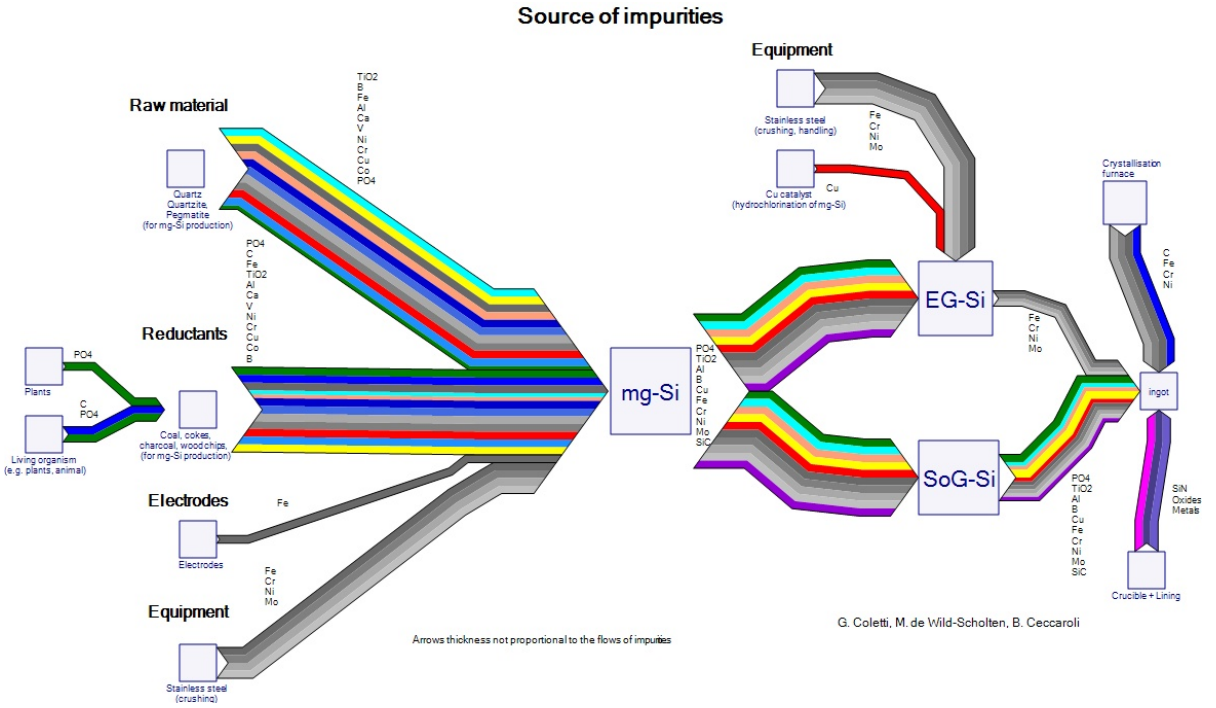

Figure 2: Schematic representation of the sources of impurities in crystalline silicon ingots (from which wafers are cut to be processed into solar cells). Graph courtesy ECN.

The learning from these studies is that good cells (high efficiency, no light induced degradation) can be achieved in spite of higher impurity contents in the feedstock. The impurities must, however, be discriminated or classified according to their ability to segregate (distribution coefficient) and diffuse (diffusivity). In addition a relationship between impurity content and extended crystal defects was found.

Furthermore, non-polysilicon feedstock is expected to contain ppm(w) amounts of boron (p-dopant) and phosphorous (n-dopant). Both modeling and experimental studies were decided to evaluate how compensation can be applied to make use of "highly" doped materials. Finally, the industry learned from the SP1 work some defect engineering remedies to achieve improved cell performances with either compensated or metal contaminated feedstock materials.

In conclusion, from these studies the industry learned more about the relationship between impurities and solar cell performances. These investigations increased the competitive knowledge base, making possible to understand the limits of the state-of-the-art technology and to further develop the technology along the overall value chain (from feedstock to solar cell manufacturing). The results of these studies will be applied by the industry to optimise and develop new manufacturing techniques, not only through relaxing the material quality without efficiency penalty (as at a first glance it might seem) but also, through improved material quality to achieve very high efficiency solar cells.

2.1.2.4 Learning through communication: The Silicon Feedstock Workshop

What could not be established through R&D studies or communication from individual partners was attempted to be clarified through a multilateral communication at a workshop organized by SP1 in November 2008. Besides disseminating the public results of the consortium, the objective of the workshop was to establish a standard set of specifications for solar grade silicon. This was partially achieved.

The feedstock is distributed into categories according to dopants (B and P) content. Electronic grade feedstock (eg-Si) was not a topic of discussion although such feedstock should be suitable for the highest efficiency solar cells (>21%). Undoped SoG is a relaxed eg-Si and nominally uncompensated (dopant compensation can be used to tune the electrical properties of feedstock with unintentional dopants present). Compensated SoG silicon is suitable for standard solar cell processes and of sufficient quality for most future generations of higher-efficiency cells. Heavily compensated potential SoG silicon is suitable for standard solar cell processes with significant process modification.

- Eg-Si: can be represented by the hyper-pure materials, e.g. polysilicon through the decomposition of (chloro)silane in a Siemens reactor.
- Uncompensated SoG-Si: likely to come from a Siemens process or a fluidized bed process optimized for supply to solar cell manufacturers.
- Compensated SoG-Si: low-compensated material which can be represented by best-in-class UMG-Si and some recycled or second class material.
- Heavily compensated potential SoG-Si: high-compensated material which can be represented by most UMG-Si currently on the market.

The next important aspect is the presence of metal impurities. Many studies reported that despite of the higher level of metal concentrations good solar cell

performances can be achieved (i.e. similar to those with standard material). The impurities' physical properties (e.g. diffusivity, distribution coefficient) are what really matters.

The workshop emphasized the need of standard analytical methods to measure impurities and quantify the material characteristics.

2.2 Wafers

Once high-purity (solar grade) silicon has been obtained it has to be brought into a form suitable for solar cells. CrystalClear is about crystalline silicon in the form of wafers. Subproject 2 deals with the preparation of crystalline solar silicon material by ingot growth applying directional solidification and ribbon growth techniques. Further it deals with wafering of these materials by multi-wire slurry sawing as well as by cutting using a diamond wire. The general aim is to reduce the wafer cost by increasing the throughput of ingot fabrication and by reducing the silicon consumption per wafer. Industry partners were Deutsche Cell, Deutsche Solar, Photowatt, REC Wafer Norway and Schott Solar, institute partners include ECN, Fraunhofer ISE, and University of Konstanz.

Several upper size ingots of 450-600 kg, i.e. up to 130% more weight than standard have been grown by two industrial partners (see Figure 3) and have been analyzed extensively by several partners in the project. Their electrical quality was found to be similar to the standard of today's production, although for some ingots reduced as-grown minority carrier lifetimes (a measure of material quality), especially close to the bottom of the block, could be observed. The productivity could be increased by around 85% for both industry partners active in the topic of increasing ingot size. This is an excellent result which adds significantly to the cost reduction goals within the crystalline silicon based module production chain.

The application of cleaner casting crucible coating and lining materials for the directional solidification technique has been tested by one industry partner. Although higher as-grown lifetimes could be reached, the resulting cell efficiency using a standard industrial solar cell process (based on "firing through SiNx") could not be significantly increased, which is an indication that impurities originating from the crucible walls can be effectively removed ("gettered") in the cell process.

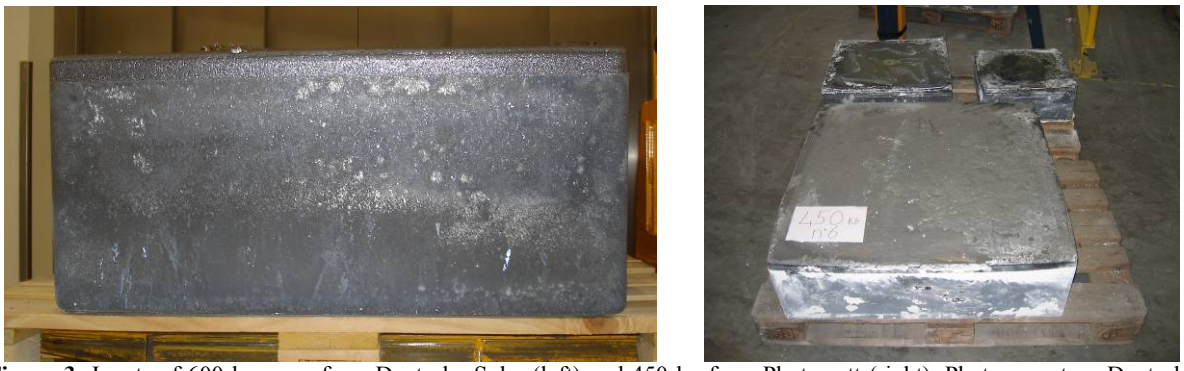

Figure 3: Ingots of 600 kg mass from Deutsche Solar (left) and 450 kg from Photowatt (right). Photos courtesy Deutsche Solar and Photowatt.

With Edge-defined Film-fed Growth (EFG) and Ribbon Growth on Substrate (RGS) two ribbon silicon materials were under investigation to address techniques which totally avoid kerf losses originating from sawing. Tests on three different feedstock alternatives for EFG revealed no differences on cell parameter level, broadening the usable feedstock base of this material. The change from 8 to 12-facet EFG technology did not show changes in cell efficiency while increasing the productivity in material production of a single EFG furnace by 50%. The investigation of thinner EFG wafers with thicknesses around 200 µm showed only slightly lower efficiencies in comparison to material with standard thickness, but on a rather low statistical basis. Thinner wafers allow for a better usage of silicon. Proof-of-concept tests on thin RGS material (100-150 µm as-grown wafer thickness) with efficiencies of around 11% demonstrated that it is possible to lower the silicon consumption per watt-peak to extremely low values of around 3 g Si/Wp.

Sawing of thinner wafers was an important issue, too. During the course of the project a large number of thin monocrystalline (Cz) and multicrystalline wafers was fabricated and delivered to Subproject 4 for processing of solar cells, among other things for the demonstrator modules (see Subproject 5). Wafering of 100 µm thin wafers with acceptable yield was demonstrated and the challenges connected with further processing have been identified.

The use of diamond wires for cutting instead of slurry-based cutting was investigated. A proof of concept could be given, but higher material costs are one limiting factor for their industrial application at the moment.

Reduction of kerf loss during wafering has been investigated and tests with two new 100 µm thin wires of different alloys have been performed in comparison to wires of standard thickness (120 µm). Using a wire of 100 µm diameter it is possible to obtain a low kerf loss of 140 µm. The 100 µm wire has a better mechanical resistance, but the sawing speed is still lower and further tests are needed for implementation in production. Apart from investigations about the total thickness variation of wafers, tests of mechanical wafer stability have been performed for a large number of wafers differing in thickness. On pre-stressed wafers, tests using different

setups (twist test and "4 bar" test geometry) have been performed. Both setups lead to comparable results, but surprisingly only two out of several methods applied for pre-stressing lead to poorer mechanical stability, whereas all other methods under investigation lead to the same mechanical stability as for the unstressed as grown reference wafers.

2.3 Wafer-equivalent approaches

Another research line pursued in the project is that of the use of so-called thin-film "wafer-equivalents" (Subproject 3). In this case a thin (typically ten to several tens of microns), high-quality silicon layer is deposited or applied onto a cheap substrate such as low grade silicon or ceramic material. Ideally, such wafer equivalents can be processed in a way very similar to regular wafers. The respective approach is therefore called "wafer-equivalent approach".

Three concepts of wafer equivalents were investigated in separate subproject "subjects": First, epitaxially thickened, free-standing thin films deposited on very thin monocrystalline silicon substrates lifted-off from thick wafers. In the second subject, work focused on a seed layer concept with recrystallized silicon seed layers on mechanically supporting substrates, thickened by thin epitaxial silicon. The respective concept is called recrystallized wafer equivalent (RexWE). The third subject investigated the epitaxial wafer equivalent (EpiWE), a sole silicon epitaxy on "standard" multi- or monocrystalline silicon substrates made from a low-cost feedstock. This subject started in month 18 of the project to realize an optimal connection to still running projects of the 5th Framework Program.

All three topics have the potential to massively reduce consumption of high-purity silicon, and therefore come along with a significant cost saving potential.

The main challenges of the first subject were the lifting off of free-standing, several tens of micrometers thin substrate films from a wafer, and the handling of these films throughout the subsequent value chain from epitaxy to solar cell processing. In CrystalClear, we could significantly enhance the possibilities for handling the lift-off films, and define a cell process better suited for the needs of the films. In this cell structure, the ~40µm thick lift-off substrate is not removed after epitaxy to give the wafer equivalent higher mechanical strength. Using an optimized solar cell process, the efficiency was improved to η=13.4% for 1.2 cm^2 cell area, and η=11.4% for a cell area of 11 cm^2. Layers up to 80 x 80 mm^2 area could be successfully lifted-off and coated with epitaxial silicon by chemical vapour deposition. Although there was significant progress and still plenty of room for further optimization, the activity was stopped already after 12 months. Reasons for this were difficulties in handling and up-scaling the layers, which only could have been overcome by investments not foreseen in the CrystalClear project. It is surely worth to carry on with this work in future projects.

Recrystallized wafer equivalents, the second subject, needed in-depth work on productivity of the recrystallization process, and on adapted layer deposition and solar cell processes to increase silicon layer quality and solar cell efficiency. Productivity is directly correlated to scanning speed in the zone melting process used for recrystallization. In the project, we were able to increase this speed from the standard value of 10 mm/min up to 400 mm/min, i.e. about a factor 40. The quality of the recrystallized layers could be kept nearly constant also at these high scanning speeds, as was proven by respective solar cells. A second main topic in the subject was the development of SiC diffusion barrier layers prepared by plasma-enhanced chemical vapour deposition. The work started from a very basic level, and resulted in SiC layers suitable for the RexWE process, characterized by good mechanical and chemical stability and sufficiently high electrical conductivity. By tuning the layer composition we managed to prepare "multi-layer Bragg" reflectors. These increased light reflection at the interface from substrate to silicon layer from 20% to 60%, resulting in an additional gain in short circuit current of 3.6 mA/cm^2. Solar cell processing resulted in maximum efficiencies on large-area RexWE solar cells (86 cm^2) of 8.5% efficiency in a zone melted and epitaxially thickened layer. Further increasing the efficiency however turned out to be very demanding, since within the resource frame given by the CrystalClear project we were not able to fully uncover the reasons for a comparatively low material quality. Although the cost predictions of the RexWE concept looked very promising, we stopped the work on this subject after 3 years, and left the necessary further material research to future R&D projects.

After stopping the first two subjects, all resources were combined to work on the subject of epitaxial wafer equivalents. The main challenges addressed in the frame of CrystalClear were the increase of solar cell efficiency mainly by increasing the fraction of light absorbed in the epitaxial layer, and the increase of productivity by use of large-area, high-throughput in-line technologies. We mainly used highly doped, photovoltaically inactive multicrystalline silicon wafers as reference substrates for our research work. Increasing the light absorption (also called "optical confinement") was realized by implementing two features: a surface texture made by plasma etching, and a reflector located on the rear of the epitaxial layer. Plasma etching in large in-line tools turned out to meet best the requirement of low removal of the epitaxial layer surface, and homogeneous texturing of the damage-free epitaxy layer. We managed to texture wafers in a commercial tool (800 mm process width) with weighted reflectivities of 16%, >99% diffuse in-coupling of light and only 2 µm etching depth.

Rear reflectors in the EpiWE concept need to be suitable for an epitaxy nucleating on their surface. In CrystalClear, we worked on a concept based on Bragg reflectors made from a multilayer stack of porous silicon of varying porosity. As a special development, we modified this concept to use a so-called chirped photonic structure. These structures allow for wide-band reflectors of very high reflectance. We achieved total reflectances higher than 90% for wavelengths from 900 nm to 1150 nm, the critical wavelength range because silicon absorbs weakly there. Applying these reflectors to EpiWE resulted in best solar cells on mc-Si substrate of 15.2% efficiency, with a current gain of 2-3 mA/cm^2 in a 20 µm thick epitaxial layer. A similar cell on monocrystalline substrate even achieved 16.1% efficiency.

As one approach to increase productivity we

developed the in-situ epitaxy of the base and the emitter (the highly doped front layer) of the solar cell, saving the elaborate separate process of phosphorus diffusion. The emitter epitaxy allows manufacturing of a high-efficiency emitter in only one minute, compared to >30 min in conventional processing. We were able to prove that the emitter deposited in-situ on the base layer is as good as conventionally processed high-efficiency emitters, and in addition has a tremendous advantage in process time and cost.

Figure 4: Demonstrator module based on 32 EpiWE cells (see text) made on monocrystalline Cz silicon wafers. Aperture area efficiency: 13.0%. Photo courtesy Fraunhofer ISE.

Large-area epitaxial deposition was investigated in an in-line prototype tool, the so-called ConCVD. We managed to increase the useable substrate size from 100 x 100 mm^2 to the nowadays standard size of 156 x 156 mm^2. Stability of the process was improved significantly, allowing deposition times of several hours before maintenance was necessary. Based on the experiences gained in CrystalClear, a scaled version of the ConCVD able to achieve throughputs of more than 20 m^2 per hour for a 20 µm thick layer is in construction in other projects. By assembling several demonstration modules, we were able to show the suitability of the wafer equivalent solar cells for standard module processing. The best module consisted of 32 EpiWE solar cells, resulting in a module aperture efficiency of 13.0%, see Figure 4. This makes clear that the EpiWE concept is close to a pilot production level, and might be successfully introduced as a new solar cell type in the market in few years time.

2.4 Cells

Solar cell manufacturing is a key issue in cost reduction strategies for photovoltaics. By enhancing cell efficiency, using thin (< 200 µm) and large (> 150 x 150 mm²) silicon wafers, processing low cost material, increasing process quality, yield and throughput, and implementing cell designs to allow for low-cost module assembly (such as rear-contact schemes) a substantial decrease of production costs per watt peak can be achieved, see Subproject 7.

A major effort was put in the development of novel cell concepts and processes suited for thin wafers in industrial fabrication [7]. Several cell concepts were distinguished and developed by the participating institutes. Three of these have been developed to the demonstration level, so that demonstrator modules could be assembled:

- cells with front and rear contacts:
  - multicrystalline silicon cell design with passivated front and rear ("i-PERC");
  - monocrystalline silicon cell design with passivated front and rear and laser fired contacts (LFC);
- cells with all-rear contacts:
  - metallization wrap-through cell design with passivated front and rear (based on SiN - ASPIRe or Al - PUM).

In addition to the efforts to implement these concepts into an industrial type of process with large area wafers, excellent results have been achieved on EFG and RGS ribbons (see also Subproject 2). World record results with laboratory-type processes could be reported, with efficiencies of 18.2 % on EFG ribbons and 14.4 % on RGS ribbons. The defect mechanism of these materials has been studied in detail and efficiency limits have been indicated.

Process steps dedicated for thin cell (see Figure 5) manufacturing like plasma texturing and in-line diffusion have been successfully implemented. Most of the novel cell concepts use rear side dielectric passivation layers to limit the influence of the surface recombination effects on the efficiency.

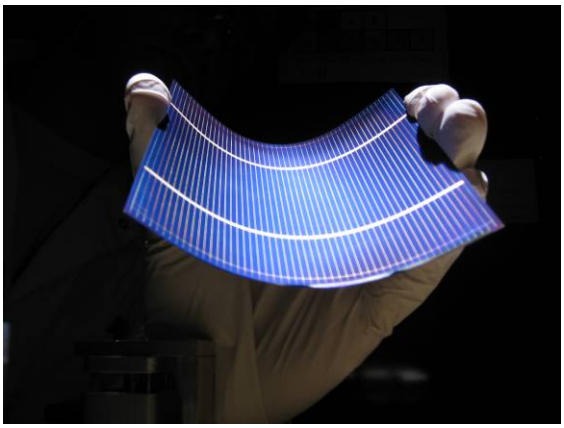

Figure 5: Ultra-thin multicrystalline silicon i-PERC cell (see text). Photo courtesy IMEC.

Implementing the novel concepts partly or completely in industrial process environments, excellent results are reported on large area solar cells. With the i-PERC process, the following results were obtained. Multicrystalline Si: 17.4% on 180 µm thick wafers, 156 cm^2; 16.8% on 120 µm, 156 cm^2 and 16.1% on 110 µm thick, 225 cm^2. Monocrystalline Cz-Si: 17.6% on 130 µm and 16.7% on 80 µm, 78 cm^2. EFG ribbons: 16.4% on 170 µm and 15.6% on 140 µm, 100 cm^2.

A Laser-Fired Contact (LFC)-PERC cell concept has been implemented in an industrial solar cell process, see Figure 6. The front-side contact has been applied using fine-line screen-printing and additional light-induced plating of silver. On Cz-Si (147.7 cm^2, 135 µm thick) an efficiency of 18.3% has been achieved.

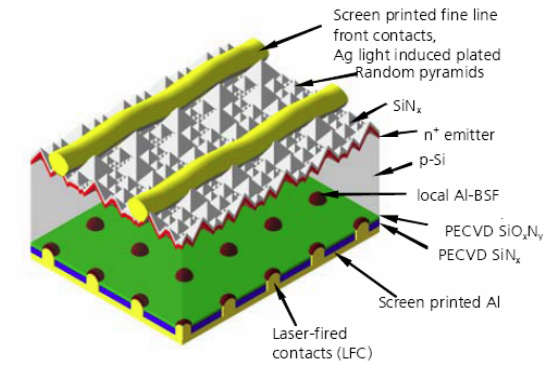

Figure 6: Schematic cross-section of an LFC cell (see text). Picture courtesy Fraunhofer ISE.

In addition to the implementation of new processes in front and rear-side contacted cells, a strong effort has been directed towards solar cells featuring all contacts on the rear side. These have the potential of low cost module manufacturing and high efficiency due to lower shading losses, higher packaging density and lower resistance losses on a module level. A Metallization Wrap-Through (MWT) concept based on a bifacial structure with dielectric passivation and fire-through contacts (ASPIRe; All Sides Passivated and Interconnected at the Rear) has been demonstrated with an efficiency of 15.9% (160 µm thick, 243 cm^2). As an alternative, an MWT structure with aluminium Back-Surface Field (Al-BSF) passivation (PUM design) has been developed towards compatibility with large and very thin wafers. Large area (243 cm^2) cells have been developed on multicrystalline silicon material with efficiencies up to 16.9% for a thickness of 120 µm (Deutsche Solar material) and 17.4% for 160 µm thickness (REC material).

Complementary, the mechanical stability of very thin wafers has been studied in detail. The impact of different crack propagation processes on the breakage was investigated. Round robins on processing and characterization have been completed. A cost study taking the implementation of the new process steps into account has been performed (see Subproject 7).

2.5 Modules

The research and development efforts of the Subprojects 1 to 4, from silicon feedstock to finished cells, come together in Subproject 5, which deals with the final 'product' of CrystalClear: the solar module. This subproject aims at developing advanced module concepts and corresponding highly automated and fast module assembly technologies, which should of course be fully matched with the cells developed in Subproject 4. The research is specifically targeted at advanced cell interconnection schemes and techniques for large and thin wafers and for back-contact cells and at new module materials and encapsulation approaches [8].

This Subproject targeted a double objective: on one hand, activities were deployed in order to sustain the trends in cell development (mainly the introduction of thinner and larger cells) while on the other hand, a direct impact on the cost of photovoltaic modules is aimed for by adapting the module manufacturing itself.

In order to maintain the cost reduction made possible by cell improvements up to the level of the finished modules, adapted interconnection technologies are required that reduce the stress between the cell and the interconnection material. A range of potential technologies were investigated with the major focus on the use of conductive adhesives, low temperature solders and laser soldering to replace conventional soldering. All methods resort in a reduced effective soldering temperature. The reliability of these technologies was demonstrated by means of an extensive test program.

The costs of the materials used dominate module manufacturing costs and lower cost alternatives would offer a direct cost benefit. The introduction of new materials however should not endanger the lifetime warranty on photovoltaic modules.

A state-of-the-art commercial solar module with crystalline solar cells is built up out of five layers. These are the cover material (iron-poor glass), the encapsulation material (EVA), the solar cells, a second layer encapsulation material and the back material (laminated foil of PVF and PET).

As possible cover materials for solar modules glass, PTFE, PMMA, PC, PVF and PET were identified. Prototype modules were manufactured and evaluated with these materials. However, except for dedicated applications, only structured glass or glass covered with ARC coatings were selected as possible alternative materials to the standard cover glass. By using anti-reflective coatings on glass, the power output of modules increases by 2.4 to 3.0% under standard test conditions (STC), corresponding to an outdoor gain of ~4% over a period of 6 months outdoor. The use of structured glass can result in an efficiency increase of 1-1.5% under standard test conditions and a 3% increase in daily output power.

For the encapsulation of solar cells the plastics EVA, PVB, silicone casting resin, epoxy casting resin and PU casting resin were examined. Test structures were constructed and exposed to temperature cycling, UV and damp/heat testing. At the end of the day, only PVB seems a real candidate to be cost competitive with the EVA used in state-of-the-art module manufacturing.

Interesting materials for the back-skin of the modules are laminates from PVDF and PET or polyester laminates with additives improving the UV stability. A candidate material to be further explored is the copper-cladded epoxy as was also used as a combined back-sheet and interconnection foil for rear-contact cells.

In support of the interest in rear-contacted solar cells as an alternative structure for thin and large substrates and their emerging market introduction, advanced module concepts that benefit from the coplanar interconnection possibilities were studied. A core method investigated is the possibility of combining the interconnection with the lamination into a single step. For the actual interconnection of rear-contact cells, two possible schemes have been identified: full pick & place using cell tabbing (eventually using preformed custom copper tabs) or using conductive back-sheet foils. In tabbing concept, the module layout is built up in one place and automated arms subsequently position all the material at the right place (encapsulation sheets, cells, tabs, adhesives, ...). In the conductive back-sheet concept, a low-cost copper cladded and patterned foil plays the combined role of interconnector and protective back-sheet. In the latter case, the conductive back-sheet is processed prior to module assembly, which ensures

flexibility over any back-contact layout; see Figure 7.

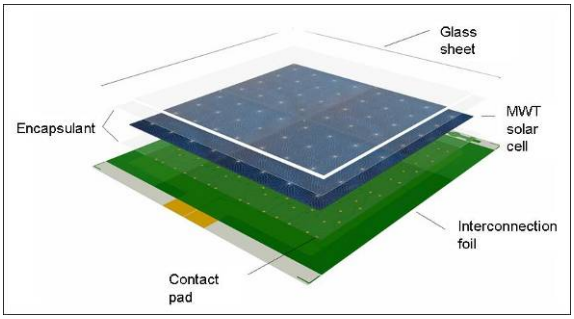

Figure 7: Exploded view of a module section based on MWT cells, conductive adhesives and patterned interconnection foil (see text). Picture courtesy ECN.

Finally, alternative encapsulation processes were studied with the eventual aim of reducing the manufacturing cost. Three main solutions have been explored: casting encapsulation, foil-based in-line roll lamination, and spray-on in-line roll lamination.
In the casting method, the encapsulant is poured in a recipient containing the cell string. A few selected resins have been used into single-cell laminates, but none of them resulted in very promising results after reliability tests.

In the roll lamination concepts, the stack of materials needed for encapsulation is fed between two rolls that apply pressure and temperature conditions enabling lamination. This concept is compatible with in-line module manufacturing and is expected to provide a very high throughput as it is a continuous process. Part of the work focused on the development of the encapsulant itself based on 2-component adhesives. From the experiments carried out, it is concluded that roll lamination as originally presented (two rolls) is not (yet) feasible.

As an important last part of the CrystalClear project, demonstrator modules have been assembled using larger batches of cells processed in Subproject 4. These demonstrator modules basically bring together (integrate) part of the results of five Subprojects: feedstock, crystallization and wafering, cell processing and module assembly.

The demonstrator modules built are based on (see Subproject 4):

- multicrystalline silicon front and rear contact (i-PERC) cells;
- monocrystalline silicon front and rear contact (LFC) cells;
- multicrystalline silicon all-rear contact (PUM) cells.

Since these modules were the very first full-size modules to be manufactured using the new cell concepts, a variety of practical problems have been encountered. Therefore only a limited set of modules actually showed the very high efficiency aimed at. These were the modules based on rear-contact (metallization wrap-through) cells of the PUM design, see Subproject 4. These modules employed conductive adhesives and patterned copper-cladded conductive foils for interconnection, see Figure 8. The aperture area module efficiencies obtained and independently verified (TüV and ESTI) are (modules with 36 cells of 156 x 156 mm^2):

- 120 μm cells: 16.0%;
- 160 μm cells: 16.4%.

Both results are world records in their class [9] (i.e. full-size modules based on multicrystalline silicon cells).

Figure 8: Solar module with world-record efficiency based on rear-contact cells and integrated interconnections (see text). Photo courtesy ECN.

2.6 Environmental sustainability

This Subproject was dedicated to the demonstration of crystalline silicon photovoltaics as a sustainable energy technology. Although photovoltaics is a renewable energy technology, the environmental quality (sustainability) of PV modules can very much differ, dependent on mainly the energy consumption during manufacture and associated environmental burdens. The energy consumption during PV manufacture is determined to the largest extent by the silicon feedstock and crystallization. Consequently the thickness of the wafers (and the solar cells) as well as the silicon loss during wafer cutting play a major role. Also, emissions during solar cell processing and manufacture of glass and encapsulation materials used for module production imply environmental burdens. The environmental burdens are usually distinguished into different impact categories. Examples of environmental impact categories are global warming, toxicity and acidification.

The activities in this part of the project covered two main aspects:

- further development of technologies for PV module recycling;
- analysis of the environmental impacts of module manufacturing by means of the Life Cycle Assessment (LCA) method.

The objectives were to demonstrate through the CrystalClear technologies that a 20% reduction per unit area of the environmental impacts of PV modules as compared to 2004 can be reached and to decrease the energy pay-back time of photovoltaic modules from 3-5 years to 2 years (installed in Central Europe).

A module recycling technology was developed in a pilot facility at Deutsche Solar in Freiberg (Saxony, Germany). Other partners offered new and existing PV module types for testing the recycling process. LCA has shown that the environmental benefit from the recovery of materials like aluminum frame, glass, copper and silicon are larger that the environmental burden created by the take-back and recycling process.

A unique LCA input data set was obtained from the industry. This data is now included in major LCA databases like ecoinvent, Probas and OpenLCA. Results of the LCA studies have been used as one of the drivers in the selection of optimal CrystalClear technology options (from silicon feedstock to PV modules) and serve as early warning for potential damaging environmental effects.

Results from SP1 to SP5, such as the processing of thinner wafers, have been implemented by the manufacturers resulting in improvement of the environmental profile. The energy payback time of crystalline silicon PV systems including module take-back and recycling is now calculated to be 1.8 years for a typical on-roof installation in Southern Europe, see Figure 9. The carbon footprint for the crystalline silicon PV system including take-back and recycling of the modules at the end of life is 30 g CO_2-eq/kWh produced for an on-roof installation in Southern Europe.

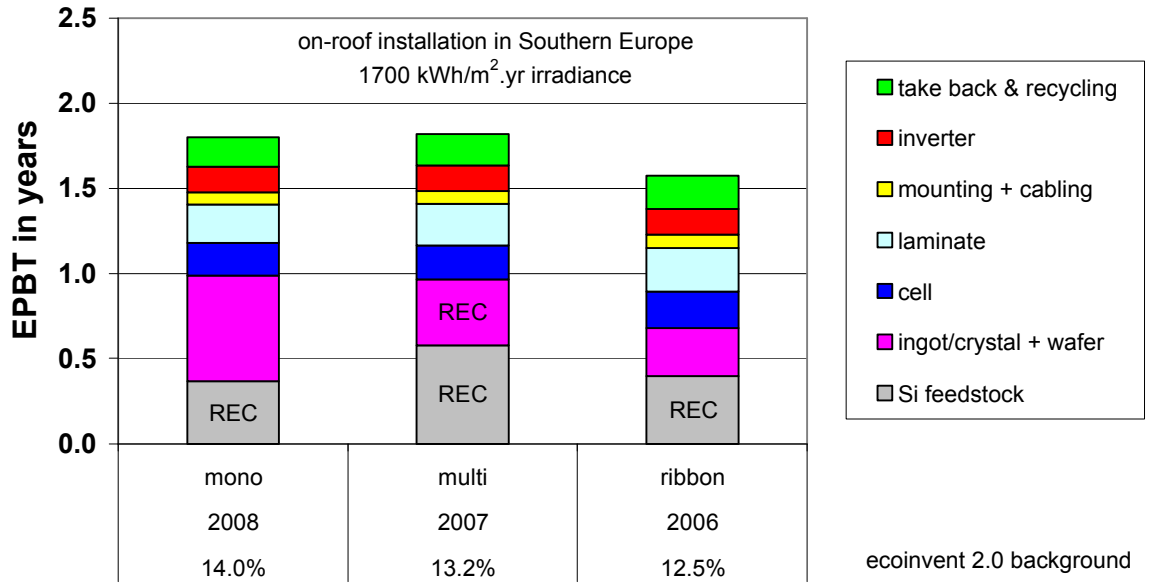

Figure 9: Energy payback time of crystalline silicon PV systems installed on-roof in Southern Europe including module take-back and recycling.

This project demonstrated a world record for multicrystalline module efficiency of 16.4% (see Subprojects 4 and 5). The module was produced by industrial scale processing and uses 180 µm thin wafers (leading to 160 µm cells). The energy payback time of this module is about 1.9 years (Central Europe) and 1.0 years (Southern Europe). Also the environmental impacts on area basis are reduced more than 20% so the CrystalClear SP6 project objectives have been achieved.

Even further improvements of the environmental performances are possible and can in fact already be anticipated for the near-term PV technology future: Si feedstock made by deposition in a fluidized bed reactor or by metallurgical purification instead of the traditional route via distillation and deposition in a Siemens type reactor implies even further reduced energy demand. Production facilities for these new Si feedstocks are coming online now.

2.7 Integration

As Integrated Project, CrystalClear addressed the entire value chain from silicon feedstock to module production. The main objective was to develop manufacturing technologies that allow wafer-based silicon solar modules to be produced at a cost of 1 € per watt-peak in next-generation plants. In order to reach this goal it was important that all aspects of the value chain were optimised with regard to each other and to the sustainability of the overall technology. Subproject 7 was the focal point for this integration. Key activities concerned cost calculations, internal roadmapping, communication and a socio-economic impact study of the factors that will influence the exploitation of the technology.

The CrystalClear research program and priorities have been set through technology roadmapping [2]. Roadmapping consisted of the definition of a set of distinctly different “overall technology options”, i.e. combinations of choices for feedstock & wafer type, cell design and process, and module design and assembly. These technology options have been analysed in terms of manufacturing costs and environmental impact (see Subproject 6).

Another core activity in SP7 was cost modeling [3, 4, 10]. To provide a solid basis for the cost modeling of the CrystalClear roadmap options, a reference technology has

been described and analysed. This technology corresponds to the typical state-of-the-art among the CrystalClear industry partners at the end of 2005. Detailed cost modeling has been performed for the different technology options defined within the CrystalClear technology roadmap and backed by the results of the other Subprojects 1-6. Direct manufacturing costs have been calculated for the whole value chain, regarding the equipment, labor, material, yield losses and fixed cost contributions. Furthermore, the impact of large-scale production scenarios (300 – 1000 MWp/a) on the manufacturing cost in the different steps of the value chain has been analysed, to take into account economy-of-scale effects. The results demonstrate that the combined effects of technology improvements (higher efficiencies, thinner wafers, improved productivity, etc.) and economies-of-scale (high-volume production) lead to calculated module manufacturing costs of CrystalClear technologies of 1.0 €/Wp (typically ± 0.1 €/Wp), see Figure 10. This represents a cost reduction of 50-60% compared to state-of-the-art at the start of the project.

A key instrument for integration-in-practice has been formed by the annual Integration Workshops, where representatives of all Subprojects presented, exchanged and discussed results. These workshops may certainly be considered a "best practice" for large EU-co-funded research projects.

In addition to these internal project meetings, CrystalClear organized five external events:

- Workshop on the Fundamentals of Silicon Nitride in Industrial Solar Cell Processing (Leuven, BE, 2005);
- Joint Scientific Workshop on R&D of Advanced Industrial Crystalline Silicon PV Technology (Budapest, HU, 2007);
- Workshop on Metallization for Crystalline Silicon Solar Cells (Utrecht, NL, 2008);
- Workshop on Solar Grade Silicon Feedstock Specifications (Amsterdam, NL, 2008);
- CrystalClear Final Event - Crystalline Silicon PV Modules at 1 Euro/Wp (Munich, DE, 2009).

These open workshops treated important issues in science and technology of wafer-based crystalline-silicon PV technology and have served as reference in the respective fields.

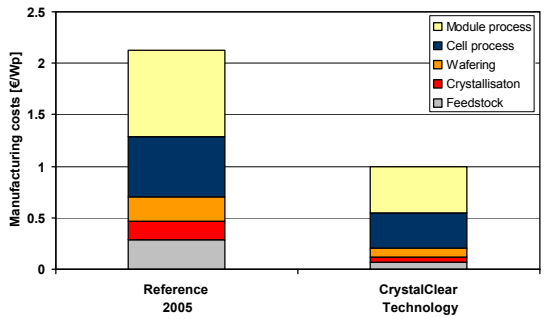

Figure 10: Calculated manufacturing costs for 2005 reference technology and selected CrystalClear roadmap technology.

3 CONCLUSIONS

Overall we can conclude that the Integrated Project CrystalClear has clearly shown that wafer-based crystalline silicon solar module technologies have the potential to reach manufacturing costs of 1 € per watt-peak or less in next generation (i.e. large) plants. This also implies that crystalline silicon PV is compatible with the requirements to (at least) achieve grid parity on the level of retail electricity prices. Furthermore, CrystalClear demonstrated the successful collaboration of a large consortium consisting of R&D and industry partners from different parts of the crystalline silicon PV value chain.

4 ACKNOWLEDGEMENTS

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5 REFERENCES

[1] W.C. Sinke, *The CRYSTALCLEAR Integrated Project: Next generation crystalline silicon technology from lab to production,* Proc. 20th European Photovoltaic Solar Energy Conference and Exhibition (WIP, Munich, DE, 2005), p.606.

[2] W.C. Sinke, G. del Coso, and C. del Cañizo, *Crystalline silicon PV technology roadmapping in the CRYSTALCLEAR Integrated Project*, Proc. 21st European Photovoltaic Solar Energy Conference and Exhibition (WIP, Munich, DE, 2006), p. 3213.

[3] W.C. Sinke, C. del Cañizo, and G. del Coso, *1 € per watt-peak advanced crystalline silicon modules: the CrystalClear Integrated Project,* Proc. 23rd European Photovoltaic Solar Energy Conference and Exhibition (WIP, Munich, DE, 2008), p. 3700.

[4] C. del Cañizo, G. del Coso, and W.C. Sinke, *Crystalline silicon solar module technology: towards the 1 € per watt-peak goal,* Progress in Photovoltaics: Research and Applications 17 (2009) 199.

[5] A list of publications and other project-related information as well as many downloads are available from www.ipcrystalclear.info.

[6] G. Coletti, P. Bronsveld, C.C. Swanson, R. Kvande, L. Arnberg, H. Habenicht, C. Knopf, *What metal impurities can we allow in silicon feedstock?,* and references therein. These proceedings.

[7] J. John, G. Beaucarne, P. Choulat, Y. Ma, R. Russell, I. Romijn, A.W. Weeber, M. Hofmann, R. Preu, L. Gautero, A. Slaoui, N. LeQuang, O. Nichiporuk, C. del Cañizo, A. Pan, H.J. Solheim, J. Evju, H. Nagel, B. Bitnar, M. Heemeier, T. Weber, M. Kaes, B. Raabe, H. Haverkamp, C. Strümpel, and G. Hahn, *A review of 5 years cell development within the European Integrated Project CrystalClear,* and references therein, These proceedings.

[8] E. van Kerschaver, I. Bennett, H. Wirth, S. Ohl, P. Sánchez-Friera, N. Lenck, R. Gomez, and A. Messant, *Results of 5 years module manufacturing research in the European CrystalClear project,* and references therein. These proceedings.

[9] I.J. Bennett, C. Tjengdrawira, A.A. Mewe, M.W. P. E. Lamers, P.C. de Jong, and A.W. Weeber, *World record module efficiency for large and thin mc-Si rear contact cells,* and references therein, These proceedings.

[10] G. del Coso, C. del Cañizo, and W.C. Sinke, *Influence of feedstock on c-Si module cost*, and references therein, These proceedings.