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CRYSTALCLEAR, A EUROPEAN RESEARCH PROJECT TOWARDS 1€/WP WAFER-BASED SI PV TECHNOLOGY

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ABSTRACT

CrystalClear is an Integrated Project carried out in the 6th Framework Program of the European Union. The main project aim is to reduce the direct manufacturing costs of crystalline silicon PV modules to 1 €/Wp, when produced in next-generation plants. CrystalClear deals with the entire crystalline silicon value chain from silicon feedstock up to module manufacturing. In the course of the project, which started in 2004, several 'overall' technologies have been defined and developed. These technologies represent different combinations of wafer options, cell and module designs as well as processing approaches, and will be discussed in the paper.

1. INTRODUCTION

CrystalClear is a large European research project covering the entire value chain from feedstock up to module technology [1,2]. The project runs from January 2004 to June 2009. The consortium consists of 16 partners and the total project budget is 28 M€. The industry partners are: BP Solar Spain (ES), Deutsche Cell (D), Deutsche Solar (D), Isofoton SA (ES), Photowatt (F), REC (NO), REC Scanwafer (NO), SolarWorld Industries (D) and SCHOTT Solar (D). The university partners are: Utrecht University (NL), the University of Konstanz (D) and the Polytechnical University of Madrid UPM-IES (ES)). The research institute partners are: CNRS-InESS (F), ECN Solar Energy (NL), Fraunhofer ISE (D) and IMEC (B). ECN is coordinating the project. Our goal is to develop a manufacturing technology for wafer-based silicon solar modules at a cost of 1 €/Wp, which corresponds to a reduction of about 50% compared to the 2005 reference technology. The cost reduction should be realized by reducing the consumption of expensive materials (especially silicon), increasing the module's conversion efficiency and developing new low-cost manufacturing processes. In addition the project aims at improving the sustainability and applicability of the modules.

The project is organized in seven subprojects. The structure can be seen in Fig. 1. The project is organized in seven subprojects. The structure can be seen in Fig. 1. The management of the project is carried out in subproject 0. The topic in subproject 1 is feedstock evaluation. New feedstock material is characterized and tested up to cell level. The effect of impurities (e.g. Fe, Ti, Mo) on cell output is investigated together with its behaviour using today's cell processing including gettering and passivation. Based on these results first demands (specifications) for so-called Solar Grade silicon can be made. In subproject 2 growing larger ingots, new sawing techniques resulting in ultra-thin wafers and ribbons made from new silicon material are examined. In subproject 3 process development for wafer equivalents is carried out. High-quality thin films are grown on low-cost substrates and solar cells are made and characterized in detail. In subproject 4 advanced cell concepts and processes are developed. These new cell concepts and processes should result in high cell efficiency at lower costs. In subproject 5 new module concepts and manufacturing technologies are developed applying new materials. In subproject 6 the sustainability of the current and newly developed technology are investigated. Recycling PV modules is a part of subproject 6 as well. Finally, subproject 7 is dealing with the integral assessment (cost model, implementation plans, etc).

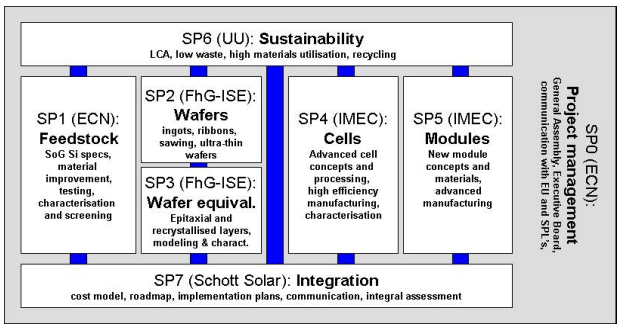

Figure 1: Structure of CrystalClear

Results of the technology developments will be discussed in the paragraphs below.

2. CRYSTALCLEAR TECHNOLOGIES

The technologies that are selected within CrystalClear for further development and evaluation are:

1. Multistar: mc-Si with front-to-rear interconnection
2. MultistaR: mc-Si with rear-to-rear interconnection (Metallization-Wrap-Through, MWT)
3. Superslice: Cz Si with front-to-rear interconnection
4. SuperslicE: Cz Si with rear-to-rear interconnection (Emitter-Wrap-Through, EWT)
5. Ribbonchamp: ribbon mc-Si with rear-to-rear interconnection (MWT)
6. Epi.C: thin-film Si on low-cost substrates using front-to-rear interconnection.

All wafer technologies (1 to 5) are based on the use of very thin wafers (typically 120 µm). This necessitates the use of low-stress interconnection methods using advanced soldering techniques or conductive adhesives. In the case of MWT and EWT cells, (rear-to-rear) interconnection is done using either 'smart tabs' (specially designed metal strips) or a foil with integrated conductive pattern. The target cell efficiencies are 19% for monocrystalline silicon, 17% for multicrystalline silicon, and 16% for ribbon and wafer equivalent silicon (rounded numbers).

Within the timeframe of the project, only technologies 1 to 3 will actually be developed to the level of a complete demonstrator module. For technologies 4 to 6 research after and beyond CrystalClear is required.

3 RESULTS CRYSTALCLEAR TECHNOLOGIES

3.1 Feedstock evaluation

One of the objectives of subproject 1 is to determine the behaviour of impurities in silicon. The effect of the impurity concentration on cell output is investigated for impurities Fe and Mo [3]. Fe is one of the common impurities in silicon and can easily be gettered. Mo is known because of its detrimental effect on the solar cell output. Furthermore, the diffusion coefficient of Mo is slow and therefore the gettering effect will be much less than for Fe. Research on the effect of other impurities is still ongoing (see this conference Coletti et al. and [4]).

To examine the effect, FZ silicon rods grown mono and multi-crystalline were intentionally contaminated before the growth take place. Solar cells were made using a today's manufacturing process based on screen-printed metallization which was fired through the SiN_x:H coating. This process includes gettering during the emitter diffusion and bulk hydrogen passivation during contact formation. The effect of impurity concentration on the internal quantum efficiency is shown in Fig. 2 (Fe) and 3 (Mo). For Fe the effect is small at concentration up to 10^{12} cm^{-3} on wafer level. The impact of Mo is already visible at concentration of 10^{11} cm^{-3} on wafer level. The results are used as first input for the specifications of solar grade silicon.

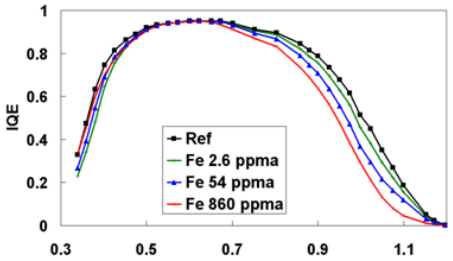

Figure 2: Effect of Fe on IQE of mc-Si solar cells. Concentrations refer to Fe added in the silicon melt, and are lower on wafer level.

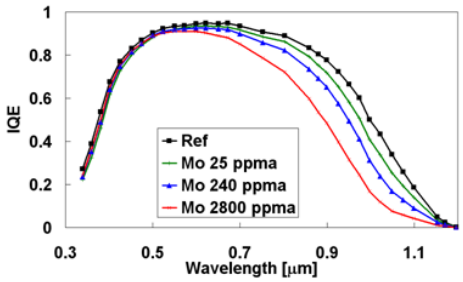

Figure 3: Effect of Mo on mc-Si solar cells. Concentrations refer to Mo added in the silicon melt.

3.2 Wafer and ribbon technologies

An important overall aim of subproject 2 is to increase the productivity of crystallization equipment and the utilization of the silicon feedstock. To this aim, larger crucibles were used for ingot crystallization, which led to a better use of the furnace capacity. Ingots with an 80% higher than standard weight (up to 400-450 kg) were successfully grown and used for wafer and cell manufacturing.

The electrical and mechanical quality of the large ingots was found to be very similar to the standard ingots of today's production. As the production time per ingot was only slightly increased the productivity of the growth equipment was increased significantly.

Slicing of large and thin silicon wafers from standard multicrystalline ingots is being developed by different partners. In the beginning of the project the thickness was around 200 µm. Recently multicrystalline wafers of 120 µm and monocrystalline wafers of only 80 µm have been demonstrated in large numbers. When processed into high efficiency solar cells, these thin wafers will lead to much lower silicon consumption in terms grams of silicon per watt-peak of module power.

Ribbon technologies that are researched are EFG (Edge-defined Film-fed Growth) and RGS (Ribbon Growth on Substrate). These techniques promise high productivity and very low silicon consumption down to 3 g/W module power in the medium term. A record

EFG cell with an efficiency of 18.2% was made on 4 cm^2 ribbon material using evaporated and plated contacts [5]. In silicon ribbon growth by the RGS technique, which is under development at ECN, thin (100–150 µm) ribbons were made for evaluation. Solar cells with high efficiency processes and industrial screen printing processes were applied and gave very promising efficiencies up to 14.4% [6].

3.3 CrystalClear Cell technologies

Multistar

One of the Multistar cells under development is the so-called *i*-PERC (Fig. 4). On 100 cm^2 180 µm thin mc-Si wafers an efficiency of 17.4% was reached [7]. The process consists of plasma texturing, $POCl_3$ emitter diffusion, SiO_x/SiN_x stack for rear surface passivation, and screen-printed front and rear side contacts. For contacting the rear, the passivating stack has been opened locally. For 156 cm^2 120 µm thin mc-Si wafers the best efficiency obtained with the process described above is 16.8% [8].

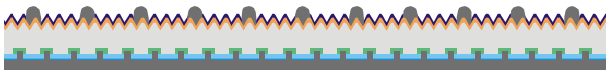

Figure 4: Cross section of the *i*-PERC cell

MultistaR

The back-contacted MultistaR, which is developed, is the so-called ASPIRe cell. This MWT cell has SiN_x passivating layers and open screen-printed metallization on both sides (Fig. 5). The best efficiency reached on mc-Si substrates with 180 µm thickness is 16.4% [9].

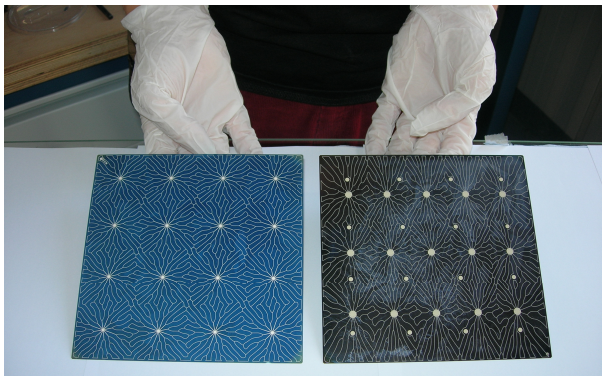

Figure 5: Front and rear side of an ASPIRe cell, an MWT cell with passivating layers on both sides.

Superslice

Different Superslice technologies are studied within CrystalClear. One is based on Laser Fired Contacts (LFC). Using high-efficiency lab processing and an a-Si/SiO_x stack for rear side passivation an efficiency of 21.7% was obtained on 4 cm^2 FZ material [10] (Fig. 6). For another concept with a boron BSF and SiN_x on both sides with screen-printed H-pattern metallization, an efficiency of 18.2% has been reached on 180 µm 156 cm^2 Cz silicon [11]. For 130 µm thin material the best efficiency reached up to now is 17.2%.

On 100 µm thin 100 cm^2 Cz i-PERC cells with efficiencies above 17% have been demonstrated [12].

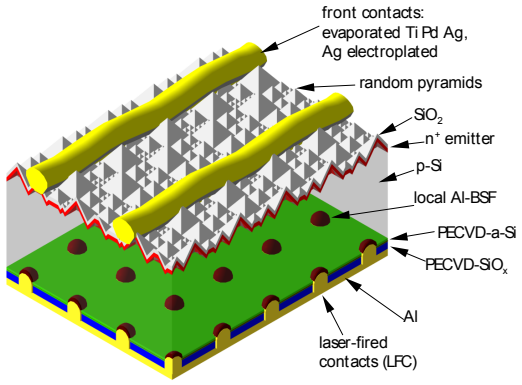

Figure 6: LFC cell concept, a Superslice technology.

SuperslicE

The SuperslicE technology investigated is the EWT concept. Cell processing is based on screen-printed contacts.

Ribbonchamp

The *i*-PERC concept has been tested on EFG material. The best efficiency obtained on 100 cm^2 ribbons are 16% for 170 µm thin material and 15.6% for 140 µm material [13].

Epi.C

For this concept a high-quality thin layer is deposited on a low-cost substrate. Cells made from an epitaxial layer with a thickness of about 20 µm on a highly-doped low-cost mc-Si substrate have shown efficiencies up to 14%. Cell processing steps are based on $POCl_3$ diffusion, screen-printed metallization and firing-through [14]. With epitaxial growth of both the thin-film base layer and emitter, and evaporated contacts and using monocrystalline Cz substrates efficiencies above 15% have been obtained [15].

3.4 Module technology

For very thin and fragile substrates it is important to develop new module technologies that will result in lower stress. New interconnection technologies based on conductive adhesives has been successfully tested. In Fig. 7 it can be seen that after more than 1000 thermal cycles the performance of strings interconnected with conductive adhesives is at least as good as those interconnected with conventional soldering [16].

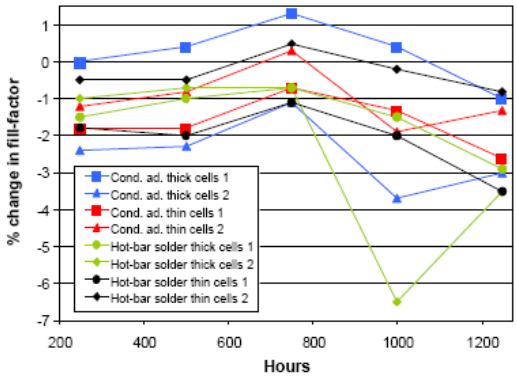

Figure 7: Relative change in FF after thermal cycling for both conductive adhesives and soldering.

Other interconnection technologies that resulted in lower stress are laser and induction soldering, tabs with low thermal expansion coefficients and the application of low-temperature solders [17].

3.5 Sustainability

A useful measure for the sustainability of PV modules is the energy pay back time (EPBT). As can be seen in Fig. 8 the EPBT for different technologies is about 2 years for Southern Europe, and is expected to be below 1 year for future technology [18]. From this figure it can be seen that the silicon wafer is the most important factor for mono and mc-Si. Therefore, reduction of the silicon consumption will improve the environmental profile of PV even more.

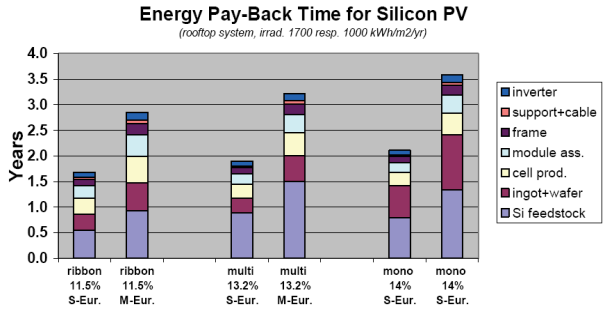

Figure 8: EPBT for different technologies and different hemispheres.

3.6 Cost analysis

The most important parameter that determines the success of solar electricity is the cost. The expected costs and silicon consumption per Wp for different CrystalClear technologies can be seen in Table I [19]. Based on these results, it can be concluded that crystalline silicon PV technology has the potential to reach direct module manufacturing costs of around 1 €/Wp on a relatively short term (i.e. within ~5 years). This implies that wafer-based crystalline silicon photovoltaics is compatible with the requirements to achieve grid parity. Critical conditions to reach this cost level are: efficient silicon utilization (g/Wp module power), high total area module efficiency and high-throughput, high-yield production.

Table I: Expected direct manufacturing costs for PV modules made using different technologies.

	η (%)	€/Wp	g Si/Wp
Multistar	17	1.00-1.14	4.5-4.7
MultistaR	17	1.05-1.21	4.5-4.7
Superslice	19	1.03-1.32	4.0-4.2
SuperslicE	19	1.15-1.32	4.1-4.2
Ribbonchamp	16	1.02-1.30	1.7-1.8
Epi.C	16	1.01-1.15	-

4. SUMMARY

Within CrystalClear different Si wafer based technologies are developed and evaluated with respect to costs and manufacturability. It can be concluded that all technologies will result in significant cost reduction and lower material use, which improves the environmental profile of the final product.

5. ACKNOWLEDGEMENTS

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