Emitter Optimization on a-Si:H/c-Si Heterojunction Solar Cells for Isotextured Wafers

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ABSTRACT: In this work we report on the emitter optimization on isotextured n-type FZ c-Si wafers for a-Si:H/c-Si heterojunction solar cells. At ECN, three different types of isotexturing have been developed. From lifetime measurements performed on passivated isotextured wafers, it was concluded that two of the three types of texturing are compatible with our silicon heterojunction process. The next step was to optimize the heterojunction emitter on the isotextured wafers. The emitter structure, consisting of a thin intrinsic layer and a p-layer has been deposited in a medium sized area (30 cm x 40 cm) PILOT reactor by means of 13.56 MHz RF PECVD. As a p-layer, we found that an a-Si:H p-layer with a thickness of around 20 nm gave the best results. Finally, we performed a thickness series of an already optimized i-layer for the isotextured wafers. We found that the optimal i-layer thickness on these isotextured wafers (10 nm) is higher than on flat polished wafers (7 nm). The newly optimized structure finally led to an efficiency of 16.4% with a V_{OC} of 623 mV, a J_{SC} of 34.2 mA/cm^2 and a FF of 77%. An important next step in our research will be to extend the results shown in this paper to isotextured mc-Si wafers.

Keywords: Heterojunction, c-Si, isotexturing, PECVD

1 INTRODUCTION

Heterojunction solar cells based on amorphous and crystalline silicon are very suitable devices for low cost and high efficiency energy conversion. Sanyo showed an efficiency of 22.3% for a-Si:H/c-Si heterojunction solar cells with a thin intrinsic layer, which clearly demonstrates its feasibility as a concept for high efficiency solar cells [1]. This type of cell has already been brought to the market as well [2,3]. Compared to conventional (m)c-Si solar cells, a considerable cost reduction can be achieved because the fabrication process can take place at temperatures below 200^{o}C. Another advantage of a-Si:H/c-Si heterojunction solar cells are the better temperature characteristics compared to conventional c-Si solar cells.

Wafer texturing is a well-established way to increase the light trapping and thereby the light induced current density in c-Si based solar cells. The most common way to apply texturing to mc-Si wafers is by isotropic texturing using an acidic solution [4,5]. It has the huge advantage over alkaline anisotropic texturing that it does not form steps at the grain boundaries [6]. These steps make it very difficult to entirely cover the surface of the wafer with the emitter, which has a total thickness of only several tens of nanometers, whereas these steps at the grain boundaries are typically in the order of several microns [7].

In this work we report on the emitter optimization on different types of isotextured wafers for a-Si:H/c-Si heterojunction solar cells. The performance of the cells on textured wafers is compared to the performance on flat, double sided polished (DSP) wafers, which are used as a reference. The emitter structure has been deposited by means of a very simple process using 13.56 MHz RF PECVD in the PILOT medium size multichamber deposition system [8] at our laboratory with substrate temperatures not exceeding 200^{0}C.

So far, we have done our research on FZ c-Si wafers because there is less variation in neighboring wafers compared to mc-Si. In the future however, we want to extend this work to a-Si:H/c-Si heterojunction solar cells on isotextured mc-Si wafers.

2 EXPERIMENTAL

For this research, 2-5 Ωcm (100) n-type FZ c-Si wafers with an area of 5x5 cm^2 and a diffused back surface field (BSF) have been used. First, the wafers were dipped in HF (1% solution in H_2O) for 1 min. Thereafter, the thin intrinsic layer and the p-layer were deposited in a multichamber medium sized vacuum system, called PILOT [8]. The a-Si:H layers have been deposited by means of 13.56 MHz RF PECVD. For the thin intrinsic layer we have used pure silane. For the p-layer we used a gas mixture consisting of silane, hydrogen and $B(CH_3)_3$, which is also known as TMB. On top of the emitter structure, an 80 nm thick ITO layer has been deposited by RF magnetron sputtering. Finally, Ag contacts were evaporated on both sides of the cells. For the Ag evaporation on the top side, a mask has been used to define the grid pattern of the front contacts. On the back side, the cells were fully covered with Ag. After these deposition steps, the cells were annealed for 1 h at 160^{0}C in a N_2 atmosphere. The performance of the solar cells has been tested by means of I-V and spectral response measurements. The quality of the p-layers has been tested and optimized by means of conductivity (both dark and illuminated), activation energy and R/T measurements on Corning glass.

3 RESULTS AND DISCUSSION

3.1 Passivation Properties of Textured Wafers

In order to increase the light absorption of the wafers used in this research, three different types of isotexture (A,B and C) have been developed and investigated [7]. First, their passivation properties have been tested in order to evaluate their compatibility with the silicon heterojunction fabrication process and compared to the results on flat, double-side polished (DSP) wafers. This has been done by performing QSSPC [9] measurements on different device structures. On all samples, the textured front side was covered with a standard emitter, and the back side with surface passivating SiN_x:H [10]. As a reference, a sample with SiN_x:H deposited on both sides has also been provided. Figure 1 shows the effective lifetime (τ_{eff}) and implied V_{OC} at an injection level of 10^{15} cm^{-3} as determined from QSSPC measurements [7].

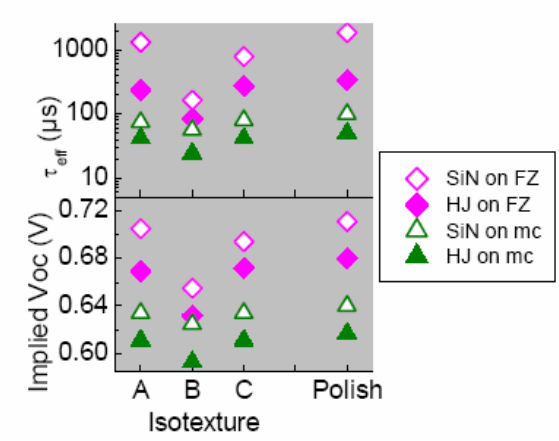

Figure 1: Effective Lifetime and Implied V_{OC} as measured by QSSPC for different types of texturization. The polished wafers are used as a reference. Courtesy of Y. Komatsu [7].

The results in Figure 1 show that the texturing types A and C show good passivation properties, almost as good as the reference sample. For type B, the effective lifetime of minority charge carriers is significantly lower than for the other samples. This indicates that texturing type B is not compatible with the silicon heterojunction process. Therefore, type B will not be considered any more in the rest of this work.

When incorporated into finished solar cells, the isotextured wafers show comparable V_{OC} values and slightly higher J_{SC} values compared to the results on flat DSP wafers. The higher J_{SC} values can be ascribed to the better light absorption of the textured wafers compared to the DSP wafers. The results are shown in Table 1.

Table 1: Output parameters for finished solar cells on flat DSP and isotextured FZ n-type c-Si wafers

Texture Type	V_{OC} (mV)	J_{SC} (mA/cm^2)
Flat DSP	613	32.3
A	617	34.0
C	610	34.0

The emitter structure which has been used so far, has not been optimized for the newly textured wafers yet. Therefore, the next step was to optimize this structure.

3.2 p-layer optimization

We tried to develop three different types of p-layers, i.e. a-Si:H, a-SiC:H and µc-Si:H and evaluated which structure is the most feasible for and compatible with our solar cells.

We have been able to fabricate good a-Si:H p-layers for our heterojunction solar cells. The activation energy was typically between 0.35 and 0.40 eV and when incorporated into solar cells we obtained proper fill factors. The optimal thickness of our a-Si:H p-layer was found to be 20 nm.

Compared to standard a-Si:H, layers consisting of a-SiC:H are expected to have a higher bandgap and thus a higher transparency. A disadvantage of a-SiC:H layers, which is caused by the carbon incorporation, is an increasing defect density which seems to have a detrimental effect on the performance of the cells. In practice, our a-SiC:H layers showed less good results than our a-Si:H p-layers. The activation energy was significantly higher and when incorporated into solar cells, the fill factor strongly decreased compared to cells with an a-Si:H p-layer. This clearly indicates that this a-SiC:H p-layer is too defective and that the doping efficiency is low.

Microcrystalline silicon usually has a higher conductivity and a lower absorption coefficient than amorphous silicon. Both of these properties are in principle beneficial for good p-layers. The main challenge when depositing a µc-Si:H p-layer in silicon heterojunction solar cells on top of a thin intrinsic layer consisting of a-Si:H is to achieve (micro)crystalline growth without a long incubation phase. This property is very critical because the optimal p-layer thickness is typically in the order of several tens of nanometers. First, individual p-layers have been deposited and optimized on Corning glass. Our a-Si:H layers showed proper results, both on glass and when incorporated in finished solar cells. The µc-Si:H layers, however, showed good results regarding conductivity and activation energy when deposited on glass, but did not show good results when incorporated in a cell. This could indicate that the growth of this layer is microcrystalline on glass, but amorphous on top of a c-Si wafer with a thin intrinsic layer. In order to test this, we deposited an i/p structure on glass, so the growth of the p-layer on top of the thin intrinsic layer could be studied. Raman spectroscopy showed that the growth of the p-layer directly on glass was microcrystalline, but on top of a thin intrinsic layer, the layer turned out to be amorphous. We tried this for an extensive range of deposition conditions, but in all cases the result was the same. The reason that we did not evaluate the crystallinity of the p-layer on top of a c-Si wafer with thin intrinsic layer is that Raman spectrum will be dominated by the wafer in that case.

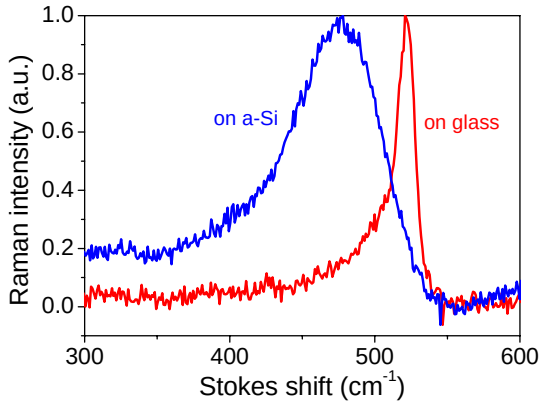

Figure 2: Raman Spectroscopy measurements for µc-Si:H p-layer on glass with and without thin intrinsic layer

So far we have succeeded to fabricate properly working a-Si:H p-layers for a-Si:H/c-Si heterojunction solar cells. For a-SiC:H and µc-Si:H p-layers, this has not been the case yet. In the case of µc-Si:H p-layers, this is due to the fact that only a thin intrinsic amorphous silicon layer can have a large influence on the nucleation of nanocrystallites. Therefore we decided to continue with the a-Si:H p-layer, combined with isotexture type C. Here, in fact, the choice between type A and C was arbitrary. The next step was to optimize the thickness of the thin intrinsic layer.

3.3 Thickness optimization of thin intrinsic buffer layer

The standard i-layer we have used in this research has been deposited at a relatively low substrate temperature of approximately 120^{0}C to prevent epitaxial growth onto the c-Si wafer. A relatively low deposition temperature combined with a high plasma power is expected to be the most suitable manner to prevent epitaxial growth onto the c-Si wafer [11]. In this research, only the thickness of this layer, combined with the new p-layer, has been optimized. The deposition conditions of the i-layer have not been changed.

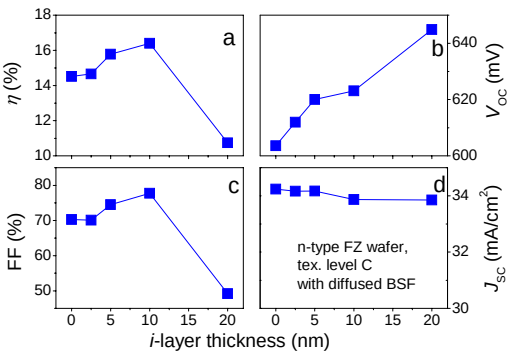

Figure 3 Output parameters for various i-layer thicknesses.

From figure 3b, it can be seen that the V_{OC} increases with increasing i-layer thickness, as can be expected due to improving surface passivation. For a thin intrinsic layer, the best surface passivation is expected to occur at several tens of nanometers [12]. The J_{SC} slightly decreases due to increasing absorption in the i-layer with increasing thickness. As can clearly be seen from figure 1c, the FF collapses for i-layer thicknesses above 10 nm. For such thicknesses, the holes cannot tunnel through the intrinsic layer any more and the layer acts as a barrier. The optimal layer thickness turned out to be approximately 10 nm, as can be seen from figure 3a. This thickness is higher than observed by most other groups [i.e.11,13] and previous work [14], which could be ascribed to the texturing of the c-Si wafers. It has to be said, however, that in our case the thickness of the thin intrinsic layer could only be estimated timewise, and might therefore be slightly overestimated.

3.4 Solar Cell Results

The newly developed solar cell structure, consisting of an isotextured c-Si wafer with diffused BSF, a 10 nm thick intrinsic layer and improved a-Si:H p-layer led to an efficiency of 16.4% with a V_{OC} of 623 mV, a J_{SC} of 34.2 mA/cm^2 and a FF of 77%.

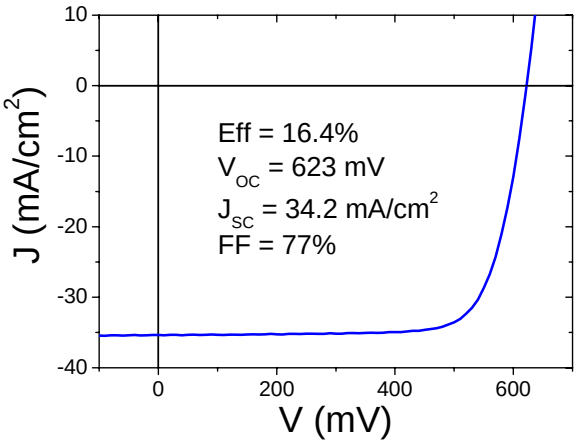

Figure 4, I-V curve of our present best cell with layers deposited in the medium-sized reactor.

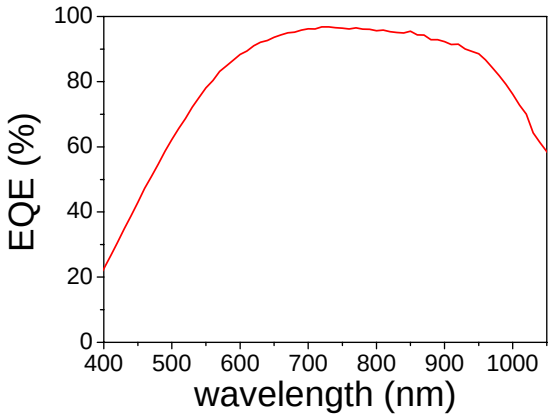

Figure 5, Spectral Response measurement of our best cell.

From the spectral response measurement shown in Figure 5, it can be seen that the cell performs very well for wavelengths between roughly 600 and 900 nm. For lower wavelengths, we can see that there is still some room for improvement. Especially the development of a thinner and more transparent emitter structure could be beneficial in this case.

4. CONCLUSIONS

We have investigated the influence of different types of isotexturing on the performance of a-Si:H/c-Si heterojunction solar cells. Compared to our results on flat DSP wafers, the cells on the textured wafers showed a considerable improvement in efficiency. Furthermore we optimized the emitter structure for the newly developed types of isotexturing. This emitter structure consists of a thin intrinsic layer with a thickness of 10 nm combined with a 20 nm thick a-Si:H p-layer. The optimal i-layer thickness was found to be higher than the optimal i-layer thickness for i-layers on flat wafers. The whole emitter structure has been deposited by 13.56 MHz rf PECVD. This finally led to an efficiency of 16.4% and a V_{OC} of 623 mV on isotextured n-type FZ c-Si wafers with diffused BSF. An important next step in our research will be, to optimize the performance of the solar cell structure described in this paper on textured mc-Si wafers. Also, the development of a deposited BSF should be mentioned.

5. ACKNOWLEDGMENTS

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