COMPARISON OF HIGH EFFICIENCY SOLAR CELLS ON N-TYPE AND P-TYPE SILICON WAFERS USING IDENTICAL PROCESSING

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ABSTRACT: A low-cost, high-efficiency process on large area n-type base silicon cells is reported which is based on a screen printed aluminium-alloyed rear junction concept and phosphorus-diffused front surface field. The cell process uses fabrication techniques which are very close to the current industry-standard screen-printed mc-Si cell process for p-type wafers. An independently confirmed record-high efficiency of 17.4% (140 cm²) is achieved on n-type floatzone (FZ) silicon wafers. We compare, by experimental tests and modeling, the differences of using n-type wafers and p-type wafers with this identical process sequence. On p-type FZ wafers, with the same process 17.6% is obtained (FF of 79%), and 16.8% on p-type CZ wafers (FF of 76%). 1D-model calculations allow us to identify the potential for further enhancement of the n-type cell efficiency to above 18.0% by improving front surface passivation. We also discuss experimental characteristics and typical limitations of cells produced by this process from n-type multicrystalline wafers.

Keywords: n-type silicon solar cell, aluminium-alloyed emitter, rear junction

1 INTRODUCTION

n-type silicon wafers are an attractive alternative to the commonly used p-type wafers due to several important characteristics including higher tolerance to metal impurities [1, 2] resulting in a high diffusion length of the minority charge carriers as well as absence of the light-induced degradation which is related to boron-oxygen defects.

The industrial applicability of the n-type wafers has been demonstrated in the advanced concepts comprising HIT-technology (Hetero-junction with Intrinsic Thin-layer) [3] or the back-contact cell design [4]. In the first case the p-n junction and excellent interface passivation have been achieved by deposition of non-doped a-Si and p-type a-Si layers on a p- or n–type c-Si substrate with PECVD method. The result is a conversion efficiency of 21.5% at a cell size of 100.3 cm^2. The back-contact cell design obtained using photolithography in combination with novel manufacturing techniques yielded efficiency of 21.5% on cell area of 149 cm^2 using PVFZ silicon. This technology enabled reaching 22% cell efficiency in producion (GEN II). As a result of recent developments efficiency of 23.4% has been reported (GEN III).

However, a wider application of the n-type silicon for industrial solar cell fabrication can be provided by compatibility with low-cost solar cell processing and preferably while applying existing manufacturing technologies. At the same time the produced n-type solar cells should sustain high and stable efficiencies at least at a comparable level with p-type. The Al-alloyed back-junction cell design represents an opportunity to fulfill those prerequisites. The concept was introduced for the first time by EBARA Solar Inc. [5]. It was applied on dendritic-web n-type silicon of base resistivity 20 Ohm/sq achieving the efficiency of 14.2% on cell area of 25 cm^2. It represents a fast way, for industry, to move from p-type to n-type substrates because of the possibility of maintaining the same process sequence. The main differences, compared to the conventional (n^+pp^+) process used in industry for p-type wafers, is that during the phosphorus diffusion a front surface field (FSF) is created instead of an emitter, and during the contact co-firing the aluminium back junction is formed instead of back surface field (BSF). Conversion efficiencies up to 17.0% were reported on industrial n-type solar cells with area of 100 cm^2 [6]. The cell processing employed phosphorus front surface field of sheet resistance 65 Ohm/sq obtained using liquid $POCl_3$ diffusion source, single layer SiNx antireflective coating formed by remote PECVD and screen printed front and rear metallization. Aluminium rear-junction cells are also an interesting and simple approach to study and identify the material limitations (including, for example, multicrystalline n-type substrates). This is an important aspect for the all back-contacted solar cells that have gained a significant scientific and industrial interest [4, 7].

Recently we have reported the application of the screen printed Aluminium-alloyed rear junction concept, reaching an independently confirmed record- high efficiency of 17.4% on n-type floatzone (FZ) silicon wafers (area 140 cm²) [8]. In this paper we compare by experimental tests and modeling the differences of using n-type wafers versus p-type wafers, applying the same processing sequence. On p-type FZ wafers with the same process 17.6% was obtained with FF of 79%, whereas 16.8% was obtained on p-type CZ wafers for FF of 76%. Further, 1D (PC1D) modeling were applied in order to identify possibilities for further n-type cell development using the Al-back junction concept. In particular, the processing of the rear emitter and phosphorus FSF has been considered as well as the influence of the front and rear surface recombination velocities (SRV).

2 EXPERIMENTAL PROCEDURE

The cell development was mainly focussed on 148.5 cm^2 n-type and p-type monocrystalline silicon wafers, but results on 156.25 cm^2 industrial p- and n-type multicrystalline silicon (mc-Si) wafers are also presented in this paper. The cell preparation was based on in-line processing for diffusion, co-firing, and on process steps which can be industrialized. It started with a texture etch (industrial isotexture, or random pyramids) of the surface. Then the front-surface field (n-type wafer) or

front emitter (p-type wafer) was formed by phosphorus diffusion in an infrared conveyor belt furnace from a spin-on source. To improve the accuracy of our modeling, and investigate the potential improvements in cell efficiency by improvement of the front properties, two front diffusions were tested: one standard diffusion resulting in a sheet resistance ≈ 60 Ohm/sq and one diffusion for improved front surface properties (sheet resistance of 75 - 80 Ohm/sq). Subsequently, a rear side polishing etch was carried out followed by the phosphorus glass removal and the PECVD SiN_x anti-reflection coating deposition on the front side. This process sequence did not further require wafer dicing or other methods for junction isolation, and thus the entire initial wafer area was used. The silver grid was then screen-printed on the SiN_x front side, followed by screen-printing of Al on the whole rear side of the cell. Both contacts were co-fired in an infrared conveyor belt furnace, thus forming also the p^+ emitter (n-type wafer) or BSF (p-type wafer) at the rear.

3 N-TYPE CELLS: EXPERIMENTAL RESULTS AND MODELING

3.1 Effect of base resistivity and front diffusion

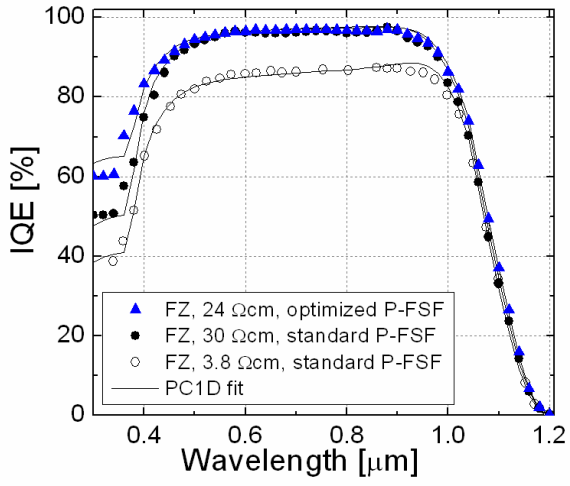
The effects of the base resistivity and the front diffusion have been investigated on n-type cells processed using the Al-back junction concept on mc-Si and FZ substrates. The best cell parameters are summarized in Table I. For both cell types the highest n-type cell efficiency is obtained for high substrate resistivity. This is in agreement with our previous results [8] and the model calculations [9,10], which show that, in order to benefit from the full potential of this type of solar cell, the wafer resistivity should typically be higher than 10 Ohm.cm.

Table I: Effect of base resistivity and front diffusion on n-type FZ and mc-Si cell properties. All cell surfaces are isotextured. Above dashed line: standard front diffusion and front surface passivation. Below dashed line: optimized front diffusion and front surface passivation. The area of the solar cells is 156.25 cm^2 for mc-Si cells and 148.5 cm^2 for monocrystalline cells.

wafer	ρ [Ωcm]	J_{sc} [mA/cm^2]	Voc [mV]	FF [%]	η [%]
mc	0.8	19.77	589	73.7	8.6
mc	12	29.7	580	72.1	12.4
FZ	3.8	30.74	620	77.9	14.9
FZ	24	34.25	627	74.8	16.1
FZ	30	34.18	621	77.4	16.4
mc	25	31.4	582	74.5	13.6
FZ	24	34.75	626	77.2	16.8

Currently we are investigating ways to reduce the front SRV of the rear junction of cells and, thus, to further improve their efficiency. One approach is the modification of the phosphorus FSF (P-FSF) diffusion. It has been shown that lighter FSF doping is helpful for reducing recombination and increasing the Jsc, however at the same time a functional series resistance should be maintained [7, 11, 12]. Therefore in our case for the optimized diffusion the sheet resistance of the FSF was kept in the range of 75 – 80 Ohm/sq. In the lower part of Table I (below dashed line) the results are shown for an improved phosphorus diffusion and front surface passivation. It is observed that a slightly higher J_{sc} is achieved by engineering the FSF diffusion and improving the cell process. At the same time no significant influence on Voc is observed. Due to the differences in the Rsheet of the phoshorus FSF, different pastes and firing conditions have been used for the front metallization which resulted in variation in cell-FF. In other experiments we also observed improvements in V_{oc} up to 12 mV due to the improved front diffusion [8]. However, the V_{oc} results show more scatter.

The IQE plots in Figure 1 top and bottom, respectively, demonstrate the improvement of the IQE collection efficiency with increasing substrate resistivity for both FZ and mc-Si types of wafers. Even though the IQE for the rear junction cells does not reach 100% the best results are obtained for the FZ high resistivity cells. The corresponding front surface recombination velocity (SRV) from the PC1D fit is $(2.0\pm0.5)\times10^5$ cm/s for the FZ-cells with optimized P-FSF and $(6.0\pm1)\times10^5$ cm/s for the standard processing. In both cases the assumed bulk life time was 1.1 ms which is high enough not to limit the device performance. In contrast, for the mc-Si material, the bulk lifetime is an additional factor that limits the device performance [8]. For the lower resistivity mc-Si wafers a bulk life time of 28 µs has been estimated from the PC1D fit. These wafers show the lowest efficiency of 8.6%. The high resistivity FZ and mc-Si wafers with optimized P-FSF were processed at the same time with comparable FSF-sheet resistance. Therefore the front SRV is expected to be in the same range. Under this condition the life time for the high resistivity mc-Si wafers is obtained to be (88±5) µs from the PC1D fit. It has been shown that the ratio between the diffusion length and the substrate thickness (L_d/W) must be higher than 2.5 for a good cell performance [13]. In our case the mc-Si cell thickness was (190±5) µm therefore the material quality is a limiting factor to the cell efficiency.



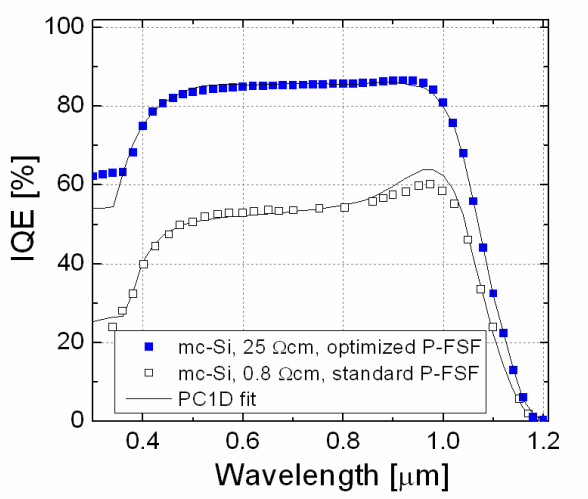
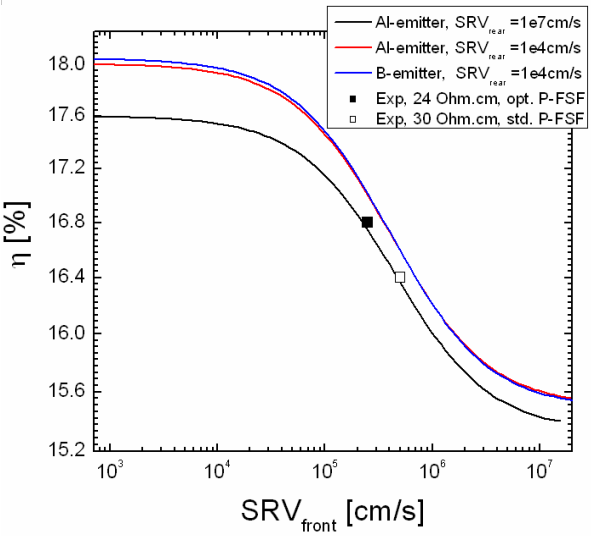


Figure 1: IQE experimental plots and PC1D modeling of the FZ (top) and mc-Si (bottom) isotextured cells of different resistivity and phosphorus FSF.

3.2 Improvement of the cell performance – model analysis

The effect of the lower front SRV on the conversion efficiency improvement has been modelled for isotextured FZ and mc-Si wafers for varied rear SRV. In case of FZ wafers with standard Al rear emitter (rear SRV of $1x10^7$ cm/s) the analysis shows a possibility to achieve above 17.5% for front SRV of $<10^4$ cm/s (Figure 2 top). The model analysis using random pyramid textured wafers shows that even higher efficiencies above 18% can be obtained [8]. In this case both Jsc and Voc have been improved. For the mc-Si n-type cells under the same conditions, the front SRV has lower importance for the improvement of the device efficiency (Figure 2 bottom) which is in agreement with the finding that for the used wafer resistivity and thickness the cell performance is dominated by the low material quality and presence of crystal defects. This interpretation is further supported by the LBIC images (discussed in the next section) which show that the used n-type mc-Si wafers originate from the edge of the ingot. Cell efficiencies as high as 14.4% have been achieved for wafers from the centre of the ingot and resistivity of 50 Ohm.cm and thickness of 180 μm [10].



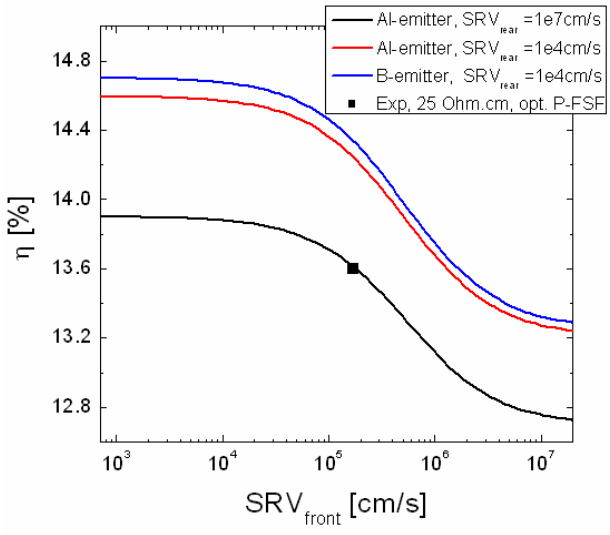


Figure 2: Modeling of the efficiency increase by improvement of the front SRV of isotextured n-type solar cells processed using FZ (top) and mc-Si wafers (bottom). The different curves in each plot represent variations in the rear SRV due to better rear emitter passivation obtained by using aluminium or boron.

We have evaluated the possibility for further efficiency improvement by modeling the effect of a reduced rear-SRV. The resultant plots are also shown in Figure 2. In case of front- and rear SRV of approximately 10^4 cm/s the cell efficiency reaches 18% for isotextured FZ wafers (Figure 2 top). A rear SRV value of $(1+0.3)x10^4$ cm/s has been recently reported [14] for Al-emitters passivated using amorphous silicon layers obtained by low temperature PECVD. The substitution of this rear SRV value in the PC1D model for our results showed the possibility to increase the FZ cell efficiency to approximately 17%, under the presence of our current front SRV. It should be noted, however, that the a-Si-passivation method for the Al-emitter would require a suitable adjustment of the rear metallization technique, e.g. evaporation of Al grid or sputtering which is better compatible with industrial applications. The model calculations show that the improved passivation of the Al-rear emitter has a higher impact on the efficiency of the mc-Si wafers (Figure 2 bottom). For the current front SRV the cell efficiency increases to 14.2%. Lower front SRV of $<10^4$ cm/s results in further efficiency increase of 0.4% absolute. This effect is mainly due to the improved Voc which is more pronounced for mc-Si compared to the FZ cells (Figure 3). It should be noted that the rear SRV has almost no effect on the Jsc for both FZ and mc-Si n-type wafers (plots not shown).

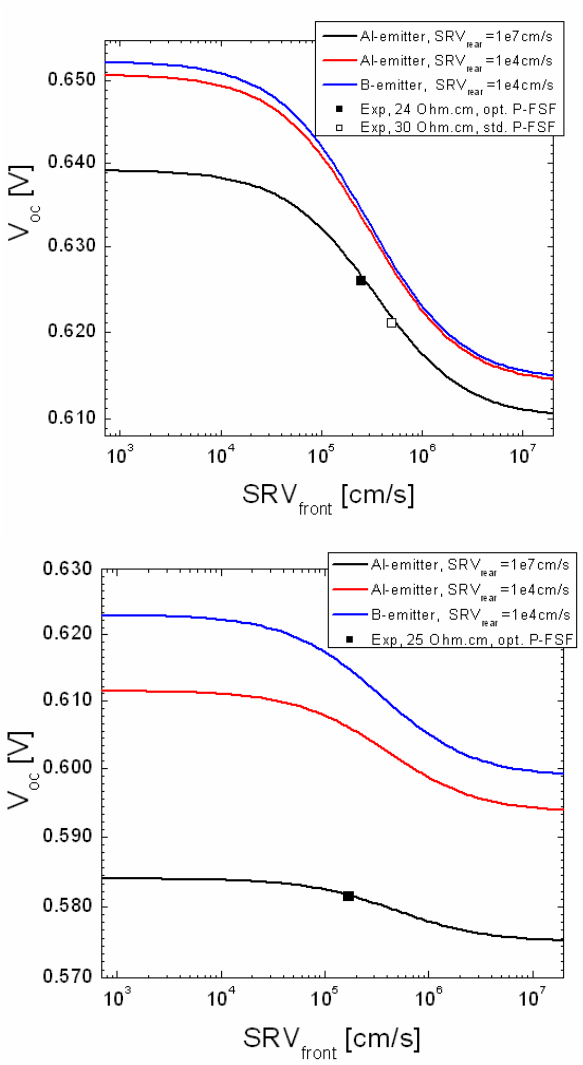


Figure 3: Modeling of the effect of the front SRV on the cell Voc of isotextured n-type solar cells processed using FZ (top) and mc-Si wafers (bottom). The different curves in each plot represent variations in the rear SRV due to better rear emitter passivation obtained by using aluminium or boron.

Another possibility to process a passivated rear emitter which is compatible with low rear SRV is to exchangee the aluminium with boron emitter. Recently in our group [15] has been reported the successful passivation of industrially produced B-doped emitters by using a stack of wet-chemical SiO_2/PECVD-SiNx layers. We have evaluated using PC1D the possibility for efficiency increase by using such a B-emitter in the rear junction n-type cells. For an emitter sheet resistance of 60 Ohm/sq a rear SRV of $<10^4$ cm/s should be possible. According to the model the performance of the FZ cells is not changed significanly when boron is used instead of aluminium for the rear emitter processing provided that the rear SRV is at the same low value. In case of mc-Si cells there is a modest efficiency increase of about 0.1% absolute and Voc improvement by 7 mV for the current experimental front SRV.

4 PERFORMANCE COMPARISON BETWEEN N-TYPE AND P-TYPE SUBSTRATES WITH SIMILAR CELL PROCESSING

4.1 Best cell efficiencies

A summary of the best cell performance for n-type and p-type substrates is shown in Table II

Table II: Parameters of the best cells processed under identical conditions. The cell area is the same as in Table I, ST – denotes the corresponding surface texture, (*) cell data from [VMi 2007].

Si	ST	ρ [Ωcm]	Jsc [mA/cm^2]	Voc [mV]	FF [%]	η [%]
n-mc	IS	25	31.4	582	74.5	13.6
p-mc	IS	1.5	33.5	603	76.6	15.5
n-FZ*	IS	31	33.27	633	78.8	16.6
n-FZ	IS	24	34.75	626	77.2	16.8
n-FZ*	RP	31	35.53	632	77.4	17.4
p-FZ	RP	2.4	35.52	626	79.0	17.6
p-CZ	RP	1.1	35.76	617	76.0	16.8

The experimental data shown in Table II demonstrate that, for the diffusion parameters used, the two types of FZ wafers do not differ much. This result is further supported by the IQE plots in Figure 5 which are indeed comparable. However, compared to the p-type CZ wafers the n-type process performs better. The expectation for n-type CZ material is that it will perform as well as n-type FZ, however n-type CZ wafers of appropriate resistivity were not available for the tests.

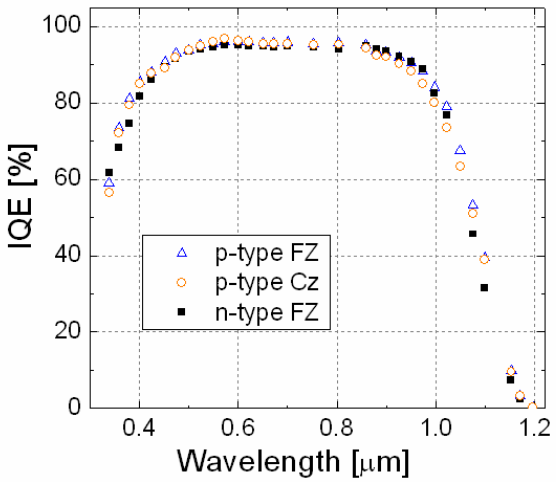


Figure 5: Internal quantum efficiency (IQE) data of the best monocrystalline p-type and n-type solar cells.

Concerning the n-type mc-Si it has been shown that it is difficult to obtain sufficient performance for the used wafer resistivity and thickness [9, 10]. Furthermore, it should be noted that the p-type wafers used for the comparison originate from the upper part of an ingot, which results in some reduction of the cell efficiency due to increased crystal defect density. A comparison between the local light beam induced current-data of both types mc-Si wafers is shown in Figure 6.

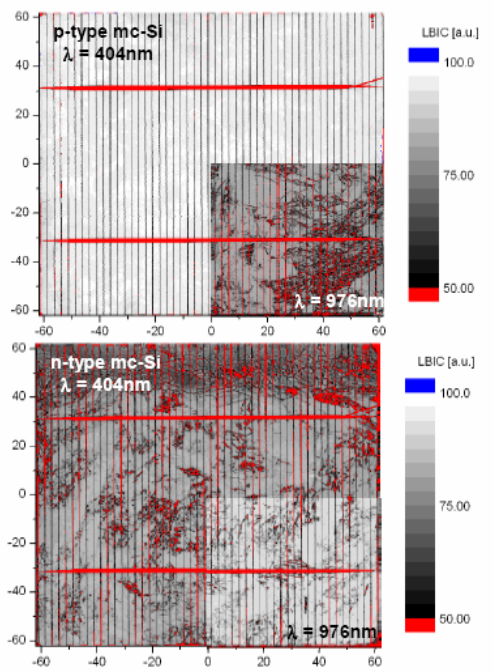


Figure 6: Local light beam induced current data of the p-type (top) and n-type (bottom) mc-Si solar cells from Table II. The light wavelength was 404 nm. Bottom right insets in both images: wavelength of 976 nm. Same scale in both figures.

5 CONCLUSION

We have compared the performance of n-type and p-type silicon solar cells fabricated using identical low cost industrially compatible process. The best results achieved are 17.4% for large area monocrystalline n-type FZ substrates, representing a record efficiency, 17.6% p-type FZ (FF of 79%) and 16.8% p-type CZ (FF of 76%). In addition, by applying PC1D modeling the possibilities for efficiency improvement of the n-type cells have been evaluated especially concerning the front and rear SRV as well as the rear emitter processing. High efficiencies may also be conceivable on n-type multicrystalline substrates if those can be produced with high lifetime and, especially, high homogeneity.

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