HIGH EFFICIENCY INDUSTRIAL SCREEN PRINTED N-TYPE SOLAR CELLS WITH FRONT BORON EMITTER

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ABSTRACT

There is currently much interest in n-type base cells because of potential advantages, both of silicon base material and of cell process, for high efficiency. We present results of n-base solar cells on large area multicrystalline and monocrystalline silicon wafers, produced using simultaneous diffusion of phosphorus back surface field and boron emitter, screen-printed metallization and firing through. The cell process leads to record high efficiencies of 16.4% on mc-Si and 18.3% on monocrystalline wafers. We also consider material-related cell characteristics. It is experimentally demonstrated that in mc-Si a low resistivity is correlated to reduced cell efficiency, with the optimum base resistivity lying between 1.5 and 4 Ohm-cm. By characterising and modeling cells from monocrystalline Si, from nominally clean mc-Si, as well as from intentionally Fe-contaminated mc-Si, the impact of the mc-Si wafer purity on emitter properties is investigated in more detail.

INTRODUCTION

N-type silicon has been proven to have a higher tolerance to common transition metal impurities, such as those present in silicon produced from quartz and carbon (via metallurgical routes), potentially resulting in higher minority carrier diffusion lengths compared to p-type substrates [1,2]. In spite of these advantages, at present, more than 85% of the silicon solar cells produced by the industry are based on p-type substrates. This is caused mostly by an insufficient development and industry implementation of the n-type cell processes for multicrystalline substrates.

This paper presents a solar cell process and cell results on n-type multicrystalline and monocrystalline wafers. The cell process is based on boron front emitter, and low cost fabrication processes for industrial use (such as screen printing and microwave plasma enhanced chemical vapour deposition (PECVD) of silicon nitride (SiNx)). We show that good passivation of p^+ emitters can be achieved on highly doped boron emitters (≈60 Ω/□), using an ultrathin oxide grown by wet chemical means prior to the SiN_x deposition. Moreover, it is experimentally demonstrated that in mc-Si a low resistivity is correlated to reduced cell efficiency, with the optimum base resistivity lying between 1.5 to 4 Ωcm. By characterising and modeling cells from monocrystalline Si, nominally clean mc-Si, as well as intentionally Fe-contaminated mc-Si, also the impact of the wafer purity on emitter properties is investigated.

CELL PROCESS AND RESULTS

Inline versus batch process for boron diffusion

Due to asymmetric capture cross sections of the recombination centres of many transition metal impurities in multicrystalline silicon, n-type doped substrates are expected to be more favourable for high efficiency than a p-type doped substrate [1,2]. However, in order to realize an emitter on the n-type Si substrate, a p^+ diffusion (usually boron) should be performed. The diffusion of boron requires a temperature higher than 900ºC and boron does not have such a significant gettering effect as phosphorus [3]. Therefore, sources of contamination should be kept away more carefully than in the case of phosphorus (n^+) diffusion [4].

We have made a comparison of two diffusion processes for boron emitters [5]: an inline process, where the emitter diffusion is carried out in a conventional infrared-heated conveyor furnace using a metal belt, and a batch process where diffusion is conducted in a horizontal quartz tube furnace with an industry-compatible scale (maximum load of 400 wafers of 15.6×15.6 cm^2). Several different boron sources were investigated, such as a commercial boron paste, a commercial boron liquid, and a boron tribromide (BBr_3) liquid bubbled by N_2.

A poor performance was obtained for inline belt furnace diffusion of boron emitters, with only a slight advantage for diffusion from liquid boron source compared to printed source. After double-sided diffusion, an effective lifetime of just 22-25 µs and an implied V_{oc} of just 581 mV indicated that substantial contamination occurs during diffusion in the belt furnace [3].

The necessity of a clean process was further strengthened by the results of tube furnace diffusion of boron paste or liquid, which showed up to a factor 4 higher lifetime, and an implied V_{oc} higher by more than 35 mV. In that case the tube furnace was used only for the temperature step (drive-in).

However, a far better performance was obtained for BBr_3 diffusion. This can probably be understood by the fact that the quartz tube furnace diffusion using BBr_3 liquid bubbled by N_2 does not have any metal inside the tube, in contrast to the belt furnace, and, additionally, it does not use either paste or liquid sources of boron which are more likely to incorporate unexpected contamination. As a result, the BBr_3 diffusion results in a much more contamination-free p^+-emitter, with a factor of ten lower emitter recombination current density. Such a low

recombination current density of the boron emitter agrees well with literature values [6, 7].

Passivation of the boron emitter

One of the major development areas of the n-type mc-Si solar cell process remains the passivation of the front side boron emitter. Since the conventional way to passivate n^+ emitters for the p-type solar cell process, using a PECVD-SiN_x layer, results in a poor or no passivation for p^+ emitters, a new way of passivating p^+ surfaces needs to be developed [8, 6]. We have developed a new method to passivate p^+ emitters which brought new potential to the n-type mc-Si industrial solar cell process [9]. This method relies on the same PECVD SiN_x technology as is widely used in industry to passivate n^+ (phosphorus) emitters, which is industrially applicable with no substantial increase in cost or process time.

The method employs an ultrathin silicon oxide between the emitter and the SiN_x. The oxide is created by wet chemical means, i.e., by immersion in nitric acid (at room temperature): NAOS or nitric acid oxidation of silicon. An almost 6-fold enhancement in the lifetime and 60 mV higher implied V_{oc} is observed for lifetime test devices after firing. These values outperform even the results obtained using thermal SiO_2/SiN_x stacked layers as a passivation method [8, 6]. Since the method employs a low-temperature oxidation process, possible deterioration of, e.g., the base material, is minimized.

As reported previously [5, 9], an enhancement in solar cell efficiency of about 2% absolute was achieved using the NAOS/SiN_x passivation method as compared with the standard SiN_x passivation method industrially used for phosphorus emitter passivation. The profound effect on boron emitter passivation can be observed in the strong enhancement of the IQE for wavelengths below 700 nm. Consequently, the V_{oc} and J_{sc} of the cell are increased.

Solar cells on n-type mc-Si and monocrystalline wafers

Having identified the importance of a clean B-diffusion, the development of n-type multicrystalline process was based on the BBr_3 diffusion. The solar cells based on n-type substrates must have an n^+ (phosphorus) diffusion for a back surface field (BSF), in order to facilitate the formation of an Ohmic contact for the base metallization. We found that the best results are obtained when the phosphorus BSF layer is diffused simultaneously with the BBr_3. Additionally, simultaneous diffusion shortens the total process time, and may give the most effective use of phosphorus gettering. A schematic layout of the final solar cell is given in Fig. 1.

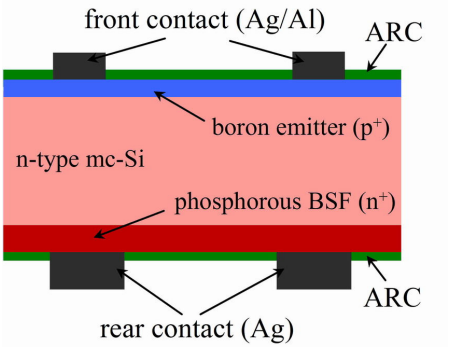

Fig. 1. Schematic cross-section of the n-type solar cell.

Table 1 shows the best solar cell parameters obtained using this process. The efficiencies of 16.4% for isotextured mc-Si, and 18.3% for random pyramid textured Cz, are to our knowledge the best efficiencies obtained for such low cost screen printing technology on n-type Si substrates (the high-efficiency cells of Sunpower and Sanyo on n-type substrates are the obvious exceptions).

Si	Jsc [mA/cm^2]	Voc [mV]	FF [%]	η [%]
mc	35.2	607	76.7	16.4
Cz	38.2	627	76.6	18.3

Table 1. Comparison of the best solar cell parameters. The solar cells were fabricated on isotexture etched n-type mc-Si wafers (with area of 156.25 cm^2), and alkaline etched monocrystalline wafers (with area of 155.72 cm^2). Boron-diffusion (60 Ω/□ emitter) was done in a tube furnace, and standard screen printed metallization was used. Average efficiency of the 10 monocrystalline cells was 17.9%.

One of the most important criteria for commercialization of solar cells is their stability under normal operational conditions of temperature and illumination. Our passivation method for p^+ emitters is very effective but it must also be stable during the operational lifetime of a solar cell. Therefore, accelerated aging tests under the influence of illumination and an elevated temperature of 60 °C were carried out, in order to study and compare the behavior of the solar cells passivated with the nitric acid SiO_2/SiN_x stack or with SiN_x. Solar cells were light soaked under open-circuit condition for a period of 1000 h by a xenon lamp at one-sun intensity. The lamp light was filtered with a UVB and infrared cutoff filter. During this period, the solar cells received a total radiation dose of 2×10^9 J /m^2 (or 555 kWh/m^2). Even after this extensive light soaking, the cell efficiency decreased by less than 2% relative to the initial value, for both passivation schemes used [9]. This shows that the ultrathin nitric acid SiO_2/SiN_x stack can be expected to be a reliable passivation scheme for p^+ emitters.

Modelling of solar cells

We have investigated solar cells fabricated on wafers belonging to different n-type mc-Si ingots. The ingots differed in their base resistivity and in their contamination levels. The purpose was two-fold: find out the optimum resistivity range for n-type mc-Si ingots and cells [10]; and find out any effects of substrate quality on emitter recombination.

The experimental IQE of solar cells were fit with PC1D using the measured front and rear doping profiles, surface reflection, base resistivity, and wafer thickness. The relevant fit parameters left for the modelling are the bulk lifetime, and the front and rear surface recombination velocities (SRV), and the amount of impurity in the p-type emitter. By fitting both front and rear IQE data and I-V results, all fit parameters can in fact be determined independently. The results show a constant front SRV of $\approx 1\times10^4$ cm/s (on boron emitter) and rear SRV of $\approx 1\times10^5$ cm/s (on phosphorus BSF).

EFFECT OF BASE RESISTIVITY

Two mc-Si n-type ingots from the same furnace were used for this investigation. A compensated ingot (labeled ingot 5) was partially p-type and partially n-type, due to doping with boron as well as phosphorus. Such a compensated ingot is very well suited for this type of investigation as it allows for a large variation in wafer resistivity on a narrow part of the ingot size where variation in concentration of metal impurities and crystal defects is relatively small. The other n-type ingot (labeled ingot 6) had resistivity ranging from 2.2 to 0.3 Ωcm from bottom to top of the ingot. Solar cells were fabricated, using the process described above, on 12.5×12.5 cm^2 wafers distributed to cover a resistivity range of 0.8 to 7.7 Ωcm from ingot 5 and 0.3 to 2.1 Ωcm from ingot 6.

Fig. 2 shows the experimental conversion efficiencies and $J_{sc}\times V_{oc}$ product as a function of base resistivity for both ingots. It can be seen that the best results are obtained for wafers belonging to ingot 6, with the highest performance obtained around 25% from the bottom of the ingot.

Fig. 3 shows IQE data, and Fig. 4 shows the τ_b resulting from fitting the IQE data, of the cells from both ingots investigated. A resistivity higher than approximately 1.3 Ωcm is required in order to ensure Ld>W (W is the averaged wafer thickness of all investigated cells) for both ingots. For Ld<W, that means a resistivity <1.3 Ωcm, both ingots have almost identical lifetime even though this threshold occurs for wafers of >50% towards the top of the ingot 6 and only >85% towards the top of ingot 5. Notably, the lifetime as a function of resistivity shows for low resistivity a linear dependence, suggesting activity of some impurity which is relatively harmful in n-type base (e.g. Au, Zn, perhaps Cr) [10, 1, 11].

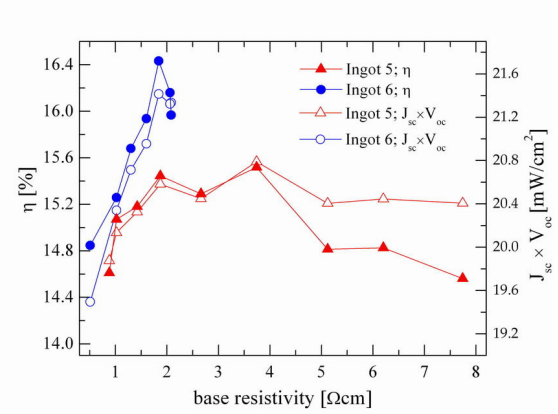

Fig. 2. Experimental power conversion efficiency (η) and $J_{sc}\times V_{oc}$ product versus base resistivity of both mc-Si ingots investigated. The record high efficiency of 16.4% is obtained for wafers close to the bottom of ingots 6.

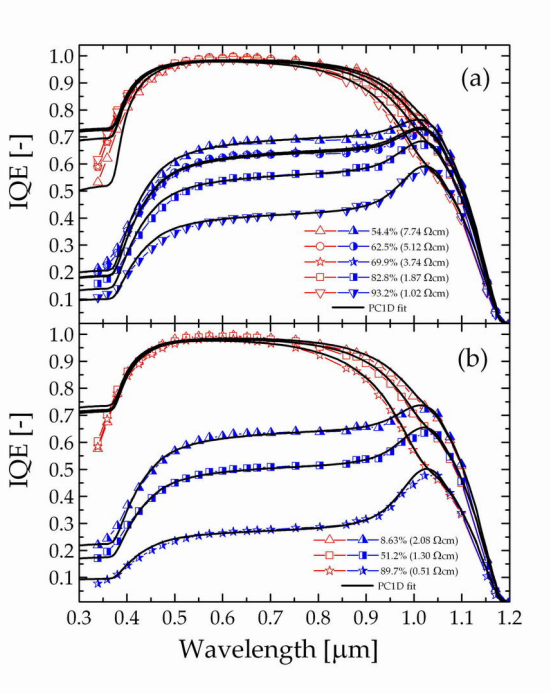

Fig. 3. Internal quantum efficiency for front (empty symbols) and rear side (semi-filled symbols) illumination of solar cells selected from ingot 5 (a) and ingot 6 (b). The legend indicates the wafer's resistivity as well as its position towards the top of the respective ingot. The solid lines represent the PC1D calculation.

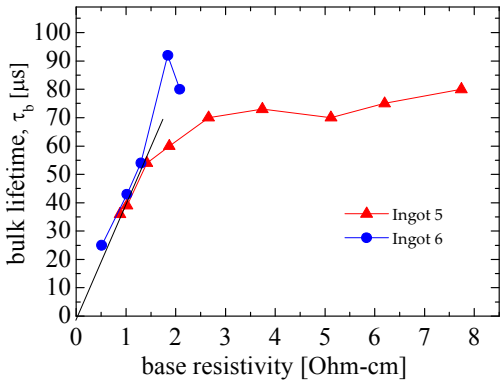

Fig. 4. Minority carrier lifetime in the bulk (τ_b) as a function of wafer base resistivity, determined from the PC1D fit of IQE data.

An interesting result that can be observed in Fig. 2 is that the $J_{sc}\times V_{oc}$ product continues to rise for cells made from ingot 6 as resistivity is increased while it stays rather constant for cells of ingot 5 for all wafers with Ld>W (resistivity>1.3 Ωcm). Above 3.5 Ωcm a decrease in efficiency of ingot 5 is caused by a decrease in FF. This decrease in FF is a result of a higher series resistance caused by a non-optimised metallization grid of the base contact.

These results show that the optimum target resistivity for n-type mc-Si wafers lies between 1.5 to 4 Ωcm (these values can be lower if thinner wafers are produced) in order to maximize the efficiency output throughout the ingot. Note that for the same doping level, a p-type substrate will have a resistivity that range from 4 to 11.8 Ωcm, far higher than what is currently used in production (0.5-2 Ωcm).

EFFECT OF CONTAMINANTS IN WAFER

While the n-type base of the solar cells may be expected to be less sensitive to many impurities, the p^+ emitter could rather be more sensitive. Therefore the PC1D model included a contamination of the emitter. It was found that consideration of this contamination was essential to simultaneously fit IQE-curves as well as V_{OC} correctly. To verify that contamination of the p^+ emitter can indeed have a significant effect, cells were processed by identical processes from clean monocrystalline (Cz) wafers, nominally clean mc-Si wafers, and mc-Si wafers from feedstock intentionally contaminated with 50 ppmw of Fe. Two mc-Si ingots from the same furnace (differing from the previous section) were investigated. Resulting IQE curves are shown in Fig. 5. The front IQE clearly does not indicate that there is a variation in front surface passivation. However, without including recombinating defects in the emitter, the PC1D calculated V_{OC}, and the real measured V_{OC}, deviate. The deviation varies from 6 mV for the Cz wafers, to ≈22 mV for the Fe-contaminated wafers. This deviation can be fitted well (without affecting the IQE curves) by including interstitial Fe defects in the emitter.

wafer	F-SRV [cm/s]	R-SRV [cm/s]	L_d-bulk [µm]	L_d-emitter [µm]	ΔV_{oc} [mV]
Mono Cz	4e4	1e5	841	0.56	6
FS2-102	1e4	1e5	284	0.47	14
FS7-136	1e4	1e5	192	0.41	22

Table 2. PC1D fit parameters used in Fig. 5. L_d-emitter is taken at $N_A=10^{20}$ cm^{-3}, whereas ΔV_{oc} represents the difference between calculated V_{oc} without considering recombination into emitter and measured V_{oc} of the cells.

Incidentally, it can be seen that the 50 ppmw of Fe have only modest effect on the diffusion length in the base of the solar cells.

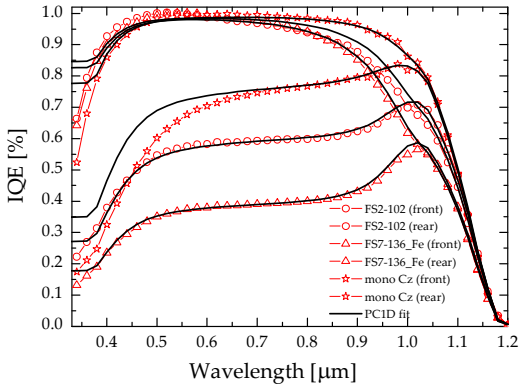

Fig. 5. Internal quantum efficiency for front and rear side illumination of solar cells selected from Cz, reference mc-Si (FS2-102), and a mc-Si ingot with 50 ppmw Fe (FS7-136). The solid lines represent the PC1D calculation, including the fit parameters listed in Table 2.

CONCLUSIONS

We have demonstrated a process to fabricate n-type solar cells on large area (12.5cm x 12.5cm) multicrystalline and Cz substrates, involving simultaneous diffusion of phosphorus BSF and BBr_3 emitter, screen-printed metallization and firing through, leading to efficiencies of 16.4% on multicrystalline Si and 18.3% on Cz.

A simple and cost-effective method to passivate the p^+ (i.e., boron) doped emitters, based on nitric acid oxidation of the silicon emitter, and deposition of PECVD SiN_x, has been developed. Concerning boron diffusion, we have obtained far better performance for a process performed in a quartz tube furnace using tribromide (BBr_3) liquid bubbled source than using printed or spin-on sources, or a conveyor belt furnace.

Experiments on wafers of different base resistivity show that the optimum target resistivity for n-type multicrystalline silicon wafers lies between 1.5 to 4 Ωcm

(these values can be lower if thinner wafers are produced) in order to maximize the efficiency output thorough the ingot. In mc-Si cells, modelling gives a clear indication that contaminants inside the wafer affect the emitter recombination.

ACKNOWLEDGEMENTS

The authors would like to thank ECN colleagues; FOXY partners; Tempress for collaborative work concerning the BBr3 diffusion furnace; Lucilla Bittoni, Chimet Spa, for the kind supply of the front side metallization paste. This work was supported by the European Commission within the FoXy project, and by the Dutch agency for energy and the environment SenterNovem.

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