Available online at www.sciencedirect.com
ScienceDirect
Journal of Non-Crystalline Solids 354 (2008) 2386–2391
JOURNAL OF NON-CRYSTALLINE SOLIDS
www.elsevier.com/locate/jnoncrysol

Back contacted a-Si:H/c-Si heterostructure solar cells

M. Tucci [a,*], L. Serenelli [b], E. Salza [a], S. De Iuliis [b], L.J. Geerligs [b], D. Caputo [c], M. Ceccarelli [c], G. de Cesare [c]

[a] ENEA Research Center Casaccia, Via Anguillarese 301, 00123 Roma, Italy
[b] ECN Solar Energy, P.O. Box 1 NL-1755 ZG Petten, The Netherlands
[c] Department of Electronic Engineering University ' Sapienza', via Eudossiana, 18, 00184 Roma, Italy

Available online 5 February 2008

Abstract

This paper shows how the amorphous/crystalline silicon technology can be implemented in the interdigitated back contact solar cell design. We have fabricated rear-junction, backside contact cells in which both the emitter and the back contact are formed by amorphous/crystalline silicon heterostructure, and the grid-less textured front surface is passivated by a double layer of amorphous silicon and silicon nitride, which also provides an anti-reflection coating. The entire self-aligned mask and photolithography-free process is performed at temperature below 300 °C with the aid of one metallic mask to create the interdigitated pattern. An open circuit voltage of 687 mV has been measured on a 0.5 Ωcm p-type monocrystalline silicon wafer. On the other hand, several technological aspects that limit the fill factor (50%) and the short circuit current density (32 mA/cm^2) still need improvement. We show that the uniformity of the deposited amorphous silicon layers is not influenced by the mask-assisted deposition process and that the alignment is feasible. Moreover, this paper investigates the photocurrent limiting factors by one-dimensional modeling and quantum efficiency measurements.

PACS: 79.60.Jv; 73.61.Jc

Keywords: Solar cells; Heterojunctions; Photovoltaics

1. Introduction

Recently, there has renewed industrial interest in high efficiency silicon solar cells, motivated by the large leveraging effect that higher cell efficiency has in reducing overall photovoltaic module and system costs, although these savings are offset by the more complicated processing required [1–3]. In the rear-junction, back contact solar cell design interdigitated n^+ and p^+ diffusions and grid lines are used to collect photogenerated carriers entirely from the rear of the cell. The advantages of this structure include no contact grid shading on the sunward side and potentially low wafer cost due to the use of a thin substrate, although high diffusion length and low front surface recombination are required to maintain high carrier collection needed for high efficiency. Moreover, the interdigitated back contact (IBC) technology allows the improvement of the module active area fraction [4,5]. On the other hand, Sanyo's HIT structure enables an excellent surface passivation of c-Si surface defects, including the contacts, by high-quality intrinsic a-Si:H layers, thus resulting in high efficiency, especially a high open circuit voltage (V_{oc}): almost 730 mV has been reached [6]. The low temperature processes (<200 °C) result in an advantage for thinner c-Si wafers. Indeed high temperature processes produce stress and bowing when c-Si wafers are thinner than 160 μm. Moreover, the temperature coefficient of HIT cells is better than the conventional c-Si solar cells and results in a higher output power at high temperatures [7,8]. Finally, the implementation of amorphous/crystalline silicon (a-Si:H/c-Si) heterojunction as solar cell concept has the capability of reaching efficiencies up to

* Corresponding author. Tel.: +39 0630484095; fax: +39 0630486405.
E-mail address: mario.tucci@casaccia.enea.it (M. Tucci).

0022-3093/$ - see front matter © 2008 Elsevier B.V. All rights reserved.
doi:10.1016/j.jnoncrysol.2007.09.023

25% [9]. Thus, it would be useful to know whether the passivation of the metallic contact areas using a-Si:H would be a practical way of improving open circuit voltage.

Here we show how the heterostructure technology can have a chance in the challenge of the IBC solar cells. We present an innovative design of the solar cell in which both the emitter and the back contact are formed by (a-Si:H/c-Si) heterostructure and placed at the rear side, and the grid-less front surface is passivated by a double layer of amorphous silicon and silicon nitride (a-Si:H/SiN_x), which also provides an anti-reflection coating [10]. We have named this device BEHIND cell (Back Enhanced Heterostructure with INterDigitated contacts cell). We present the preliminary results on textured p-type monocrystalline silicon wafers; we show that the uniformity of the deposited amorphous silicon layers is not influenced by the mask-assisted deposition process and that the alignment is feasible. We investigate in detail the technological issues, needed to develop our process technology, and analyze the results by individuating ways of improvements with the aid of simulations.

2. Experimental details

We have fabricated 6.25 cm^2 solar cells starting from 4 in. diameter, 250 μm thick, ⟨100⟩ oriented, 0.5 Ωcm p-type, one side polished float-zoned silicon wafers. We have performed a front surface alkaline texturization, while we have chosen the polished side of the wafer as the back side of the cell. Each deposition process has been performed in a three chamber 13.56 MHz direct Plasma Enhanced Chemical Vapour Deposition (PECVD) system, in which each chamber is devoted to a particular doping type. On the whole polished side of the wafer, after a standard RCA cleaning and HF dip, 5 nm thick intrinsic a-Si:H buffer layer and 15 nm thick n-type doped a-Si:H have been subsequently deposited. Then the wafer has been turned over to deposit the passivation/anti-reflection coating. We have preferred to passivate the sunward side by the (a-Si:H/SiN_x) double layer instead of single SiN_x layer, since it has been demonstrated to better passivate crystalline silicon surface with respect to the SiN_x [11]. In turn, we lose part of the blue sun spectrum due to the a-Si:H absorption of the high energy photons. After a native oxide removal by 1% HF, we have chosen to deposit 5 nm and 70 nm of a-Si:H and SiN_x, respectively, to also ensure the anti-reflection against sun spectrum. The two amorphous films have been grown in the same chamber, avoiding interruption of glow discharge to reduce interface damages. To form the p-type contact, we have fabricated a particular metal mask on 100 μm thick Molybdenum foil, on which a comb shape grid has been opened focusing a Nd-YAG laser at a wavelength of 1064 nm. We have fixed this mask on the rear side of wafer by a particular designed holder. A dry etching procedure using NF_3 gas has been performed to remove the n-type a-Si:H portion not covered by the mask, using settings defined on the basis of the previous experiences [12]. We have carefully optimized the dry etching procedure avoiding damages and fluorine radicals contaminations at the silicon surface. After trial and error procedures, we have estimated 30 s as sufficient time to etch about 15 nm of a-Si:H material, which corresponds to the n-layer thickness. To ensure an isolation between the n-type doped a-Si:H edges and the p-type doped a-Si:H areas we have deposited, in the patterned region, a very thin intrinsic buffer layer of about 5 nm prior to the growth of a 15 nm p-type a-Si:H film. Keeping the metallic mask still held on the sample, we have evaporated 2 μm of Al on the p-type a-Si:H to form the base contact. Then we have rotated the mask in the holder of 180 degree and evaporated 2 μm of Ag to contact the n-type a-Si:H layer. We remark that the mask alignment is not critical since the n-type a-Si:H emitter width is three times wider than the p-type a-Si:H region. We have dimensioned the distance between two n-type a-Si:H fingers of the interdigitated combs supposing a diffusion length of minority photogenerated carriers in the order of 400 μm. Schematic diagram of the BEHIND solar cell process is shown in Fig. 1. The process parameters used in PECVD system are summarized in Table 1.

At this stage the BEHIND cells have been characterized in terms of current–voltage (*IV*), both in dark and in AM1.5G conditions, reflectance and quantum efficiency (IQE: internal quantum efficiency; EQE: external quantum efficiency). As we will discuss in the next section, to reduce the series resistance we have irradiated, by a Q-switched Nd-YAG laser, the Al contact following the comb pattern by a PC controlled XY stage that is able to move the sub-

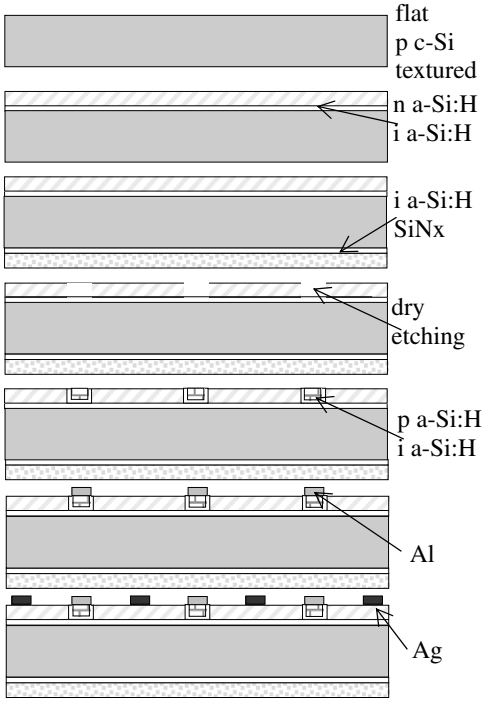

Fig. 1. Schematic diagram of BEHIND cell process.

Table 1
Deposition parameters of BEHIND cells

Process step	RF power (mW/cm^2)	Temperature (°C)	Pressure (m Torr)	Gas flows
i a-Si:H back layer	28	300	300	40 sccm SiH_4
n a-Si:H back layer	28	300	300	10 sccm PH_3/SiH_4 5%; 40 sccm SiH_4
i a-Si:H front layer	36	250	750	120 sccm of 5% SiH_4 diluted in Ar
SiN_x front layer	260	250	750	1.66 as NH_3/SiH_4 gas flows ratio
Dry etching	400	25	50	48 sccm NF_3
p a-Si:H layer	28	300	300	6 sccm of B_2H_6; 40 sccm SiH_4

strate at 10 mm/s under the beam. The used laser settings (wavelength at 1064 nm, mode TEM00, power 320 mW, repetition rate 1 KHz) have been chosen on the basis of previous work [13].

3. Results

The experimental *IV* characteristic in this study has been measured at room temperature, calibrated to 100 mW/cm^2 and AM1.5G illumination and is shown in Fig. 2 as symbols. The 687 mV as open circuit voltage (V_{oc}) value confirms that the uniformity of the deposited amorphous silicon layers is not influenced by the mask-assisted deposition process, the alignment is feasible and the regions where the doped layers can overlap are well isolated by the intrinsic a-Si:H. We remark that at the end of the fabrication process, the cell photocurrent was completely dominated by a very high series resistance. To overcome this problem we have performed a laser treatment over the Al comb, knowing that this treatment is able to promote, in the right conditions [13], Al and B (being within the p-type a-Si:H material) diffusion into the crystalline base, thus producing a less resistive contact, even if in a narrow region. Although the absence of front metal shading should reflect in higher short circuit current (J_{sc}) this does not exceed 32 mA/cm^2, as confirmed by integrating the EQE data over the sun spectrum. A detailed view of IQE, EQE and reflectance measurements is reported in Fig. 3 as symbols. Since the cell rear side is not homogeneous in terms of depletion depth, the QE varies depending on the monochromatic spotlight dimension and position with respect to the fingers of the rear contacts. In Fig. 4, we have compared different QE measurements using a focused spotlight having a dimension comparable to that of single metal finger contact. When a single n-type electrode is illuminated, a hump in the EQE data appears in the spectral region ranging from 900 nm to 950 nm, due to the depletion region that enhances the photogeneration collection toward the n-type a-Si:H layer. In turn, when a single p-type electrode is illuminated, the EQE profile

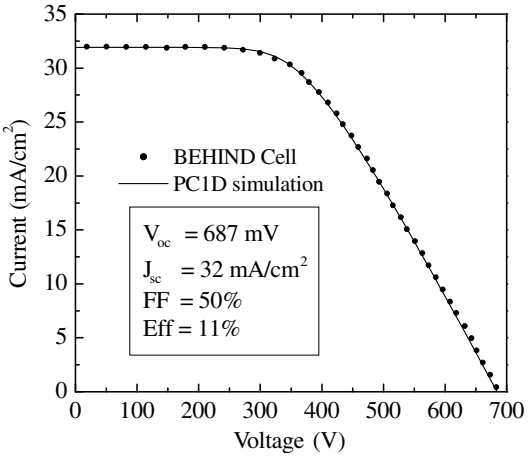

Fig. 2. *IV* measurements and photovoltaic parameters under AM1.5G condition: experimental data (symbols) and PC1D simulations (line). The fit goodness χ^2 is 0.015.

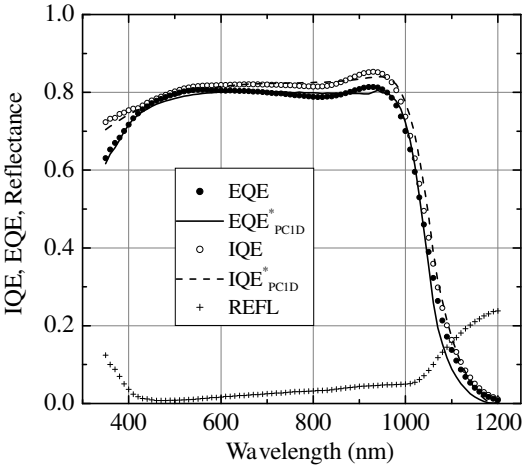

Fig. 3. IQE, EQE, reflectance of the BEHIND cell: experimental data (symbols) and PC1D simulations (lines). The fit goodnesses χ^2 are 0.3 and 0.06 for IQE and EQE, respectively.

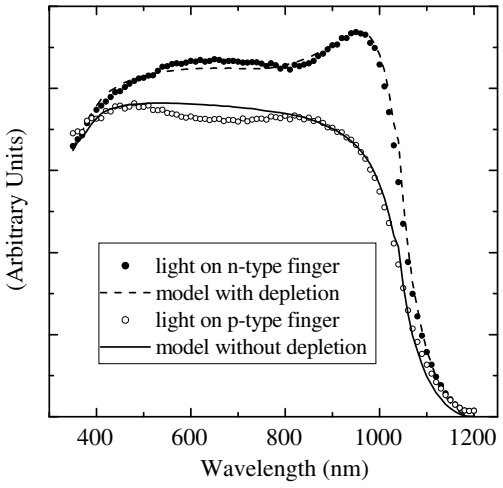

Fig. 4. Comparison of normalized photocurrent, measured using narrow spotlight size shined on different doped fingers of the BEHIND cell. The fit goodnesses χ^2 are 0.16 and 0.06 for data as filled symbols and for data as open symbols, respectively.

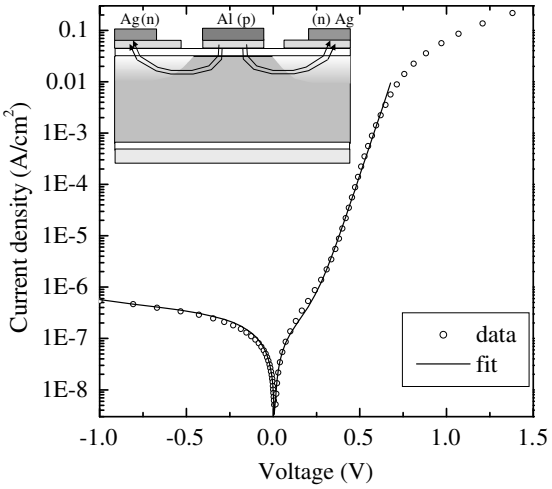

Fig. 5. *IV* experimental data (symbols) and simulation (line), at room temperature and at dark conditions. The fit goodness χ^2 is 0.015. In the inset, it is shown how the dark current flows between rear contacts.

results smooth over the entire spectrum because of the lack of an electric field close to the p-type c-Si/p-type a-Si:H/Al contact.

When the cell is not illuminated the current flows mainly between the rear contacts, so the *IV* characteristic at room temperature and in dark conditions, reported in Fig. 5 as symbols, can help to verify the presence of shunts and recombination paths between electrodes.

4. Discussion

Our approach to BEHIND cell fabrication is focused on several issues, but the main idea is to develop an innovative IBC technology entirely performed at low temperature (<300 °C), thus resulting in an advantage for thinner wafers; involving a self-aligned mask-assisted and photolithography-free process and that could benefit from the passivation quality of the a-Si:H. If the rear-junction and backside contact design enjoys reduced optical shading losses, then it also requires high bulk lifetime and low front surface recombination. At this stage of our research activity, is really difficult to imagine the reliability of the entire process, but we can ensure that all the steps have been deeply investigated to find an easy way to implement them into our solar cell process.

As mentioned, the J_{sc} value is less than the expected one due to both optical and recombination losses. The photocurrent is mainly due to electron diffusion in the p-type doped crystalline base, plus a contribution of depletion due to the backside position of the p–n heterojunction. So the BEHIND design is able to overcome the problem of emitter absorption that still affects the n-type a-Si:H/p-type c-Si heterostructure solar cell, due to low band gap of the n-type a-Si:H layer that does not exceed 1.65 eV [14]. The key issues to obtain high J_{sc} depends on diffusion length, L_d, and surface recombination velocity, $S_{n,p}$. To explore the effect of both parameters we have compared the EQE experimental data with a PC1D [15] simulation, in which we have simplified our BEHIND cell into one-dimensional crystalline based solar cell having a back thin n-type a-Si:H emitter layer. A detailed description of the parameters adopted in the simulation is reported in Table 2. These parameters have been fixed on the basis of both c-Si and a-Si:H properties and on geometrical characteristic of the cell. Choosing appropriate L_d and $S_{n,p}$ values, and taking into account the measured reflectance profile, reported in Fig. 3 as symbols, we have obtained a good agreement between experimental data and simulation model, except in the region of higher energy photons, since the simulation does not account for the passivation/anti-reflection coating absorption. So at the end of EQE simulation, these data have been reduced by the a-Si:H thin layer ($d = 3$ nm) absorption as follows

$$\mathrm{EQE}^{*}_{\mathrm{PC1D}}(\lambda) = \mathrm{EQE}_{\mathrm{PC1D}}(\lambda) \cdot \mathrm{e}^{-\alpha_{\text{a-Si:H}}(\lambda)\cdot d} \tag{1}$$

where $\alpha_{\text{a-Si:H}}$ is the a-Si:H absorption coefficient and $\mathrm{EQE}_{\mathrm{PC1D}}$ is the EQE data as calculated by PC1D. The modeling suggests that with $S_{n,p}$ down to 10 cm/s and L_d up to 1 mm or wafer thickness down to 170 μm, it would be possible to reach the maximum IQE values of this kind of device. These values are not limiting factors for mass production as demonstrated by SunPower and Sanyo [4,5]. Lower $S_{n,p}$ and longer L_d can be reached by taking more care in substrate preparation, as demonstrated by the same group in other work [18].

To discriminate the photocurrent contributions of the different cell regions, we have modeled the generation by using the following expression:

$$G(\lambda) = \mathrm{e}^{-\alpha_{\text{a-Si:H}}(\lambda)\cdot d} \cdot \left[1 - \frac{\mathrm{e}^{-\alpha_{\text{c-Si}}(\lambda)\cdot t}}{1+\alpha_{\text{c-Si}}(\lambda)\cdot L_d} + \mathrm{e}^{-\alpha_{\text{c-Si}}(\lambda)\cdot(t-w)} \cdot \left(1 - \mathrm{e}^{-\alpha_{\text{c-Si}}(\lambda)\cdot w}\right)\right] \tag{2}$$

Table 2
Parameters used in PC1D simulation

c-Si parameters	
Thickness (μm)	250
Mobility μ_n, μ_p (cm^2/Vs)	1417, 470
Bandgap (eV)	1.124
Intrinsic concentration n_i (cm^{-3})	1×10^{10}
Absorption coefficient (model)	[16]
p-Type doping (cm^{-3})	3.2×10^{16}
Diffusion lenght L_d(μm)	500
Front surface recomb. S_n, S_p (cm/s)	80, 80
Rear surface recomb. S_n, S_p (cm/s)	1×10^6, 1×10^6
a-S:H parameters	
Thickness (μm)	0.015
Mobility μ_n, μ_p (cm^2/Vs)	1, 0.1
Bandgap (eV)	1.65
Intrinsic concentration n_i (cm^{-3})	1×10^7
Absorption coefficient (model)	[17]
$\mu\tau$ (cm^2/V)	1×10^{-12}
n-Type doping (cm^{-3})	5×10^{17}

where t is the wafer thickness, $\alpha_{\text{c-Si}}$ is the c-Si absorption coefficient, and w is the depletion depth. We have neglected the contribution of the intrinsic a-Si:H, since it is blinded from the c-Si bulk thickness. By modeling the data reported in Fig. 4, when a single p-type finger is illuminated, the generation can be evaluated only with the left term of (2), while when a single n-type finger is illuminated the contribution of the depletion depth, described in the right term of (2), becomes more evident than in the case of EQE measurements obtained by a monochromatic spotlight area larger than several finger contacts.

With the set of PC1D parameters adopted in EQE simulation, we have also fitted the IV characteristic under sunlight exposure, reported in Fig. 2 as a continuous line. A series resistance has been added to simulate the effect of low lateral conductivity of the n-type a-Si:H emitter that strongly reduces the cell fill factor. This problem mainly arises from the p-type c-Si/i a-Si:H/p-type a-Si:H contact in which the carrier transport is determined by tunneling mechanism, due to the relevant band offset between the two valence bands of p-type c-Si and p-type a-Si:H [18]. In our samples, these thicknesses could be thicker than expected, since the necessity to avoid shunts between the two amorphous doped layers has wrongly induced to deposit thicker buffer layers. The series resistance can be lowered reducing the thicknesses of both p-type and intrinsic a-Si:H layers and introducing a method to increase the conductivity of the p-type a-Si:H layer [19]. Moreover, a large number of fingers should be introduced per square centimeter and a treatment to increase the n-type layer conductivity, forming a thin CrSi layer on it, can be really useful also on the n-type amorphous emitter [14].

To exploit the V_{oc} value we have measured IV characteristic at room temperature and dark conditions. The dark current mainly flows between the fingers shaped back contacts in a region almost depleted as depicted in the inset of Fig. 4. To extract information about the recombination in the depletion region inside the crystalline side close to the heterojunction, it is possible to adopt the following detailed expression to describe the dark IV curve:

$$I(V) = I_0 \cdot \left(e^{\frac{V}{n_1 V_T}} - 1\right) + I_r e^{\frac{V}{n_2 V_T}} - I_g \cdot \left(\frac{1}{1 - (|V|/\text{BV})^{n_3}}\right) \tag{3}$$

where I_0 is the diode reverse saturation current; I_r, I_g are the recombination and thermal generation currents in the depletion region, respectively; BV is the breakdown voltage; n_1, n_2, n_3 are the ideality factors and V_T is the thermal equivalent voltage ($V_T = KT/q$ where K is the Boltzmann constant, T is the temperature and q is the electron charge). By fitting procedure, reported in Fig. 5 as a line, we have obtained the values reported in Table 3. In this model we have neglected the current flowing through the amorphous intrinsic insulator between the two rear contacts, due to both its poor conductivity (at least $10^{-11}\ \Omega^{-1}\,\text{cm}^{-1}$) and its thin thickness (10 nm). Moreover we have also neglected the depletion inside the n-type a-Si:H due to its defect density and dopant concentration [14]. At high current injection level the transport mechanism is dominated by the series resistance, as already seen in the lighted IV curve, not described by Eq. (3). From the latter analysis, we can conclude that the recombination mechanism limits the V_{oc}. However, the built-in potential, arising from the c-Si/a-Si:H heterojunction, still remains sufficiently high to determine a V_{oc} value of 687 mV.

Table 3
Parameters used to fit the IV dark data

Parameters	Values
I_0, reverse current (A/cm^2)	1.3×10^{-9}
I_r, recombination in the depletion region (A/cm^2)	4.5×10^{-7}
I_g, thermal generation in the depletion region (A/cm^2)	4.6×10^{-7}
n_1, ideality factor	1.65
n_2, ideality factor	8
n_3, ideality factor	3
BV, breakdown voltage (V)	1.6

5. Conclusion

In this paper, we have shown the BEHIND cell as an innovative design of the a-Si:H/c-Si heterostructure solar cell, where both the emitter and the back contact are formed by amorphous/crystalline silicon heterostructure. The grid-less textured front surface has been passivated by a double layer of amorphous silicon and silicon nitride (a-Si:H/SiN_x), which also provides anti-reflection against sunlight. We remark that the mask-assisted deposition of a-Si:H layer is feasible and only one metallic mask can be used in the entire fabrication process. We have analyzed the generation mechanism in different regions of the back contacts. With the aid of a PC1D model, we have deduced the properties of transport and recombination that affect the photocurrent and we have addressed the way for future improvements. Even if several technological aspects have to be optimized, such as the high value of series resistance, a V_{oc} of 687 mV has been reached that can be considered as a good starting point to continue to develop this low temperature process useful to reduce the PV manufacturing cost.

References

[1] W. Mulligan, R. Swanson, in: Proceedings of the 13th NREL Crystalline Silicon Workshop, Colorado, 2003, p. 30.
[2] D. Rose, O. Koehler, N. Kaminar, B. Mulligan, D. King, in: Proceedings of the 4th World Conference Photovoltaic Energy Conversion, 2006, p. 2018.
[3] W.P. Mulligan, D.H. Rose, M.J. Cudzinovic, D.M. De Ceuster, K.R. McIntosh, D.D. Smith, R.M. Swanson, in: Proceedings of the 19th European Photovoltaic Solar Energy Conference, 2004, p. 387.
[4] R.M. Swanson, in: Proceedings of the 31st IEEE PVSEC, Lake Buena Vista, 2005, p. 889.
[5] <http://www.sanyo.co.jp/clean/solar/hit_e/hit.html>.
[6] W.P. Mulligan, M.A. Carandang, M. Dawson, D.M. De Ceuster, C.N. Stone, R.M. Swanson, in: Proceedings of the 21st European Photovoltaic Solar Energy Conference, 2006, p. 1301.

[7] E. Van Kerschaver, G. Beaucarne, Prog. Photovolt.: Res. Appl. 14 (2006) 107.
[8] M. Taguchi, K. Kawamoto, S. Tsuge, T. Baba, H. Sakata, M. Morizane, K. Uchihashi, N. Nakamura, S. Kiyama, O. Oota, Prog. Photovolt.: Res. Appl. 8 (2000) 503.
[9] E. Maruyama, A. Terakawa, M. Taguchi, Y. Yoshimine, D. Ide, T. Baba, M. Shima, H. Sakata, M. Tanaka, in: Proceedings of the 4th World Conference Photovoltaic Energy Conversion, 2006, p. 1455.
[10] M. Taguchi, A. Terakawa, E. Maruyama, M. Tanaka, Prog. Photovolt.: Res. Appl. 3 (2005) 481.
[11] M. Tucci, L. Serenelli, S. De Iuliis, M. Izzi, Thin Solid Film 515 (2007) 7625.
[12] M. Tucci, L. Serenelli, S. De Iuliis, E. Salza, L. Pirozzi, in: Proceedings of the 21st European Photovoltaic Solar Energy Conference, 2006, p. 1250.
[13] L. Kreinin, N. Bordin, J. Broder, N. Eisenberg, M. Tucci, E. Talgorn, S. De Iuliis, L. Serenelli, M. Izzi, E. Salza, L. Pirozzi, in: Proceedings of the 21st European Photovoltaic Solar Energy Conference, 2006, p. 855.
[14] M. Tucci, G. de Cesare, J. Non-Cryst. Solids 338 (2004) 663.
[15] P.A. Basore, D.A. Clugston, PC1D version 5.3, University of New South Wales, 1998.
[16] M.A. Green, M.J. Keevers, Prog. Photovolt.: Res. Appl. 3 (1995) 189.
[17] E.D. Palik, in: Handbook of Optical Constants of Solids, Academic Press, New York, 1985.
[18] M. Tucci, L. Serenelli, S. De Iuliis, D. Caputo, A. Nascetti, G. de Cesare, in: Proceedings of the 21st European Photovoltaic Solar Energy Conference, 2006, p. 902.
[19] D. Caputo, G. de Cesare, A. Nascetti, M. Tucci, J. Non-Cryst. Solids 352 (2006) 1818.