INTERDIGITATED BACK CONTACT AMORPHOUS/CRYSTALLINE SILICON HETEROJUNCTION SOLAR CELLS

Simona De Iuliis[1], L. J. Geerligs[1], M. Tucci[3], L. Serenelli[3], G. de Cesare[2], M. Ceccarelli[2],
[1] ECN Solar Energy, P.O. Box 1, 1755 ZG Petten, The Netherlands.
[2] University "Sapienza", Department of Electronic Engineering, via Eudossiana 18, 00184 Roma, Italy
[3] ENEA Research Center Casaccia, via Anguillarese 301, 00123 Roma, Italy

ABSTRACT

This paper shows how the amorphous/crystalline silicon technology can be implemented in the interdigitated back contact solar cell design. The entire self-aligned mask and photolithography-free process is performed at temperature below 300 °C with the aid of one metallic mask to create the interdigitated pattern. An open-circuit voltage of 687 mV has been measured on a *p*-type mono-crystalline silicon wafer. We show that the uniformity of the deposited amorphous silicon layers is not influenced by the mask-assisted deposition process and that the alignment is feasible. Moreover, this paper investigates the photocurrent limiting factors by one-dimensional modelling and quantum efficiency measurements.

1. INTRODUCTION

Top performing production cells include SunPower's A-300 cell and Sanyo's HIT cell [1,2]. We present an innovative solar cell design demonstrating that the heterostructure technology can have a chance in the challenge of the IBC solar cells. We named our device: BEHIND cell (Back Enhanced Heterostructure with INterDigitated contacts cell).

2. EXPERIMENTAL

We have fabricated rear junction, backside contact cells in which both the emitter and the back contact are formed by hydrogenated amorphous/crystalline silicon (a-Si:H/c-Si) heterostructure, using a three chamber 13.56 MHz direct Plasma Enhanced Chemical Vapour Deposition (PECVD) system. Our device is formed starting from 1 Ωcm *p*-type, random pyramids textured, mono-crystalline silicon wafer. After a standard cleaning, on the complete back side we have deposit a double layer of a-Si:H, the intrinsic buffer layer followed by the *n*-type doped one. By the aid of a metallic mask, we have selectively dry etched the *n*-layer and subsequently we have deposit a *p*-type a-Si:H layer and evaporated the aluminum (Al) grid. Then we have rotated the mask of 180 degrees to evaporate the silver (Ag) grid on the *n*-layer, thus forming a comb pattern interdigitated with the previous one. The grid-less front surface is passivated by a double layer of amorphous silicon and silicon nitride (a-Si:H/SiN_x), which also acts as anti-reflective coating. The entire self-aligned mask and photolithography-free process is performed at temperature below 300 °C with the aid of just one metallic mask to create the interdigitated pattern. The process scheme and the process conditions are elsewhere explained [3].

3. RESULTS AND DISCUSSION

The experimental IV data have been measured at room temperature, calibrated to 100 mW/cm^2 and AM1.5g illumination and are shown in the Fig. 1 as symbols.

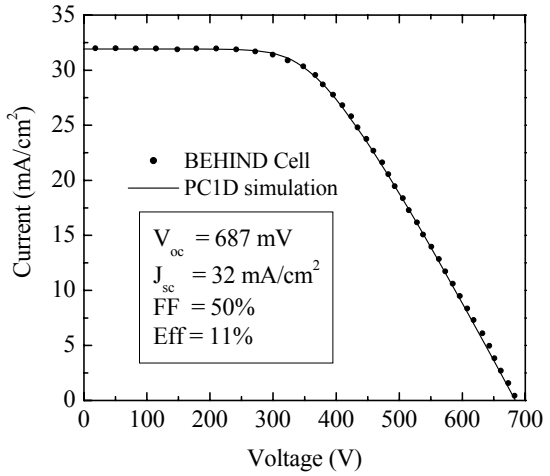

Fig. 1 IV light measurements and photovoltaic parameters: experimental data (symbols) and PC1D simulations (lines).

The 687 mV as open circuit voltage (V_{oc}) value confirms that the uniformity of the deposited amorphous silicon layers is not influenced by the mask-assisted deposition process, the alignment is feasible and the regions where the doped layers can overlap are well isolated by the intrinsic a-Si:H. We remark that at the end of fabrication process the cell photocurrent was completely dominated by a very high series resistance. To overcome this problem we have performed a laser treatment over the Al comb [4], thus producing a less resistive contact, even if in a narrow region. Although the absence of front metal shading should reflect in higher short circuit current (J_{sc}) this does not exceed 32 mA/cm^2, as confirmed by integrating the EQE data over the sun spectrum. The IQE, EQE and reflectance data are reported in Fig. 2 as symbols. The J_{sc} value is less than the expected one due to both optical and recombination losses. The key issues to obtain high J_{sc} depends on diffusion length, L_d, and surface recombination velocity, $S_{n,p}$. To explore the effect of both parameters we have compared the EQE experimental data with a PC1D [5] simulation, in which we have simplified our BEHIND cell into one dimensional crystalline based solar cell having a back thin *n*-type a-Si:H emitter layer. We have obtained a good agreement between experimental data and simulation by choosing appropriate L_d and $S_{n,p}$ values, taking into account the measured reflectance profile, and considering the passivation/antireflection coating absorption in the blue region. The modelling suggest that with $S_{n,p}$ down to 10 cm/s

and L_d up to 1 mm it would be possible to reach the maximum IQE values of this kind of device.

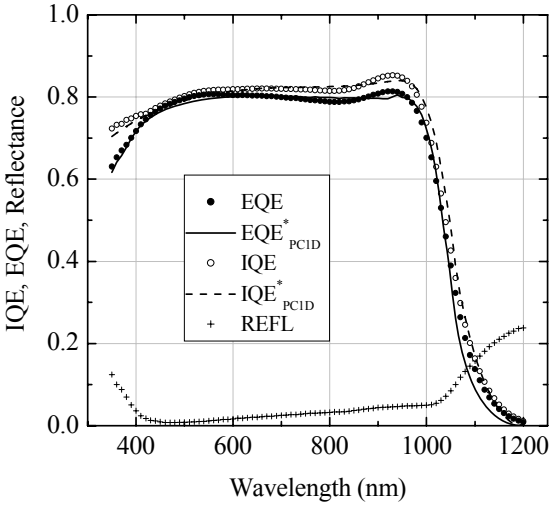

Fig. 2 IQE, EQE, Reflectance of the BEHIND cell: experimental data (symbols) and PC1D simulations (lines).

With the set of PC1D parameters adopted in QE simulation we have also fitted the IV characteristic under sunlight exposure, reported in Fig. 1 as continuous line. A series resistance has been added to simulate the effect of low lateral conductivity of the *n*-type a-Si:H emitter that strongly reduces the cell fill factor. This problem mainly arises from the *p*-type c-Si / *i* a-Si:H / *p*-type a-Si:H contact in which the carrier transport is determined by tunneling mechanism, due to the relevant band offset between the two valence band of *p*-type c-Si and *p*-type a-Si:H [6]. In our samples, these layers could be thicker than expected, since the need to avoid shunts between the two amorphous doped layers has wrongly induced to deposit thicker buffer layer. The series resistance can be lowered by reducing the thickness of both *p*-type and intrinsic a-Si:H layers and increasing the conductivity of the *p*-type a-Si:H layer [7]. Moreover a large number of fingers should be introduced per square centimetre and a treatment to increase the *n*-type layer conductivity, forming a thin CrSi layer on it, can be really useful also on the *n*-type amorphous emitter [8].

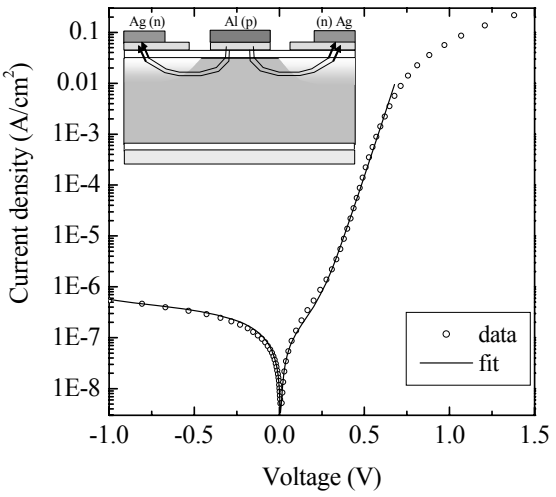

Fig. 3 IV characteristic at room temperature and dark conditions. In the inset how to the dark current flows between rear contacts.

To exploit the V_{oc} value we have measured IV characteristic at room temperature and dark conditions. The dark current mainly flows between the fingers shaped back contacts in a region almost depleted as depicted in the inset of Fig. 4. To extract information about the recombination in the depletion region inside the crystalline side close to the heterojunction we have analytically modelled the dark IV curve. By fitting procedure, reported in Fig. 4 as line, we have obtained the values of 1.3×10^{-9} A/cm^2 and 4.5×10^{-7} A/cm^2 for the diode reverse saturation current and the recombination current in the depletion region respectively. We can conclude that the recombination mechanism limits the V_{oc}. However the built-in potential, arising from the c-Si/a-Si:H heterojunction, still remains sufficiently high to determine a V_{oc} value of 687 mV.

4. CONCLUSION

In this paper we have shown the BEHIND cell as an innovative design of the interdigitated back contact a-Si:H/c-Si heterojunction solar cell. The mask-assisted deposition of a-Si:H layer is feasible and the entire self-aligned mask and photolithography-free process is performed at temperature below 300 °C with the aid of one metallic mask to create the interdigitated pattern. Even if several technological aspects have to be optimized a V_{oc} of 687 mV has been reached that can be considered a good starting point to continue to develop this low temperature process useful to reduce the PV manufacturing cost.

5. AKCNOLEDGMENTS

This work was supported by SenterNovem in the QCPassi Project.

REFERENCES

[1] *http://www.sunpowercorp.com/*
[2] *http://www.sanyo.co.jp/clean/solar/hit_e/hit.html*
[3] *M. Tucci, L. Serenelli, E. Salza, S. De Iuliis, L. J. Geerligs , D. Caputo, M. Ceccarelli, G. de Cesare; J. of Non-Cryst. Solids, to be published.*
[4] *L. Kreinin, N. Bordin, J. Broder, N. Eisenberg, M. Tucci, E. Talgorn, S. De Iuliis, L. Serenelli, M. Izzi, E. Salza, L. Pirozzi; Proc. of 21st European Photovoltaic Solar Energy Conference (2006) 855.*
[5] *PC1D version 5.3 P.A. Basore, D.A. Clugston University of New South Wales (1998).*
[6] *M. Tucci, L Serenelli, S De Iuliis, D Caputo, A Nascetti, G de Cesare; Proc. of 21st European Photovoltaic Solar Energy Conference (2006) 902.*
[7] *D. Caputo, G. de Cesare, A. Nascetti, M. Tucci; J. of Non-Cryst. Solids 352 (2006) 1818.*
[8] *M. Tucci, G. de Cesare; J. of Non-Cryst. Solids 338 (2004) 663.*