ECN-E--10-056

Quantum Cutting and Passivation for Back-contacted Heterojunction solar cells ("QCPassi")

SenterNovem project EOSLT03011

Jan 1, 2006 - Dec 31, 2009

Final Report

L.J. Geerligs[1], R.E.I. Schropp[2], A. Meijerink[3], A.W. Weeber[1]

[1]ECN Solar Energy (penvoerder)

[2]Utrecht University, SID-Physics of Devices

[3]Utrecht University, Debye Institute, Condensed Matter and Interfaces

July 2010

Preface

Crystalline silicon solar cell technology currently can produce commercial modules at prices well below 2€/Wp. This is based on a cell design that has been developed and refined over the past approximately 30 years. As the industry grows, economy of scale and optimization of production processes will result in significant further price reductions for modules based on this standard technology.
In addition, the silicon pv industry has recently entered into a phase of strong interest in development of alternative, higher efficiency cell designs, still based on silicon wafers. The rationale is that cell processing cost (also called 'cell conversion cost': converting wafer to solar cell) is only a small part of the cost/Wp. Much of the cost/Wp is proportional to area (e.g. cost of the wafer, module construction, and part of the system installation). Therefore, increased efficiency will reduce the cost/Wp, if the cell conversion cost is not increased too much. High efficiency is particularly important where area is scarce (as on Japanese roofs) or system installation is expensive (in western countries). Higher efficiency also makes silicon solar cells perform better at high temperature, and usually also in indirect light, increasing the annual yield (the kWh/Wp per year).
Higher efficiency, at affordable cell processing cost, is probably necessary for a module price significantly below 1€/Wp.

The standard cell technology at this moment results in efficiencies around 16% for multicrystalline wafers, and around 17 to 17.5% for monocrystalline wafers. The practical efficiency limit for silicon wafers is expected to be about 26% (based on the theoretical limit of 29%, and including realistic best achievable optical and bulk recombination losses, and very small surface recombination losses). Thus there is still much potential gain to be made by increasing cell efficiency.

There are two keys to achieving a solar cell efficiency close to the limit: passivating the wafer surfaces, and avoiding optical losses on the front side, in particular avoiding a metal grid on the front side. The objective of QCPassi project was the development of a new crystalline silicon solar cell concept, exactly aimed at these two key points. This is the concept of a back contact silicon heterojunction solar cell. A silicon heterojunction (SHJ) solar cell offers the best practical technology for excellent surface passivation. A back contact solar cell is the method to avoid a metal grid on the front side. The combination of the two, the back contact silicon heterojunction solar cell, appears to be a public domain idea. Ebara Corporation of Japan filed a PCT application on the idea in 2002, but as far as known did not pursue it to national patents.

Through collaboration of the QCPassi project with ENEA (Italian Agency for New Technologies, Energy, and the Sustainable Economic Development) and University of Rome, Italy, indeed the back contact SHJ solar cell was demonstrated. Recently, a large activity has developed over the world, and especially in Europe, at institutes, universities, and companies, working on the same or similar concepts.
It seems that the back contact SHJ solar cell is now internationally regarded as one of the most promising highest efficiency cell designs for the mid-term future.
The traditional silicon heterojunction solar cell (with front metallization grid, not fully back-contacted), until now exclusive for Sanyo, also has become subject of intense R&D, with companies such as Roth&Rau, Jusung, and Kaneka, aiming at production within the next few years. This traditional SHJ solar cell allows efficiencies in excess of 20%, with simpler technology than the back-contact cell.

Exceeding the traditional efficiency limit of silicon solar cells (the 26% described above) is also not out of the question. To this end, QCPassi has investigated down conversion, also known as quantum cutting, of photons. This process entails creating two IR photons from one UV photon. Thus more electrons can be generated per incident solar (UV) photon, and the cell efficiency

can potentially be increased. Also this concept was demonstrated in the project, although not yet integrated in a solar cell.

We acknowledge the useful and friendly collaboration with the partners of a French national project on silicon heterojunction cells, also named QCPassi. The technical and scientific staff of Utrecht University and ECN is acknowledged for assistance with experiments, processing and for discussions.

This report can be downloaded from the website of ECN. On request, printouts of the report can be obtained from ECN Solar Energy.

For more information, please contact the secretary of ECN Solar Energy: tel. 0224-56 4761; or via http://www.ecn.nl/nl/units/zon/contact/

Het project is uitgevoerd met subsidie van het Ministerie van Economische Zaken, regeling EOS: Lange Termijn uitgevoerd door het Agentschap NL. Projectnummer EOSLT03011.

Abstract

The objective of the QCPassi project was the development of a new crystalline silicon solar cell concept, designed for highly integrated module manufacturing, very high efficiencies (>20%) and strongly reduced cost (< 1 €/Wp on the module level). The concept is that of a back-contacted solar cell with hetero-junctions at the rear made on three times thinner silicon substrates. The concept includes photon conversion.

The back contact silicon heterojunction solar cell was demonstrated in the QCPassi project through collaboration with ENEA (Italian Agency for New Technologies, Energy, and the Sustainable Economic Development) and University of Rome, Italy, initially on untextured wafers with a best efficiency of 11%. By introducing wafer texture and improved mask design, an efficiency of 15% was reached. The high voltage of 695mV demonstrates the very high efficiency potential of the concept. The efficiency is so far limited by absorption in front coating, and by fill factor, which are both subjects for future optimization.

For antireflection coating of back contact silicon heterojunction cells, dielectric coatings which can be deposited at low temperature offer particular advantage. Low temperature deposition of silicon nitride coatings by hot wire (HW) CVD was demonstrated (at 230 °C), resulting in films with minimal light absorption. Also high rate deposition by HW CVD was demonstrated.

The development of heterojunction deposition technology at Utrecht and ECN resulted in promising traditional (front-grid) devices with >13% efficiency, and clear routes for improvement. Hybrid cells combining heterojunction emitter with diffused back surface field yielded an efficiency of 16.4% and a VOC of 623 mV on isotextured n-type FZ c-Si wafers with diffused BSF. Major points for improvement are the introduction of texture, optimization of the thickness of a-Si emitter to reduce optical loss, and improvement of the ITO, also to reduce optical loss. The use of a unique remote rf pecvd tool resulted in good heterojunctions without intrinsic buffer layer, potentially reducing cost and improving performance of heterojunction solar cells.
The feasibility of depositing patterned doped layers through a shadow mask for the formation of interdigitated back contacts (IBC) has been investigated and compared for Hot Wire CVD and Plasma Enhanced CVD. This has led valuable insight in the differences of the two CVD techniques and to optimized design of a mask system for IBC solar cell production.
First back contact heterojunction solar cells were also made at ECN. However, due to insufficient surface passivation and high series resistance, the efficiencies are very low. This can be solved by optimization of the pecvd process.

At this status of the back contact technology, it was not deemed useful to test mc-Si back contact cells. However, front-grid SHJ cells were made on mc-Si wafers, within the consortium as well as through collaboration with ENEA and University of Rome, Italy. The results of up to 15% efficiency are the best published value in literature for this concept.

For downconversion, focus was on Lanthanide ions. The energy-level structure of Yb^{3+} is ideally suited for use in the downconversion of c-Si solar cells. The Yb^{3+} ion has a single excited state approximately 10^4 cm^{-1} above the ground state, corresponding to an emission around 980 nm. The absence of other energy levels allows Yb^{3+} to exclusively 'pick up' energy packages of 10^4 cm^{-1} from other lanthanide ions and emit photons at 980 nm, which can be absorbed in the Silicon solar cell. Pr^{3+} was chosen as donor ion, to pick up the UV photon energy and transfer it in two packages to Yb^{3+} ions. SrF2 was used as the host lattice. A highest conversion efficiency of 140% was obtained, using excitation at 441nm at room temperature.

Efforts to demonstrate current gain at cell level were not successful. One reason may be that the absorption band is quite narrow, and without a sensitizer the amount of photons exciting Pr^{3+} is relatively small.
Er^{3+} and Nd^{3+} were tested as alternative donor ions, however, with limited succes. A relevant limitation for these donor ions will be their sensitivity for wavelengths of 380nm or lower, which are less abundant in the terrestrial solar radiation.

Contents

1. Introduction

This report starts with a selection of publications produced by the project, which give a good overview of the work performed in, and the results of, the project.

Chapters 2-4 deal with the development of the IBC-SHJ cell, in a collaboration with ENEA (Italian Agency for New Technologies, Energy, and the Sustainable Economic Development) and University of Rome, Italy. Chapters 5-6 deal with the development of SHJ cells on mc-Si, within QCPassi, and in the same collaboration with Italian partners. Chapters 7-8 deal with the development of silicon heterojunction layers. Chapters 9-10 deal with deposition of antireflection coating by low-temperature and high rate CVD of SiNx, respectively. Chapter 11 contains a review of photon conversion (up- as well as down-conversion). Chapters 12-14 deal with the investigation of three quantum cutting couples based on Yb^{3+}, with Pr^{3+}, Er^{3+} and Nd^{3+} as donor ions.
Papers which are copyrighted by the publisher are included as abstract.

The final chapter (chapter 15) gives an outlook for the field.

Apart from the collaboration with University of Rome and ENEA, the QCPassi project also collaborated with a French sister project QCPassi, in which the French national energy organization (CEA-INES), several groups of the French national science foundation CNRS, and the company Photowatt participated. Regular meetings were held to update each other on progress, and discuss, for example, new insights in the technology, progress in modelling tools, developments in the state of the art, or developments in IP.

Het project is uitgevoerd met subsidie van het Ministerie van Economische Zaken, regeling EOS: Lange Termijn uitgevoerd door het Agentschap NL.

2. Interdigitated back contact amorphous/crystalline silicon heterojunction solar cells

Simona De Iuliis, L. J. Geerligs, M. Tucci, L. Serenelli, G. de Cesare, M. Ceccarelli. Technical Digest of the International PVSEC-17, Fukuoka, Japan, 2007, p.397.

INTERDIGITATED BACK CONTACT AMORPHOUS/CRYSTALLINE SILICON HETEROJUNCTION SOLAR CELLS

Simona De Iuliis[1], L. J. Geerligs[1], M. Tucci[3], L. Serenelli[3], G. de Cesare[2], M. Ceccarelli[2],
[1] ECN Solar Energy, P.O. Box 1, 1755 ZG Petten, The Netherlands.
[2] University "Sapienza", Department of Electronic Engineering, via Eudossiana 18, 00184 Roma, Italy
[3] ENEA Research Center Casaccia, via Anguillarese 301, 00123 Roma, Italy

ABSTRACT

This paper shows how the amorphous/crystalline silicon technology can be implemented in the interdigitated back contact solar cell design. The entire self-aligned mask and photolithography-free process is performed at temperature below 300 °C with the aid of one metallic mask to create the interdigitated pattern. An open-circuit voltage of 687 mV has been measured on a *p*-type mono-crystalline silicon wafer. We show that the uniformity of the deposited amorphous silicon layers is not influenced by the mask-assisted deposition process and that the alignment is feasible. Moreover, this paper investigates the photocurrent limiting factors by one-dimensional modelling and quantum efficiency measurements.

1. INTRODUCTION

Top performing production cells include SunPower's A-300 cell and Sanyo's HIT cell [1,2]. We present an innovative solar cell design demonstrating that the heterostructure technology can have a chance in the challenge of the IBC solar cells. We named our device: BEHIND cell (Back Enhanced Heterostructure with INterDigitated contacts cell).

2. EXPERIMENTAL

We have fabricated rear junction, backside contact cells in which both the emitter and the back contact are formed by hydrogenated amorphous/crystalline silicon (a-Si:H/c-Si) heterostructure, using a three chamber 13.56 MHz direct Plasma Enhanced Chemical Vapour Deposition (PECVD) system. Our device is formed starting from 1 Ωcm *p*-type, random pyramids textured, mono-crystalline silicon wafer. After a standard cleaning, on the complete back side we have deposit a double layer of a-Si:H, the intrinsic buffer layer followed by the *n*-type doped one. By the aid of a metallic mask, we have selectively dry etched the *n*-layer and subsequently we have deposit a *p*-type a-Si:H layer and evaporated the aluminum (Al) grid. Then we have rotated the mask of 180 degrees to evaporate the silver (Ag) grid on the *n*-layer, thus forming a comb pattern interdigitated with the previous one. The grid-less front surface is passivated by a double layer of amorphous silicon and silicon nitride (a-Si:H/SiN_x), which also acts as anti-reflective coating. The entire self-aligned mask and photolithography-free process is performed at temperature below 300 °C with the aid of just one metallic mask to create the interdigitated pattern. The process scheme and the process conditions are elsewhere explained [3].

3. RESULTS AND DISCUSSION

The experimental IV data have been measured at room temperature, calibrated to 100 mW/cm^2 and AM1.5g illumination and are shown in the Fig. 1 as symbols.

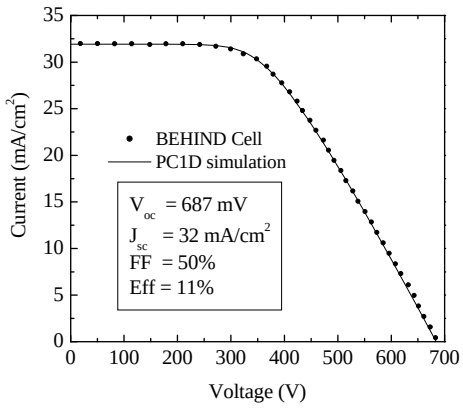

Fig. 1 IV light measurements and photovoltaic parameters: experimental data (symbols) and PC1D simulations (lines).

The 687 mV as open circuit voltage (V_{oc}) value confirms that the uniformity of the deposited amorphous silicon layers is not influenced by the mask-assisted deposition process, the alignment is feasible and the regions where the doped layers can overlap are well isolated by the intrinsic a-Si:H. We remark that at the end of fabrication process the cell photocurrent was completely dominated by a very high series resistance. To overcome this problem we have performed a laser treatment over the Al comb [4], thus producing a less resistive contact, even if in a narrow region. Although the absence of front metal shading should reflect in higher short circuit current (J_{sc}) this does not exceed 32 mA/cm^2, as confirmed by integrating the EQE data over the sun spectrum. The IQE, EQE and reflectance data are reported in Fig. 2 as symbols. The J_{sc} value is less than the expected one due to both optical and recombination losses. The key issues to obtain high J_{sc} depends on diffusion length, L_d, and surface recombination velocity, $S_{n,p}$. To explore the effect of both parameters we have compared the EQE experimental data with a PC1D [5] simulation, in which we have simplified our BEHIND cell into one dimensional crystalline based solar cell having a back thin *n*-type a-Si:H emitter layer. We have obtained a good agreement between experimental data and simulation by choosing appropriate L_d and $S_{n,p}$ values, taking into account the measured reflectance profile, and considering the passivation/antireflection coating absorption in the blue region. The modelling suggest that with $S_{n,p}$ down to 10 cm/s

and L_d up to 1 mm it would be possible to reach the maximum IQE values of this kind of device.

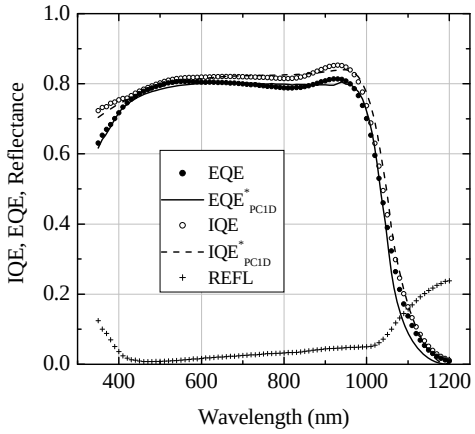

Fig. 2 IQE, EQE, Reflectance of the BEHIND cell: experimental data (symbols) and PC1D simulations (lines).

With the set of PC1D parameters adopted in QE simulation we have also fitted the IV characteristic under sunlight exposure, reported in Fig. 1 as continuous line. A series resistance has been added to simulate the effect of low lateral conductivity of the *n*-type a-Si:H emitter that strongly reduces the cell fill factor. This problem mainly arises from the *p*-type c-Si / *i* a-Si:H / *p*-type a-Si:H contact in which the carrier transport is determined by tunneling mechanism, due to the relevant band offset between the two valence band of *p*-type c-Si and *p*-type a-Si:H [6]. In our samples, these layers could be thicker than expected, since the need to avoid shunts between the two amorphous doped layers has wrongly induced to deposit thicker buffer layer. The series resistance can be lowered by reducing the thickness of both *p*-type and intrinsic a-Si:H layers and increasing the conductivity of the *p*-type a-Si:H layer [7]. Moreover a large number of fingers should be introduced per square centimetre and a treatment to increase the *n*-type layer conductivity, forming a thin CrSi layer on it, can be really useful also on the *n*-type amorphous emitter [8].

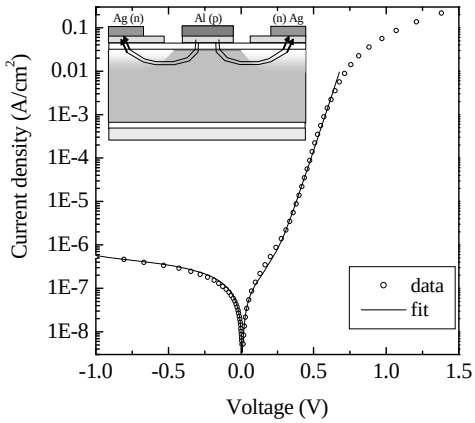

Fig. 3 IV characteristic at room temperature and dark conditions. In the inset how to the dark current flows between rear contacts.

To exploit the V_{oc} value we have measured IV characteristic at room temperature and dark conditions. The dark current mainly flows between the fingers shaped back contacts in a region almost depleted as depicted in the inset of Fig. 4. To extract information about the recombination in the depletion region inside the crystalline side close to the heterojunction we have analytically modelled the dark IV curve. By fitting procedure, reported in Fig. 4 as line, we have obtained the values of 1.3×10^{-9} A/cm^2 and 4.5×10^{-7} A/cm^2 for the diode reverse saturation current and the recombination current in the depletion region respectively. We can conclude that the recombination mechanism limits the V_{oc}. However the built-in potential, arising from the c-Si/a-Si:H heterojunction, still remains sufficiently high to determine a V_{oc} value of 687 mV.

4. CONCLUSION

In this paper we have shown the BEHIND cell as an innovative design of the interdigitated back contact a-Si:H/c-Si heterojunction solar cell. The mask-assisted deposition of a-Si:H layer is feasible and the entire self-aligned mask and photolithography-free process is performed at temperature below 300 °C with the aid of one metallic mask to create the interdigitated pattern. Even if several technological aspects have to be optimized a V_{oc} of 687 mV has been reached that can be considered a good starting point to continue to develop this low temperature process useful to reduce the PV manufacturing cost.

5. AKCNOLEDGMENTS

This work was supported by SenterNovem in the QCPassi Project.

REFERENCES

[1] *http://www.sunpowercorp.com/*
[2] *http://www.sanyo.co.jp/clean/solar/hit_e/hit.html*
[3] *M. Tucci, L. Serenelli, E. Salza, S. De Iuliis, L. J. Geerligs , D. Caputo, M. Ceccarelli, G. de Cesare; J. of Non-Cryst. Solids, to be published.*
[4] *L. Kreinin, N. Bordin, J. Broder, N. Eisenberg, M. Tucci, E. Talgorn, S. De Iuliis, L. Serenelli, M. Izzi, E. Salza, L. Pirozzi; Proc. of 21st European Photovoltaic Solar Energy Conference (2006) 855.*
[5] *PC1D version 5.3 P.A. Basore, D.A. Clugston University of New South Wales (1998).*
[6] *M. Tucci, L Serenelli, S De Iuliis, D Caputo, A Nascetti, G de Cesare; Proc. of 21st European Photovoltaic Solar Energy Conference (2006) 902.*
[7] *D. Caputo, G. de Cesare, A. Nascetti, M. Tucci; J. of Non-Cryst. Solids 352 (2006) 1818.*
[8] *M. Tucci, G. de Cesare; J. of Non-Cryst. Solids 338 (2004) 663.*

3. Back contacted a-Si:H/c-Si heterostructure solar cells

M. Tucci, L. Serenelli, E. Salza, S. De Iuliis, L.J. Geerligs, D. Caputo, M. Ceccarelli, G. de Cesare, Journal of Non-crystalline solids 354, 2386 (2008).

Available online at www.sciencedirect.com

ScienceDirect

Journal of Non-Crystalline Solids 354 (2008) 2386–2391

JOURNAL OF NON-CRYSTALLINE SOLIDS

www.elsevier.com/locate/jnoncrysol

Back contacted a-Si:H/c-Si heterostructure solar cells

M. Tucci [a,*], L. Serenelli [b], E. Salza [a], S. De Iuliis [b], L.J. Geerligs [b], D. Caputo [c], M. Ceccarelli [c], G. de Cesare [c]

[a] *ENEA Research Center Casaccia, Via Anguillarese 301, 00123 Roma, Italy*
[b] *ECN Solar Energy, P.O. Box 1 NL-1755 ZG Petten, The Netherlands*
[c] *Department of Electronic Engineering University ' Sapienza', via Eudossiana, 18, 00184 Roma, Italy*

Available online 5 February 2008

Abstract

This paper shows how the amorphous/crystalline silicon technology can be implemented in the interdigitated back contact solar cell design. We have fabricated rear-junction, backside contact cells in which both the emitter and the back contact are formed by amorphous/crystalline silicon heterostructure, and the grid-less textured front surface is passivated by a double layer of amorphous silicon and silicon nitride, which also provides an anti-reflection coating. The entire self-aligned mask and photolithography-free process is performed at temperature below 300 °C with the aid of one metallic mask to create the interdigitated pattern. An open circuit voltage of 687 mV has been measured on a 0.5 Ωcm p-type monocrystalline silicon wafer. On the other hand, several technological aspects that limit the fill factor (50%) and the short circuit current density (32 mA/cm^2) still need improvement. We show that the uniformity of the deposited amorphous silicon layers is not influenced by the mask-assisted deposition process and that the alignment is feasible. Moreover, this paper investigates the photocurrent limiting factors by one-dimensional modeling and quantum efficiency measurements.

PACS: 79.60.Jv; 73.61.Jc

Keywords: Solar cells; Heterojunctions; Photovoltaics

4. Back Enhanced Heterostructure with INterDigitated contact – BEHIND – solar cell

Mario Tucci, Luca Serenelli, Enrico Salza, Luisa Pirozzi, Giampiero de Cesare, Domenico Caputo, Matteo Ceccarelli, Pierino Martufi, Simona De Iuliis, Lambert J. Geerligs. International Conference on Electronic Materials (IUMRS-ICEM), Sydney, Australia, July 28 - Aug 1, 2008.

Back Enhanced Heterostructure with INterDigitated contact – BEHIND - solar cell

Mario Tucci[1], Luca Serenelli[1], Enrico Salza[1], Luisa Pirozzi[1]
Giampiero de Cesare[2], Domenico Caputo[2], Matteo Ceccarelli[2], Pierino Martufi[2]
Simona De Iuliis[3], Lambert J. Geerligs[3]
[1] ENEA Research Center Casaccia, Via Anguillarese 301, 00123 Roma, Italy
e-mail: mario.tucci@casaccia.enea.it tel.: +39 06 30484095
[2] Electronic Engineering University of Rome "Sapienza", via Eudossiana 18, 00184 Roma, Italy
[3] ECN Solar Energy, P.O. Box 1, NL-1755 ZG Petten, The Netherlands

***Abstract*—In this paper we investigate in detail how the heterostructure concept can be implemented in an interdigitated back contact solar cell, in which both the emitters are formed on the back side of the c-Si wafer by amorphous/crystalline silicon heterostructure, and at the same time the grid-less front surface is passivated by a double layer of amorphous silicon and silicon nitride, which also provides an anti-reflection coating. The entire process, held at temperature below 300 °C, is photolithography-free, using a metallic self-aligned mask to create the interdigitated pattern. An open-circuit voltage of 695 mV has been measured on this device fabricated. The mask-assisted deposition process does not influence the uniformity of the deposited amorphous silicon layers. Several technological aspects that limit the fill factor are considered and discussed.**

Keywords-component; heterostructure, IBC, amorphous silicon.

I. INTRODUCTION

The tendency towards shrinking wafer thickness to reduce the photovoltaic cost, is driving solar cell fabrication to reduce the process temperature. This in particularly for multi-crystalline silicon where wafer bowing and thermal stresses in the bulk material can be problematic. On the other hand, an effective back surface field, usually provided by high temperature processes, is an increasing necessity with decreasing substrate thickness. Both of these issues can be faced with amorphous/crystalline (a-Si/c-Si) silicon heterostructure, which can be deposited by Plasma Enhanced Chemical Vapour Deposition (PECVD) at temperature below 400 °C. A way to increase PV conversion efficiency is represented by rear-junction, back-contact solar cell design interdigitated (IBC) able to collect photogenerated carriers entirely from the rear of the cell. The advantages of this structure include no contact grid shading on the sunward side and use of a thin substrate, [1, 2]. Another useful concept for increasing c-Si based solar cells is the one adopted by Sanyo's HIT structure in which high-quality intrinsic a-Si:H layers allow an excellent surface passivation of c-Si surface, resulting in high efficiency, especially a high open circuit voltage (V_{oc}): almost 730 mV has been reached [3]. This technology has been demonstrated effective both on n-type or p-type crystalline silicon [4, 5]. Moreover the temperature coefficient of a-Si:H / c-Si heterostructure cells is better than conventional c-Si solar cells and results in a higher output power at high temperatures [6]. Finally the implementation of a-Si:H / c-Si heterojunction as solar cell concept has the capability of reaching efficiencies up to 25% [7]. Even if such technology can increase the open-circuit voltage, the a-Si window layer can still affect the short-circuit current due to the amorphous silicon absorption in the blue region of the solar spectrum. To overcome this and to remove any shadowing effect from a top metal grid, we have developed a new cell design transferring the emitter and both contacts to the rear side of the device: the BEHIND (Back Enhanced Heterostructure with InterDigitated contact) solar cell. Our approach to BEHIND cell fabrication is based on the idea to develop an innovative IBC technology entirely performed at very low temperature (< 300 °C), thus resulting in an advantage for thinner wafers; involving a self-aligned mask assisted and photolithography-free process and that could benefit of the passivation quality of the a-Si:H. If the rear-junction and backside contact design enjoys reduced optical shading losses, also requires high bulk lifetime and low front-surface recombination. In particular this work has been devoted to overcome several problems that strongly affected the previously reported structure [8], such as p-type c-Si p-type a-Si base contact, shunt effect and series resistance, in order to achieve a reliable solar cell process.

II. DEVICE FABRICATION

Actual BEHIND solar cell has been fabricated starting from a 4 inch diameter, 200 μm thick, <100> oriented, 1 Ωcm p-type, one side polished CZ mono-crystalline silicon wafer. After front side alkaline texturing and industrial cleaning, the front side antireflection passivation coating and the rear side emitter and back contact have been deposited in a 13.56 MHz direct Plasma Enhanced Chemical Vapour Deposition (PECVD) system. In particular a double layer stack of a-Si/SiN_x on the sunward side, acting as passivation and anti-reflection layer [9] has been deposited using the conditions reported in table I. Then on the whole polished backside of the wafer, after an HF-dipping procedure to remove the native oxide, an intrinsic a-Si:H buffer layer has been deposited followed by a n-type doped a-Si:H one. Over this film a chromium silicide (CrSi) layer has been formed to increase the

Table I. PECVD deposition parameters used in the thin film formation (temperature indicated are effective).

Layer		Gas	Flow (sccm)	Pressure (mTorr)	Temperature (°C)	RF Power (mW/cm^2)	Thickness (nm)
Front side	a-Si:H	SiH_4/Ar 5%	120	750	250	36	10
	SiNx	SiH_4/Ar 5%,NH_3	120, 10	750	250	36	65
Rear side	a-Si:H	SiH_4/Ar 5%	120	750	250	36	5
	n-a-Si:H	SiH_4, PH_3	40, 10	300	200	28	20
	a-Si:H	SiH_4/Ar 5%	120	750	250	36	5
	p-a-Si:H	SiH_4, B_2H_6	40, 4	680	170	28	10
	δn a-Si:H	SiH_4, PH_3	40, 10	300	200	28	5

emitter conductivity [10] by Cr evaporation and wet removal. At this stage a metallic mask has been held and fixed by a particular holder on the rear side of the device. This mask, fabricated from a 100 µm thick Molybdenum foil, has a comb shaped aperture obtained by Nd-YAG laser ablation. A dry etching procedure using NF_3 gas has been performed to remove the n-type a-Si:H portion not covered by the mask, using settings defined on the base of previous experiences [11]. Subsequently, keeping the mask in the same position, the cell base contact has been formed by an intrinsic a-Si:H buffer and a p-type a-Si:H layers, followed by a δn-a-Si:H deposition useful to increase the amorphous conductivity [10]. All the deposition conditions of the above mentioned layer in Table I are summarised. Then another comb shaped aperture mask, having narrower fingers with respect to the previous mask, has been held and fixed on the rear side of the device using the previously used holder. The aperture of each finger of this second mask is about the half of the first mask leading to not difficult mechanical alignment with the pattern underneath.
Through these aperture a 30 nm thick Cr followed by 4 µm Al layers have been evaporated. The Cr is used to form the CrSi layer on the p-type a-Si:H layer [10]. Finally, the mask has been rotated 180 degrees and 4 µm of Ag has been evaporated to contact the emitter region, creating the interdigitated shape with respect to the base contact. The total area of the solar cell is 6.25 cm^2. A schematic cross section of the BEHIND cell in Figure 1 is depicted. At this stage the BEHIND cells have been characterized in terms of current-voltage (I-V), both in dark and AM1.5G conditions, reflectance and Quantum Efficiency (IQE: Internal Quantum Efficiency; EQE: External Quantum Efficiency).

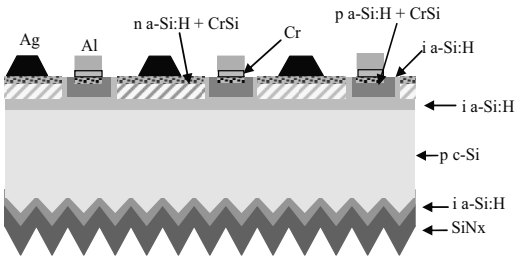

Figure 1: Schematic cross section of the BEHIND cell.

III. Results and discussion

The experimental IV characteristic has been measured at room temperature, under Class A calibrated to 1000 mW/cm2 and AM1.5g illumination and in Figure 2 is shown as symbols. Taking into account the best result of a silicon based interdigitated solar cell [1] we can see that the very high open circuit voltage Voc = 694 mV confirms the effectiveness of the a-Si/c-Si heterojunction as the way to improve the silicon based solar cell efficiency. This result also confirms that the uniformity of the deposited amorphous silicon layers is not influenced by the mask-assisted deposition process even when multiple masks are used in the fabrication process. Indeed the alignment between masks and substrate is feasible and the regions where the doped layers can unfortunately overlap are isolated by the intrinsic a-Si:H. The introduction of CrSi on p-type a-Si:H base contact has allowed to overcome the necessity of laser treatment to obtain an effective base contact [8]. This effect is more evident considering the band bending distribution at the p-S-Si/i-a:Si:H/p-a-Si:H interface, as simulated with a finite difference software [5] and reported in Figure 3 before (a) and after (b) the CrSi introduction at 1 sun illumination conditions. The CrSi layer enhances the tunnelling mechanism at the interface, resulting in a better hole collection. Moreover the CrSi formation on n-a-Si:H layer has produced an equipotential emitter surface that reflects in a higher cell Fill Factor (FF) by lowering the series resistance.

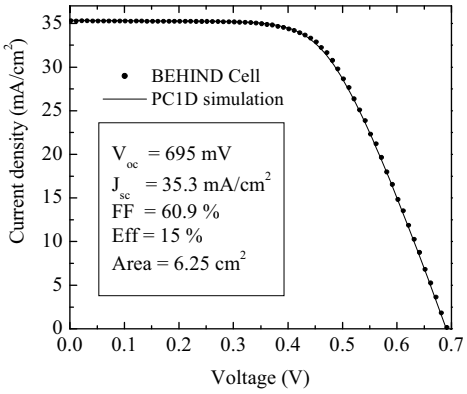

Figure 2: I-V measurements and photovoltaic parameters under AM1.5G condition: experimental data (symbols) and PC1D simulations (lines).

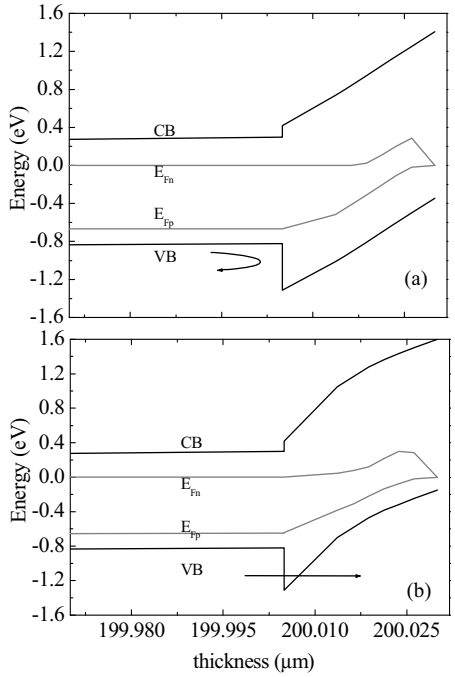

Figure 3: Band bending distribution before (a) and after (b) CrSi introduction simulated at 1 sun illumination condition.

As expected the short circuit current J_{sc} is higher than that collected by a grid shaped front contact cell, but in principle should be higher, so optical and recombination losses still affect the cell. To get better inside the limiting factor for J_{sc} a detailed analysis of the EQE has been performed using PC1D software [12].

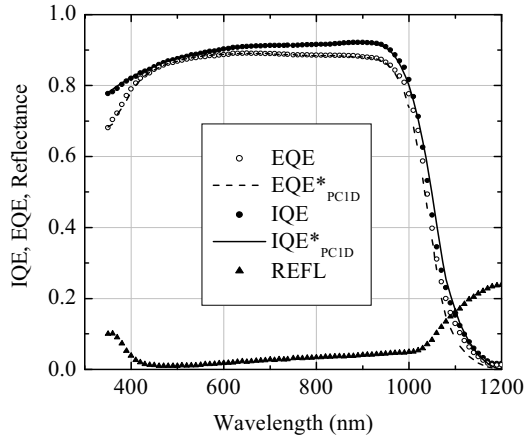

Figure 4: IQE, EQE, Reflectance of the BEHIND cell: experimental data (symbols) and PC1D simulations (lines).

Table II Parameters used in PC1D simulation.

c-Si parameters	
thickness (μm)	200
mobility μ_n , μ_p (cm^2/Vs)	1417, 470
bandgap (eV)	1.124
intrinsic conc. n_i (cm^{-3})	$1 \cdot 10^{10}$
p-type doping (cm^{-3})	$3.2 \cdot 10^{16}$
diffusion length L_d (μm)	680
front surf. rec. S_n,S_p (cm/s)	80
rear surf. rec. S_n,S_p (cm/s)	$1 \cdot 10^{6}$
a-Si:H parameters	
thickness (μm)	0.015
mobility μ_n , μ_p (cm^2/Vs)	1, 0.1
bandgap (eV)	1.65
intrinsic concentration ni (cm^{-3})	$1 \cdot 10^{7}$
μτ (cm^2/V)	$1 \cdot 10^{-12}$
n-type doping (cm^{-3})	$5 \cdot 10^{17}$
n^+-type doped (CrSi)	$5 \cdot 10^{18}$

The key issues to obtain high J_{sc} depends on diffusion length, L_d, and surface recombination velocity, $S_{n,p}$. To explore the effect of both parameters we have compared the EQE experimental data with a PC1D simulation, in which we have simplified our BEHIND cell into one dimensional crystalline based solar cell having a back thin n-type aSi:H emitter layer. A detailed description of parameters adopted in the simulation is reported in Table II. Those parameters have been fixed on the based of both c-Si and a-Si:H properties and on geometrical characteristic of the cell. The majority of parameters reported in Table I are commonly used in literature for both c-Si and a-Si:H materials [5]. Choosing appropriate L_d and $S_{n,p}$ values, and taking into account the measured reflectance profile, reported in Figure 4 as symbols, we have obtained a good agreement between experimental data and simulation model, except in the region of higher energy photons, since the simulation does not account for the passivation/antireflection coating absorption. So at the end of simulations, EQE, IQE data have been reduced by the a-Si:H thin layer (d = 3 nm) absorption and reported as EQE*and IQE* in Figure 4. The model suggests that with $S_{n,p}$ down to 10 cm/s and L_d up to 1 mm or the actual L_d = 680 nm and a wafer thickness thinner than 170 μm, it would be possible to reach the unity IQE value in the spectral range from 400 nm to 900 nm. In this improved version of the cell with respect to the previously shown in ref [8] the EQE curves does not show any hump related to the depletion region at the edge of the emitter in the spectral region ranging from 900 nm to 1000 nm as commonly appears on rear emitter cell having not sufficiently high L_d and not optimized finger number per square centimetres in the interdigitated rear geometry. This confirms the goodness of the actual fabrication process. Moreover the Reflectance profile measured and reported in Figure 3 remarks the efficacy of the texturization and antireflection coating, leading to an effective value of 4.6% if compared with the sunlight spectrum.

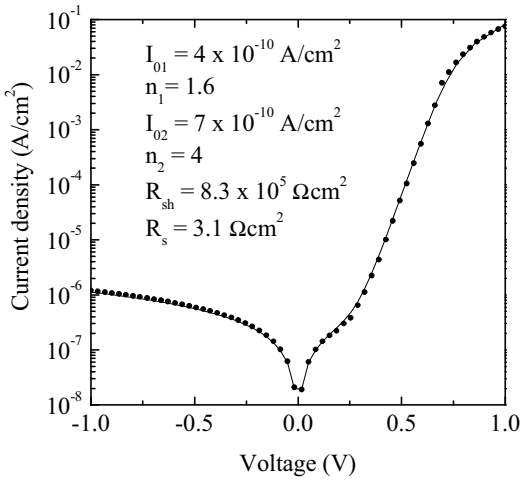

Figure 5: Experimental (symbols) and modelled (line) I-V characteristic at room temperature and dark conditions.

The second mask used for the metal deposition over the p-type a.Si:H base contact has been very helpful to reduce the shunt effect at the edge of the p and n contact that now are more pronounced due to increased n-type a-Si:H layer conductivity. Although this shunt effect is still evident from the I-V measurement performed in dark condition reported in Figure 5. In fact the dark current mainly flows between the fingers shaped back contacts. For this reason the area used in I-V dark evaluation is only that of the p-type base contact.

The I-V measurement can be modelled by the two diode model plus a series and a shunt resistance contributes.

$$I(V) = I_{01}\left(e^{\frac{V}{n_1 V_T}} - 1\right) + I_{02}\left(e^{\frac{V}{n_2 V_T}} - 1\right) + \frac{V}{R_{sh}}$$

Where I_{01} is the diode reverse saturation current; I_{02} accounts for recombination thermal generation currents in the depletion region; R_{sh} is the shunt resistance, n_1, n_2 are the ideality factors and V_T is the thermal equivalent voltage. By iterative solution it is possible to evaluate also the series resistance R_s. The parameter values used to fit the experimental data In the inset of Figure 5 are listed. At high current injection level the transport mechanism is dominated by the series resistance, as already seen in the lighted IV curve. From the latter analysis we can conclude that the recombination mechanism still limits the V_{oc}. However the built-in potential, arising from the c-Si/a-Si:H heterojunction, still remains sufficiently high to determine a V_{oc} value of 695 mV.

IV. Conclusions

In this paper we have shown the actual improvement of the BEHIND cell concept in which a-Si:H/c-Si heterostructures have been used to form an interdigitated emitter and base contacts. The grid-less front surface now ensures as high I_{sc} value as 35.3 mA/cm^2 due to improved diffusion length. With the aid of a PC1D model we have deduced that front surface recombination still limits the J_{sc} and we have also evaluated the effectiveness of CrSi to increase the transport reducing the series resistance. In turn, to form this layer, a secondary mask has been needed but this does not reduce the effectiveness of mask-assisted deposition process. Actually a V_{oc} of 695 mV has been reached, that can be considered a further improvement respect to the previous results to continue to develop this low temperature process helpful to reduce the PV manufacturing cost.

References

[1] R.M. Swanson, Proc. of the 31st IEEE PVSEC, Lake Buena Vista, (2005); pp. 889–894.

[2] W. P. Mulligan, M. A. Carandang, M. Dawson, D. M. De Ceuster, C. N. Stone, and R. M. Swanson, Proc. of XXI European Photovoltaic Solar Energy Conference (2006) pp. 1301-1303.

[3] M. Taguchi, K. Kawamoto, S. Tsuge, T. Baba, H. Sakata, M. Morizane, K. Uchihashi, N. Nakamura, S. Kiyama and O. Oota, Prog. Photovolt: Res. Appl. (2000) vol. 8 pp. 503-505.

[4] H. Angermann, J. Rappich, K. v. Maydell, E. Conrad, I. Sieber, D. Schaffarzik and M. Schmidt Proc. 21st EPVSEC, Dresden (2006) pp. 895-898.

[5] M. Tucci, G. de Cesare, J. Non-Cryst. Solids (2004) vol. 338 pp. 663-667.

[6] E. Maruyama, A. Terakawa, M. Taguchi, Y. Yoshimine, D. Ide, T. Baba, M. Shima, H. Sakata, and M. Tanaka, Proc. of 4th World Conference Photovoltaic Energy Conversion, (2006) pp. 1455-1458.

[7] M. Taguchi, A. Terakawa, E. Maruyama and M. Tanaka, Prog. Photovolt: Res. Appl. (2005) vol. 3, pp. 481-484.

[8] M. Tucci, L. Serenelli, E. Salza, S. De Iuliis, L. J. Geerligs, D. Caputo, M. Ceccarelli, G. de Cesare; Journal of non-crystalline solids (2008) Vol. 354, pp.2386-2391.

[9] M. Tucci and L. Serenelli; Thin Solid Films (2008) vol. 516 pp. 6939-6942.

[10] D. Caputo, G. de Cesare, M. Ceccarelli, A. Nascetti, M. Tucci, L. Meda, M. Losurdo, G. Bruno. Journal of non-crystalline solids (2008)vol. 354, pp. 2171-2175.

[11] M. Tucci, L. Serenelli, S. De Iuliis, E.Salza, L. Pirozzi. Proceeding of XXI European Photovoltaic Solar Energy Conference Dresden (2006) pp. 1250-1254.

[12] PC1D version 5.3 P.A. Basore, D.A. Clugston University of New South Wales (1998).

5. Emitter Optimization on a-Si:H/c-Si Heterojunction Solar Cells for Isotextured Wafers

J.W.A. Schüttauf, Y. Komatsu, L.J. Geerligs, Y. Mai, A. Bink, D.A. Spee, R.E.I. Schropp. 23rd European PVSEC, Valencia, 2008.

Emitter Optimization on a-Si:H/c-Si Heterojunction Solar Cells for Isotextured Wafers

J.W.A. Schüttauf[1], Y. Komatsu[2], L.J. Geerligs[2], Y. Mai[1], A. Bink[1], D.A. Spee[1], R.E.I. Schropp[1]

1. Utrecht University, Debye Institute for Nanomaterials Science,
Section Nanophotonics – Physics of Devices,
P.O. Box 80000, 3508 TA Utrecht, The Netherlands

2. ECN Solar Energy,
P.O. Box 1, 1755 ZG Petten, The Netherlands

ABSTRACT: In this work we report on the emitter optimization on isotextured n-type FZ c-Si wafers for a-Si:H/c-Si heterojunction solar cells. At ECN, three different types of isotexturing have been developed. From lifetime measurements performed on passivated isotextured wafers, it was concluded that two of the three types of texturing are compatible with our silicon heterojunction process. The next step was to optimize the heterojunction emitter on the isotextured wafers. The emitter structure, consisting of a thin intrinsic layer and a p-layer has been deposited in a medium sized area (30 cm x 40 cm) PILOT reactor by means of 13.56 MHz RF PECVD. As a p-layer, we found that an a-Si:H p-layer with a thickness of around 20 nm gave the best results. Finally, we performed a thickness series of an already optimized i-layer for the isotextured wafers. We found that the optimal i-layer thickness on these isotextured wafers (10 nm) is higher than on flat polished wafers (7 nm). The newly optimized structure finally led to an efficiency of 16.4% with a V_{OC} of 623 mV, a J_{SC} of 34.2 mA/cm^2 and a FF of 77%. An important next step in our research will be to extend the results shown in this paper to isotextured mc-Si wafers.

Keywords: Heterojunction, c-Si, isotexturing, PECVD

1 INTRODUCTION

Heterojunction solar cells based on amorphous and crystalline silicon are very suitable devices for low cost and high efficiency energy conversion. Sanyo showed an efficiency of 22.3% for a-Si:H/c-Si heterojunction solar cells with a thin intrinsic layer, which clearly demonstrates its feasibility as a concept for high efficiency solar cells [1]. This type of cell has already been brought to the market as well [2,3]. Compared to conventional (m)c-Si solar cells, a considerable cost reduction can be achieved because the fabrication process can take place at temperatures below 200^{o}C. Another advantage of a-Si:H/c-Si heterojunction solar cells are the better temperature characteristics compared to conventional c-Si solar cells.

Wafer texturing is a well-established way to increase the light trapping and thereby the light induced current density in c-Si based solar cells. The most common way to apply texturing to mc-Si wafers is by isotropic texturing using an acidic solution [4,5]. It has the huge advantage over alkaline anisotropic texturing that it does not form steps at the grain boundaries [6]. These steps make it very difficult to entirely cover the surface of the wafer with the emitter, which has a total thickness of only several tens of nanometers, whereas these steps at the grain boundaries are typically in the order of several microns [7].

In this work we report on the emitter optimization on different types of isotextured wafers for a-Si:H/c-Si heterojunction solar cells. The performance of the cells on textured wafers is compared to the performance on flat, double sided polished (DSP) wafers, which are used as a reference. The emitter structure has been deposited by means of a very simple process using 13.56 MHz RF PECVD in the PILOT medium size multichamber deposition system [8] at our laboratory with substrate temperatures not exceeding 200^{0}C.

So far, we have done our research on FZ c-Si wafers because there is less variation in neighboring wafers compared to mc-Si. In the future however, we want to extend this work to a-Si:H/c-Si heterojunction solar cells on isotextured mc-Si wafers.

2 EXPERIMENTAL

For this research, 2-5 Ωcm (100) n-type FZ c-Si wafers with an area of 5x5 cm^2 and a diffused back surface field (BSF) have been used. First, the wafers were dipped in HF (1% solution in H_2O) for 1 min. Thereafter, the thin intrinsic layer and the p-layer were deposited in a multichamber medium sized vacuum system, called PILOT [8]. The a-Si:H layers have been deposited by means of 13.56 MHz RF PECVD. For the thin intrinsic layer we have used pure silane. For the p-layer we used a gas mixture consisting of silane, hydrogen and $B(CH_3)_3$, which is also known as TMB. On top of the emitter structure, an 80 nm thick ITO layer has been deposited by RF magnetron sputtering. Finally, Ag contacts were evaporated on both sides of the cells. For the Ag evaporation on the top side, a mask has been used to define the grid pattern of the front contacts. On the back side, the cells were fully covered with Ag. After these deposition steps, the cells were annealed for 1 h at 160^{0}C in a N_2 atmosphere. The performance of the solar cells has been tested by means of I-V and spectral response measurements. The quality of the p-layers has been tested and optimized by means of conductivity (both dark and illuminated), activation energy and R/T measurements on Corning glass.

3 RESULTS AND DISCUSSION

3.1 Passivation Properties of Textured Wafers

In order to increase the light absorption of the wafers used in this research, three different types of isotexture (A,B and C) have been developed and investigated [7]. First, their passivation properties have been tested in order to evaluate their compatibility with the silicon heterojunction fabrication process and compared to the results on flat, double-side polished (DSP) wafers. This has been done by performing QSSPC [9] measurements on different device structures. On all samples, the textured front side was covered with a standard emitter, and the back side with surface passivating SiN_x:H [10]. As a reference, a sample with SiN_x:H deposited on both sides has also been provided. Figure 1 shows the effective lifetime (τ_{eff}) and implied V_{OC} at an injection level of 10^{15} cm^{-3} as determined from QSSPC measurements [7].

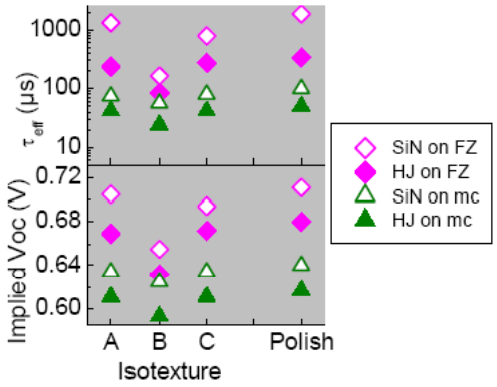

Figure 1: Effective Lifetime and Implied V_{OC} as measured by QSSPC for different types of texturization. The polished wafers are used as a reference. Courtesy of Y. Komatsu [7].

The results in Figure 1 show that the texturing types A and C show good passivation properties, almost as good as the reference sample. For type B, the effective lifetime of minority charge carriers is significantly lower than for the other samples. This indicates that texturing type B is not compatible with the silicon heterojunction process. Therefore, type B will not be considered any more in the rest of this work.

When incorporated into finished solar cells, the isotextured wafers show comparable V_{OC} values and slightly higher J_{SC} values compared to the results on flat DSP wafers. The higher J_{SC} values can be ascribed to the better light absorption of the textured wafers compared to the DSP wafers. The results are shown in Table 1.

Table 1: Output parameters for finished solar cells on flat DSP and isotextured FZ n-type c-Si wafers

Texture Type	V_{OC} (mV)	J_{SC} (mA/cm^2)
Flat DSP	613	32.3
A	617	34.0
C	610	34.0

The emitter structure which has been used so far, has not been optimized for the newly textured wafers yet. Therefore, the next step was to optimize this structure.

3.2 p-layer optimization

We tried to develop three different types of p-layers, i.e. a-Si:H, a-SiC:H and µc-Si:H and evaluated which structure is the most feasible for and compatible with our solar cells.

We have been able to fabricate good a-Si:H p-layers for our heterojunction solar cells. The activation energy was typically between 0.35 and 0.40 eV and when incorporated into solar cells we obtained proper fill factors. The optimal thickness of our a-Si:H p-layer was found to be 20 nm.

Compared to standard a-Si:H, layers consisting of a-SiC:H are expected to have a higher bandgap and thus a higher transparency. A disadvantage of a-SiC:H layers, which is caused by the carbon incorporation, is an increasing defect density which seems to have a detrimental effect on the performance of the cells. In practice, our a-SiC:H layers showed less good results than our a-Si:H p-layers. The activation energy was significantly higher and when incorporated into solar cells, the fill factor strongly decreased compared to cells with an a-Si:H p-layer. This clearly indicates that this a-SiC:H p-layer is too defective and that the doping efficiency is low.

Microcrystalline silicon usually has a higher conductivity and a lower absorption coefficient than amorphous silicon. Both of these properties are in principle beneficial for good p-layers. The main challenge when depositing a µc-Si:H p-layer in silicon heterojunction solar cells on top of a thin intrinsic layer consisting of a-Si:H is to achieve (micro)crystalline growth without a long incubation phase. This property is very critical because the optimal p-layer thickness is typically in the order of several tens of nanometers. First, individual p-layers have been deposited and optimized on Corning glass. Our a-Si:H layers showed proper results, both on glass and when incorporated in finished solar cells. The µc-Si:H layers, however, showed good results regarding conductivity and activation energy when deposited on glass, but did not show good results when incorporated in a cell. This could indicate that the growth of this layer is microcrystalline on glass, but amorphous on top of a c-Si wafer with a thin intrinsic layer. In order to test this, we deposited an i/p structure on glass, so the growth of the p-layer on top of the thin intrinsic layer could be studied. Raman spectroscopy showed that the growth of the p-layer directly on glass was microcrystalline, but on top of a thin intrinsic layer, the layer turned out to be amorphous. We tried this for an extensive range of deposition conditions, but in all cases the result was the same. The reason that we did not evaluate the crystallinity of the p-layer on top of a c-Si wafer with thin intrinsic layer is that Raman spectrum will be dominated by the wafer in that case.

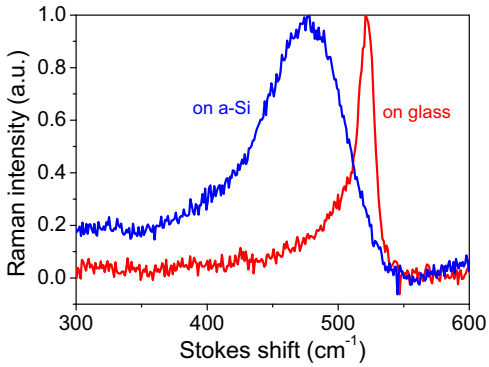

Figure 2: Raman Spectroscopy measurements for µc-Si:H p-layer on glass with and without thin intrinsic layer

So far we have succeeded to fabricate properly working a-Si:H p-layers for a-Si:H/c-Si heterojunction solar cells. For a-SiC:H and µc-Si:H p-layers, this has not been the case yet. In the case of µc-Si:H p-layers, this is due to the fact that only a thin intrinsic amorphous silicon layer can have a large influence on the nucleation of nanocrystallites. Therefore we decided to continue with the a-Si:H p-layer, combined with isotexture type C. Here, in fact, the choice between type A and C was arbitrary. The next step was to optimize the thickness of the thin intrinsic layer.

3.3 Thickness optimization of thin intrinsic buffer layer

The standard i-layer we have used in this research has been deposited at a relatively low substrate temperature of approximately 120^{0}C to prevent epitaxial growth onto the c-Si wafer. A relatively low deposition temperature combined with a high plasma power is expected to be the most suitable manner to prevent epitaxial growth onto the c-Si wafer [11]. In this research, only the thickness of this layer, combined with the new p-layer, has been optimized. The deposition conditions of the i-layer have not been changed.

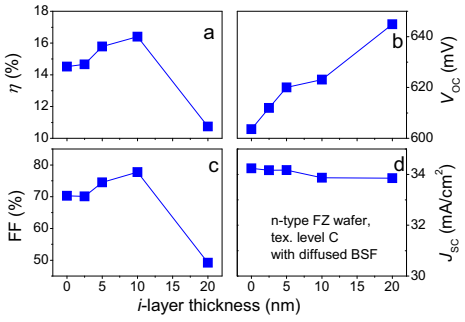

Figure 3 Output parameters for various i-layer thicknesses.

From figure 3b, it can be seen that the V_{OC} increases with increasing i-layer thickness, as can be expected due to improving surface passivation. For a thin intrinsic layer, the best surface passivation is expected to occur at several tens of nanometers [12]. The J_{SC} slightly decreases due to increasing absorption in the i-layer with increasing thickness. As can clearly be seen from figure 1c, the FF collapses for i-layer thicknesses above 10 nm. For such thicknesses, the holes cannot tunnel through the intrinsic layer any more and the layer acts as a barrier. The optimal layer thickness turned out to be approximately 10 nm, as can be seen from figure 3a. This thickness is higher than observed by most other groups [i.e.11,13] and previous work [14], which could be ascribed to the texturing of the c-Si wafers. It has to be said, however, that in our case the thickness of the thin intrinsic layer could only be estimated timewise, and might therefore be slightly overestimated.

3.4 Solar Cell Results

The newly developed solar cell structure, consisting of an isotextured c-Si wafer with diffused BSF, a 10 nm thick intrinsic layer and improved a-Si:H p-layer led to an efficiency of 16.4% with a V_{OC} of 623 mV, a J_{SC} of 34.2 mA/cm^2 and a FF of 77%.

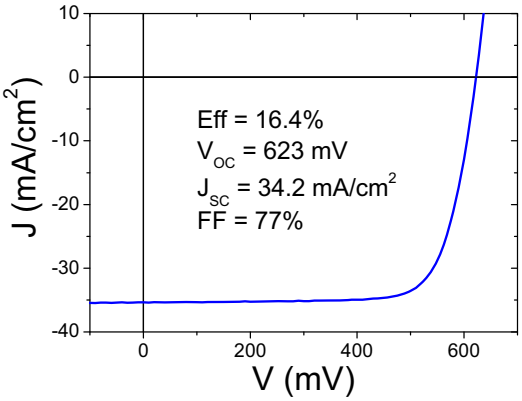

Figure 4, I-V curve of our present best cell with layers deposited in the medium-sized reactor.

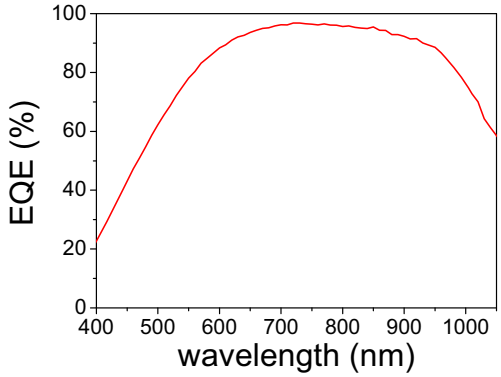

Figure 5, Spectral Response measurement of our best cell.

From the spectral response measurement shown in Figure 5, it can be seen that the cell performs very well for wavelengths between roughly 600 and 900 nm. For lower wavelengths, we can see that there is still some room for improvement. Especially the development of a thinner and more transparent emitter structure could be beneficial in this case.

4. CONCLUSIONS

We have investigated the influence of different types of isotexturing on the performance of a-Si:H/c-Si heterojunction solar cells. Compared to our results on flat DSP wafers, the cells on the textured wafers showed a considerable improvement in efficiency. Furthermore we optimized the emitter structure for the newly developed types of isotexturing. This emitter structure consists of a thin intrinsic layer with a thickness of 10 nm combined with a 20 nm thick a-Si:H p-layer. The optimal i-layer thickness was found to be higher than the optimal i-layer thickness for i-layers on flat wafers. The whole emitter structure has been deposited by 13.56 MHz rf PECVD. This finally led to an efficiency of 16.4% and a V_{OC} of 623 mV on isotextured n-type FZ c-Si wafers with diffused BSF. An important next step in our research will be, to optimize the performance of the solar cell structure described in this paper on textured mc-Si wafers. Also, the development of a deposited BSF should be mentioned.

5. ACKNOWLEDGMENTS

This project is undertaken with financial support from the Ministry of Economic Affairs of The Netherlands: program EOS (Energy Research Subsidy), project QC-Passi.

6. REFERENCES

[1] S. Taira and Y. Yoshimine, Proc. 22nd European Photovoltaic Solar Energy Conference (2007)

[2] E. Maruyama, A. Terakawa, M. Taguchi, Y. Yoshimine, D. Ide, T. Baba, M. Shima, H. Sakata and M. Tanaka, Proc. 4th World Conference on Photovoltaic Energy Conversion (2006)

[3] M. Taguchi, H. Sakata, Y. Yoshimine, E. Maruyama, A. Terakawa, M. Tanaka and S. Kiyama, Proc. 31st IEEE Photovoltaic Specialist Conference (2005)

[6] D. Sarti, Q.N. Lê, S. Bastide, G. Goaer and D. Ferry, Proc. 13th European Photovoltaic Solar Energy Conference (1995)

[7] Y. Komatsu, H.D. Goldbach, Y. Mai, A. Bink, S. De Iuliis, L.J. Geerligs and R.E.I. Schropp, Proc. 22nd European Photovoltaic Solar Energy Conference (2007)

[4] C.J.J. Tool, G. Coletti, F.J. Granek, J. Hoornstra, M. Koppes, E.J. Kossen, H.C. Rieffe, I.G. Romijn and A.W. Weeber, Proc 31st IEEE Photovoltaic Specialist Conference (2005)

[5] C.J.J. Tool, M. Koppes, E.J. Kossen, H.C. Rieffe, I.G. Romijn and A.W. Weeber, Technical Digest 15th International Photovoltaic Science and Engineering Conference (2005)

[8] H.D. Goldbach, A. Bink and R.E.I. Schropp, Amorphous and Nanocrystalline Silicon Science and Technology (2005), MRS Proc. MRS **862** (2005) A23.4

[9] A. Cuevas, R.A. Sinton, Progress in Photovoltaics, **5** (1997) pp.79

[10] I. Romijn, M. Koppes, E.J. Kossen, C.J.J. Tool and A.W. Weeber, Proc. 21st European Photovoltaic Solar Energy Conference (2006)

[11] H. Fujiwara and M. Kondo, Applied Physics Letters **90** (2007) 013503

[12] S. Olibet, E. Vallat-Sauvain and C. Ballif, Proc. 21st European Photovoltaic Solar Energy Conference (2006)

[13] D. Muñoz, C. Voz, I. Martin, A. Orpella, J. Puigdollers, R. Alcubilla, F. Villar, J. Bertomeu, J. Andreu, J. Damon-Lacoste and P. Roca i Cabarrocas, Thin Solid Films **516**-5 (2008) pp. 761

[14] H.D. Goldbach, A. Bink and R.E.I. Schropp, Journal of Non-Crystalline Solids **352** (2006) pp.1872

6. Multi-crystalline Silicon heterojunction solar cells

Simona De Iuliis, L.J. Geerligs, M. Tucci, L. Serenelli, M. Ceccarelli, G. de Cesare. 22nd European PVSEC, Milano, 2007.

MULTI-CRYSTALLINE SILICON HETEROJUNCTION SOLAR CELLS

Simona De Iuliis [1], L.J. Geerligs [1], M. Tucci [2], L. Serenelli [2], M. Ceccarelli [3], G. de Cesare [3]
[1] ECN Solar Energy, P.O. Box 1, 1755 ZG Petten, The Netherlands
Phone: +31 (0) 224-56-4723, Fax: +31 (0) 224-56-8214, E-mail: deiuliis@ecn.nl
[2] ENEA Research Centre Casaccia, via Anguillarese 301, 00123 Rome, Italy
[3] Department of Electronic Engineering University of Rome "Sapienza", via Eudossiana 18, 00184 Rome, Italy

ABSTRACT: In this work we present the results we obtained by processing 1 Ω*cm p-type alkaline textured multi-crystalline silicon wafers when a double hydrogenated amorphous/crystalline silicon heterojunction is applied to sandwich the substrate. At the sunward surface to form the emitter and at the rear side to act as back surface field. We investigate the efficiency limiting factors by evaluating the photogeneration mechanism and we address a way of improvement. Even if the obtained photovoltaic efficiency is not impressive (15%), it is worth to note that this result is one of the very few results obtained on hydrogenated amorphous/crystalline silicon heterostructure based on p-type textured multi-crystalline silicon wafer, and the best published up to now.

Keywords: Silicon, Heterojunction, a-Si.

1 INTRODUCTION

The hydrogenated amorphous/crystalline silicon (a-Si:H/c-Si) heterostructure have recently attracted new interest since have been deputed as one of the way to get close 25% of cell efficiency [1]. While very interesting results have been obtained on mono-crystalline silicon substrate, the silicon heterojunction (SHJ) based on multi-crystalline silicon (mc-Si) wafers still presents many aspects to be addressed and some questions still wait an answer [2-4].

Efficiency and carrier transport properties of a-Si:H/c-Si heterojunction solar cells are significantly affected by the c-Si surface conditionings prior the plasma deposition process and, of course, by the amorphous silicon deposition conditions.

The hydrogen plasma treatment could result in a useful defect (like dislocations and grain boundaries) passivation for multi-crystalline silicon. Likewise, if for mono-crystalline the choice of silane as a precursor gas for the amorphous deposition could not be the best and tetrafluorosilane should be preferred, for multi-crystalline it seems the right choice, again thanks to the hydrogen defect passivation. Moreover surface treatments, prior the amorphous silicon deposition, able to reduce the surface roughness and the steps between individual grains, must be investigated in order to avoid micro-shunt that can affect the open circuit voltage of the photovoltaic device.

In this work we present the results we have obtained processing 1 Ω*cm p-type alkaline textured multi-crystalline silicon wafers when a double a-Si:H/c-Si is applied to sandwich the substrate. At the sunward surface to form the emitter and at the rear side to act as back surface field (BSF). We have investigated on the efficiency limiting factors, and we have numerically modeled the solar cell internal quantum efficiency (IQE) to evaluate the photogeneration mechanism. By that we were able to estimate the thicknesses of the amorphous layers, the diffusion length of the minority carriers (L_n) and the back surface recombination velocity (S_b). We have also compared the performances of our heterostructure device to that of an industrial high efficiency solar cell, fabricated on sister substrate with a high temperature process, having a phosphorous diffused emitter and an alloyed aluminum/silicon back surface field (P-diffused and Al-BSF).

2 TECHNOLOGICAL ISSUES

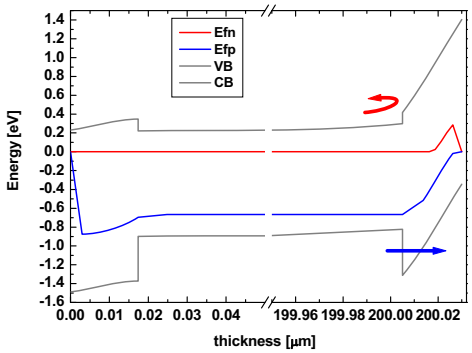

Figure 1: *Simulation with DIFFIN of the ideal band bending and carrier concentration at the back side of our heterostructure solar cell in AM1.5G condition. The dark lines correspond to the conduction and valence band.*

For n-type a-Si:H/p-type c-Si heterojunction surface passivation is still a challenge in order to obtain high open circuit voltage (>700 mV). Different approaches have been investigated to improve the interface with the c-Si substrate [5]. In addition, considering the p-type based HIT [3] cell, the band offset at the p-type c-Si/intrinsic a-Si:H/p-type a-Si:H interfaces, at the rear of the device, is influencing the photogenerated carriers collection from the back contact [6]. While the offset in the conduction band and the band bending can be useful as back surface barrier against electrons, the higher band offset in the valence band should behave as a barrier for the holes collection. A simulation of the back side behavior of the double SHJ solar cell based on p-type mc-Si wafer, by DIFFIN program, elsewhere presented [7], clearly describes this ideal situation, as reported in

Figure 1.

The key issue for the result of 17% efficiency on the heterostructure solar cell based on p-type mono-crystalline silicon, presented by the authors in 2003, was the chromium silicide (CrSi) [8]. We found that the formation of a CrSi film occurs at room temperature at the interface between amorphous silicon and chromium, and can be obtained by vacuum evaporation of chromium followed by a wet metal etching, performed with a solution of 30 g ceric ammonium nitrate, 9 ml glacial acetic acid and 200 ml deionized water. This process does not remove the CrSi film, but it just etches the metal in excess. The extension of this high conductivity layer inside the n-type doped a-Si:H has been estimated to about 10 nm [9]. Further investigation reduced this depth to few nanometers. It is important to note that the CrSi formation is independent from the electronic properties of the n-doped a-Si:H. In particular, we have also observed the presence of CrSi on n-layers grown at room temperature. Moreover this layer does not introduce any further absorption to the n-type doped a-Si:H. After several tests on amorphous silicon films, we found that the CrSi is formed only on n-type amorphous film, while its formation unluckily was inhibited on p-type or intrinsic material. Therefore we have adopted a different approach by adding a ultra thin n-doped amorphous silicon film (δn) deposited on the top p-type a-Si:H layer. This technological step has allowed us to form the CrSi film on the p-type a-Si:H-layer [10]. Very similar effect also happens on a p-type doped a-SiC:H. It is worth pointing out here that the p-δn structure does not behave as a junction due to the tunneling current caused by the high defect density of the doped layers. Then, this new kind of layer can be adopted in the heterojunction solar cell process technology in order to overcome the problem of low doping value and high activation energy of the p-type a-Si:H or p-type a-SiC:H layers used as a window layer in the heterostructure devices based on n-type crystalline silicon, or as back contact and BSF formation in the heterostructure devices based on p-type crystalline silicon.

3 EXPERIMENTAL

To fabricate heterostructure solar cells we have used 106 cm^2, 210 µm thick, 1 Ω*cm boron doped, multi-crystalline silicon as-cut wafer. A cross section of the solar cell is depicted in Figure 2.

This device presents a double heterojunction with silicon wafer: one at the front side, as Ag-grid/ITO/n-type a-Si:H/intrinsic a-Si:H; and the other at the back side, as intrinsic a-Si:H/p-type a-Si:H/ITO/Al. We have alkaline textured and industrially cleaned the wafer and then, after an 1% HF dip we have deposited the amorphous silicon layers in a three chambers 13.56 MHz RF PECVD reactor, using always the following conditions:

- 28 mW/cm^2 RF power density;
- 200 °C temperature;
- 300 mTorr pressure, and

adding the following gas mixtures:

1) 40 sccm SiH_4 flow for the intrinsic layer;
2) 10 sccm PH_3 and 40 sccm SiH_4 for the n-type layer;
3) 6 sccm B_2H_6 and 40 sccm SiH_4 for the p-type layer.

On the front side of the wafer we have deposited a 5 nm thick intrinsic a-Si:H buffer layer, and 10 nm thick *n*-type doped a-Si:H. On the rear we have deposited 5 nm thick intrinsic a-Si:H followed by a 15 nm thick *p*-type doped a-Si:H layer and a *δn* doped a-Si:H buffer layer. Afterwards we have evaporated and subsequently removed 30 nm thick chromium layer on both sides of the device to form the high conductivity CrSi layer. By sputtering system we have deposited the ITO layers, 67 nm at the emitter side and 80 nm at the back side, using the following conditions: ITO target, 25 sccm Ar, 5 sccm O_2, 150 °C, 200 W RF power. Finally, by e-beam evaporator, we have deposited 2 µm of Al on the whole surface of the cell, as back contact, , and 2 µm of silver (Ag) through a grid shape mask, as front metal grid. The total area of the device has been fixed at 4 cm^2.

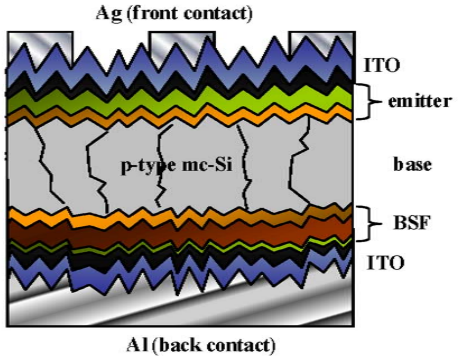

Figure 2: *Basic structure of our double heterostructure solar cell (not to scale).*

4 RESULTS AND DISCUSSION

The PV devices have been characterized by current voltage (I-V) measurements at standard conditions (100 mW/cm^2, AM1.5G and 25 C°), and by quantum efficiency (QE) in the range of 350-1200 nm. In Figure 3 the lighted I-V characteristic of the heterostructure solar cell is reported together with the evaluation of its photovoltaic parameters.

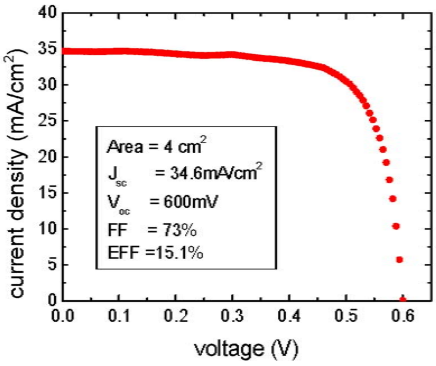

Figure 3: *I-V characteristic under standard conditions (100 mW/cm^2, AM1.5G and 25 C°) and photovoltaic*

parameters of the double heterostructure solar cell based on p-type mc-Si wafers.

The photovoltaic efficiency of this cell is still lower than that of the industrial high efficiency P-diffused and Al-BSF cell (15% vs. 17%). The fill factor and the series resistance are still the limiting factors; although the chromium silicide formation on the top of the amorphous films results in a series resistance reduction and a better charge collection.

The shunt resistance is strongly influencing the open circuit voltage. To prove this we have fabricated a sister wafer following the same process but chemically polishing, instead of alkaline texturing, the surfaces. The measured V_{oc} increased 30 mV (from 600 mV to 630 mV). This means that the thickness uniformity of the thin amorphous layers over a wide and textured silicon surface still requires further investigations.

Up to now just SANYO [3] has been able to produce high photovoltaic efficiency on 100 cm^2 substrate. All other research groups have obtained good results only on very small device.

Even if the obtained photovoltaic efficiency is not impressive, it is worth to note that this result is one of the very few results obtained on a-Si:H/c-Si heterostructure based on p-type textured multi-crystalline silicon wafer, and the best published up to now.

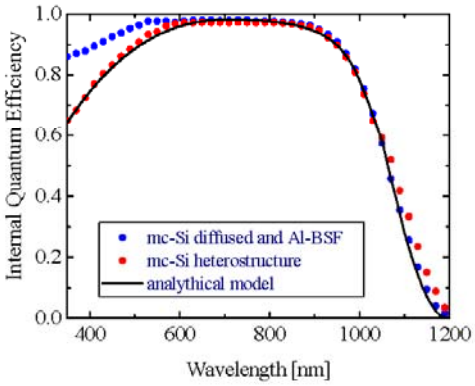

Figure 4: *Internal Quantum Efficiency comparison of our heterostructure device (red symbols) and P-diffused + Al-BSF solar cell (blue symbols) based on sister p-type mc-Si substrate. The line is the fit with an analytical model of the IQE data of the heterostructure cell.*

In Figure 4 the Internal Quantum Efficiency (IQE) data of the heterostructure solar cell are reported (red symbols) together with the simulation obtained by a simple analytical model (black line). This model takes into account the absorption coefficients ($\alpha(\lambda)$), the thickness of the materials, the depletion width, and the diffusion length in the crystalline silicon bulk. Of course, the photocurrent is as a sum of the two main components: drift at the depletion region and diffusion in the bulk. The carrier transport at the a-Si:H/c-Si interface, limited by the defect density, is restricted by the $\mu\tau$ product of the amorphous silicon, that has been fixed at 10^{-12} [cm^2/V]. By fitting procedure in the blue region of the spectrum this simple model is able to verify the thicknesses of the amorphous silicon layers not easy to control, since they are very thin. Indeed we have found that the n-type a-Si:H is 8 nm and the intrinsic a-Si:H is 5 nm. The value of the effective diffusion length of the minority carriers has been obtained by the linear behavior of the IQE vs $\alpha_{c\text{-}Si}(\lambda)$ at the edge of the silicon bandgap absorption and has been evaluated as 350 μm. Tunneling effect and other series resistance losses are not considered.

In the Figure 4 are also showed the IQE data (blue symbols) of the industrial high efficiency solar cell realized by a standard high temperature process (P-diffused and Al-BSF) using a sister substrate and having an efficiency of 17%.

In the blue region of the spectrum the IQE of the diffused cell is higher than one of the heterostructure. Even if the thicknesses of the amorphous silicon layers are very thin, their absorption represents a limiting factor. One way to improve the blue response is to optimize the front transparent conductive oxide (TCO) layer characteristics, like increasing its transparency and its conductance.

Since in the spectrum region between 900 nm and 1000 nm the IQE of both cells is almost equal we can assume an equal effective diffusion length (L_n). It is worth to note that the back contact of the diffused cell is ensured by the high temperature Al diffusion, able to produce a gettering of the bulk impurities and an effective surface field as well. Then we can deduce that also the heterostructure device has a similar effect. Probably the intrinsic a-Si:H layer is able to passivate the back side of the silicon wafer and the p-type a-Si:H/CrSi/ITO stuck layers are able to promote a good extraction of holes. Moreover the heterostructure device presents a quite higher internal reflectance, as evident comparing the IQE of both cells in the spectrum region between 1050 nm and 1200 nm. This means that the mirroring effect of the a-Si:H/ITO/Al structure deposited on a textured surface is better than that of Si/Si-Al-alloy/Al.

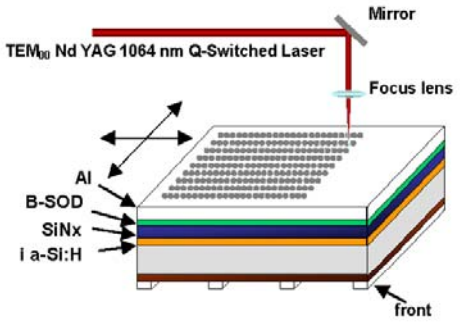

Figure 5:. *Basic structure of our alternative heterostructure solar cell having a SHJ as emitter and at the back the stuck layers : (intrinsic a-Si:H/SiN_x/B-SOD/Al) + processed by laser to get the localized BSF (not to scale).*

To increase the holes collection at the back metal contact a thickness reduction of the deposited a-Si:H layer at the rear is needed together with a reduction of the activation energy of the p-type doped a-Si:H layer. The

application of CrSi layer at the back side of the cell before the ITO deposition goes in this direction and can also reduce the contact resistance between the p-type doped a-Si:H and the ITO layers.

To further increase the infrared response of our device we are investigating a new back side scheme (see Figure 5) that replaces the rear heterostructure with the following stack layers: intrinsic a-Si:H/SiNx/B-SOD/Al. After the deposition of these layers the rear side has been treated by a laser assisted process to get localized back surface field [11]. The results in terms of IQE are showed in the Figure 6.

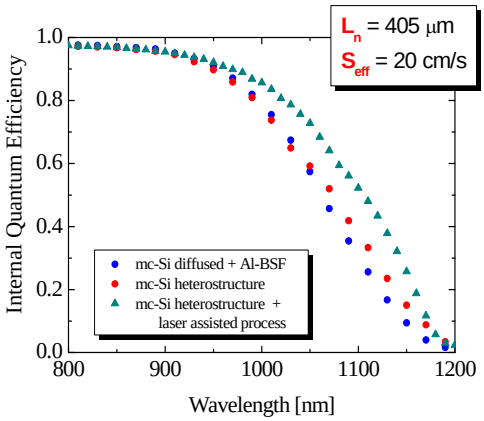

Figure 6:. *Internal Quantum Efficiency data comparison of the double heterostructure device (red symbols), of the P-diffused + Al-BSF solar cell (blue symbols), and of the solar cell having a SHJ as emitter and the stuck layers intrinsic a-Si:H/SiNx/B-SOD/Al + laser assisted process at the back. The devices are based on sister p-type mc-Si substrates.*

The first obtained results are very good in terms of L_n (from 350 μm to 450 μm), and J_{sc} (an increase of about 4 mA/cm^2). The S_{eff} at the back has been evaluated as 20 cm/s, but there is enough room to improve this parameter by optimizing the surface pre-treatment prior the amorphous silicon deposition. Finally it is worth to point out that the entire process still remains performed at low temperature.

5 CONCLUSION

We have fabricated double amorphous /crystalline silicon heterojunction solar cell on 1 Ω*cm p-type alkaline textured multi-crystalline substrate with 15% of efficiency. In order to increase the hole and the electron collection, respectively, at the back side and at the front side of the cell; we have deposited a chromium silicide film between the amorphous silicon and the transparent conductive oxide layers. The role of this buffer layer has been detailed investigated. We have discussed the transport mechanism at the rear side of the device by modeling the heterostructure device. Even if the PV performances we have got are still below that one obtained by using the high temperature technology (15% vs. 17%); it is worth to note that is the best published result on multi-crystalline silicon HIT structure up to now. Finally we have introduced a new promising low temperature design for SHJ solar cells based on p-type mc-Si wafers, having an a-Si:H/c-Si heterostructure as emitter and a stuck layer of intrinsic a-Si:H/SiNx/B-SOD/Al at the rear of the device, followed by a laser assisted process to get localized back surface field.

6 ACKNOWLEDGEMENTS

This work was supported by the Dutch SenterNovem Agency within the QCPassi Project.

7 REFERENCES

[1] R.M. Swanson; *Proc. of the 20th EPVSEC, Barcelona, 2005; 584.*

[2] Mikio Taguchi, Akira Terakawa, Eiji Maruyama and Makoto Tanaka, *Prog. Phototovolt: Res. Appl. 2005; 13: 481-488.*

[3] http://www.sanyo.co.jp/clean/solar/hit_e/hit.html.

[4] L. Korte, E. Conrad, H. Angermann, R. Stangl, M. Schmidt; *this conference 2DP.1.4.*

[5] E. Conrad, L. Korte, K. v. Maydell, H. Angermann,C. Schubert, R. Stangl, M. Schmidt; *Proc. 21st EPVSEC (2006) 784.*

[6] T.H. Wang, M.R. Page, E. Iwaniczko, D.H. Levi, Y. Yan, H.M. Branz, Q. Wang, V. Yelundur, A. Rohatgi, G. Bunea and A. Terao; *Proc. of the 14th Workshop on Crystalline Silicon Solar Cells and Modules Winter Park, Colorado August 8–11, 2004.*

[7] D. Caputo, U. Forghieri, F. Palma; *Journal Appl. Phys. 82 (1997) 733.*

[8] M. Tucci, G. de Cesare; *J. Non-Cryst. Solids 338 (2004) 663.*

[9] D. Caputo, G. de Cesare, A. Nascetti, M. Tucci; *Thin Solid Films (in press, available online 17 January 2007).*

[10] D. Caputo, G. de Cesare, M. Ceccarelli, A. Nascetti, M. Tucci, L. Meda, M. Losurdo, G. Bruno; *J. Non-Cryst. Sol. (in press, 2007).*

[11] L. Kreinin, N. Bordin, J. Broder, N. Eisenberg, M. Tucci, E. Talgorn, S. De Iuliis, L. Serenelli, M. Izzi, E. Salza, L. Pirozzi; *Proc. of 21st EPVSEC (2006) 855.*

7. Thin p^{++} μc-Si layers for use as back surface field in p-type silicon heterojunction solar cells

H.D. Goldbach *, A. Bink, R.E.I. Schropp, Journal of Non-Crystalline Solids **352**, 1872 (2006)

Available online at www.sciencedirect.com
SCIENCE DIRECT®
Journal of Non-Crystalline Solids 352 (2006) 1872–1875
JOURNAL OF NON-CRYSTALLINE SOLIDS
www.elsevier.com/locate/jnoncrysol

Thin p^{++} μc-Si layers for use as back surface field in p-type silicon heterojunction solar cells

H.D. Goldbach *, A. Bink, R.E.I. Schropp

Utrecht University, Faculty of Science, Department of Physics and Astronomy, SID – Physics of Devices, PO Box 80000, 3508 TA Utrecht, The Netherlands

Available online 17 April 2006

Abstract

A p^{++} μc-Si:H layer for the use as *deposited* back surface field (BSF) has to be highly doped in order to achieve a truly functioning BSF. We optimized a p^{++} μc-Si:H deposited on glass in terms of activation energy by varying the deposition parameters. The activation energy of the 30 nm thick μc p^{++} layer on glass reaches an optimum at $E_a = 0.15 \pm 0.01$ eV at a flow ratio TMB/SiH_4 of 0.016. To obtain a measure of the value of the activation energy of the p^{++} μc-Si:H layer on wafers, the layers were deposited on highly crystalline intrinsic μc-Si:H layers due to which the incubation layer of the μc p-layer can be avoided. The optimum TMB flow is higher on the microcrystalline i-layer, simulating the wafer, and the activation energy is greatly reduced to $E_a = 0.08 \pm 0.01$ eV. The best bifacial silicon heterojunction cell (SHJ) using such a low activation energy layer as the deposited BSF has an active area efficiency of 14.87%. This is high compared to the efficiency of 11.86% for the cell without BSF, due to a 22.4 mV higher V_{oc} and a 4.6 mA/cm^2 higher J_{sc}, demonstrating that the deposited BSF performs successfully.

PACS: 85.30.De; 81.07.Bc; 81.15.Gh; 84.60.Jt

Keywords: Solar cells; Heterojunctions; Photovoltaics; Electrical and electronic properties; Band structure; Films and coatings; Chemical vapor deposition; Plasma deposition; Microcrystallinity

8. Remote linear radio frequency PECVD deposited high quality a-Si:H(p) layers and their application in Si heterojunction structures

Y. Wu, C. Devilee, B.B. van Aken, K.. Boulif, W.J. Soppe, A.W. Weeber, L.J. Geerligs, Proceedings of the IEEE PV Specialists Conference, Philadelphia, USA, June 2010, to be published.

Y. Wu, C. Devilee, B. B. Van Aken, K. Boulif, W. J. Soppe, A. W. Weeber, L. J. Geerligs
ECN Solar Energy, PO Box 1, 1755 ZG Petten, The Netherlands

ABSTRACT

In this paper, we report on deposition and properties of high quality boron doped p-type amorphous Si (a-Si:H(p)) layers on n-type float zone Si(100) wafers by remote linear radio frequency plasma-enhanced CVD. The a-Si:H(p) layers show excellent surface passivation that is comparable to the one of a-Si:H intrinsic layers (a-Si:H(i)), and high stability of the passivation when stored in the dark . Additionally, the measured dark conductivity of deposited a-Si(p) is increased up to $>7\times10^{-6}$ S/cm by annealing. In a Si heterojunction cell structure, the a-Si:H(p) layer will be the emitter on an n-type base wafer. The effective lifetime of test structures of a-Si(p)/c-Si(n)/a-Si(n) has approached 1 ms, and a high pseudo fill factor and open circuit voltage have been obtained from a SunsVoc measurement. We conclude that these a-Si:H(p) layers are very promising for the application in high performance silicon heterojunction solar cells without using an intermediate a-Si:H(i) layer.

INTRODUCTION

The silicon heterojunction solar cell (SHJ), with a record efficiency of 22.3% reported by Sanyo in 2007 [1], has attracted extensive attention all over the world. Recently 23% have been reached (http://www.pv-tech.org/news/_a/sanyo_a_hit_with_23_solar_cell_efficiency_record/)

So far, many efforts have been made in order to understand the role of the amorphous Si layer in the heterojunction solar cell such as: 1) modeling the surface passivation of the amorphous silicon layer on the crystalline silicon wafer to understand its fundamental physical mechanism [2]; 2) studying and engineering the electronic band structure in order to improve the charge transport across the silicon heterojunction structure [3]; 3) experimentally optimizing the amorphous silicon deposition condition aiming at a high quality layer and device [4, 5].

The SHJ process is already well-known for its outstanding properties compared to the conventional solar cell process: 1) the SHJ formation is a process carried out at low temperature (< 200°C) with a very short deposition period; 2) doped a-Si:H for emitter and back surface field (BSF) can be produced via tuning the dopant species and deposition parameters; 3) a-Si:H(i) was demonstrated to result in excellent surface passivation [6].

High quality a-Si:H(i) thin layers (thickness of around 5 nm) play a very important role in the performance of the usual SHJ cells. To achieve such extremely thin and homogenous layers with a high surface passivation is not an easy task and the characterization of such kind of layers *ex-situ* is almost impossible due to their instability in ambient. Olibet et al. found that the surface passivation of a-Si:H(i) varied with the layer thickness and the best surface passivation was obtained at a layer thickness of 40 nm. The passivation degraded both with decreasing and increasing thickness, due to either less layer relaxation or mechanical stress respectively [7]. Therefore, for passivation, the intermediate a-Si:H(i) layer with a thickness of 5 nm is not the best choice. However, with increasing layer thickness, such insulating layers can greatly reduce the charge transport between silicon wafer and amorphous doped layer, and also increase the light absorption.

Depositing a-Si:H(p/n) directly on the Si wafer is another option but there is usually an inferior surface passivation due to the recombination via the interface defects, which are produced by the dopant species. So far, there was only one report of succeeding in the high performance Si heterojunction cell produced without intermediate a-Si:H(i) from K. V. Maydell et. al.[8].

In this work, we apply a new method, remote linear radio frequency plasma-enhanced CVD (rf-PECVD), to produce high quality a-Si:H(p) layers directly on the mono-crystalline silicon (100) wafer. It not only results in a very good surface passivation that is comparable to its intrinsic counterpart, but the layers also posses a high dark conductivity. The surface passivation of such a-Si:H(p) as a function of layer thickness and applied dopant flow rate is investigated. The lowest surface recombination velocity S_{eff} ~7 cm/s is obtained at a layer thickness of ~70 nm. A range of dopant gas flow rates for achieving both good surface passivation and conductivity has been defined. A stable effective lifetime (τ_{eff}) is demonstrated for a thin (~20 nm) a-Si:H(p) layer. The surface passivation of various cell structures is investigated and the pseudo fill factor and open circuit voltage (V_{oc}) are studied by using the SunsVoc measurement.

EXPERIMENTS

N-type float zone silicon (100) wafers (diam.=100 mm) with a thickness of 250 μm and a resistivity of 2.3 Ωcm were used as the substrates for the amorphous silicon layer deposition. Prior to the deposition, chemical cleaning and a short HF dip were performed. After the HF dip, the wafer is transported into the high vacuum chamber of the rf-PECVD within a short time to avoid surface degradation.

For studying the single a-Si:H(p) layer, we deposit a thick, passivating a-SiN_x layer [9] on one side of the wafer by using a separate Microwave PECVD system. This assures a good surface passivation, which normally yields τ_{eff} > 1 ms. The a-Si:H(p) is deposited on the other side for this study.

The a-Si:H(p) layer deposition is carried out in the p-chamber of rf-PECVD system equipped with a rf plasma source (13.56 Mhz) [10]. The PECVD chamber has a layout as shown in figure 1. This system is able to deposit layers with mild ion energy, which would not easily damage the wafer surface. Beside SiH_4 and H_2 gas, a (B_2H_6 + H_2) gas mixture was introduced in the deposition for the p-type doping process. The ratio B:Si was varied by tuning the gas flow rate.

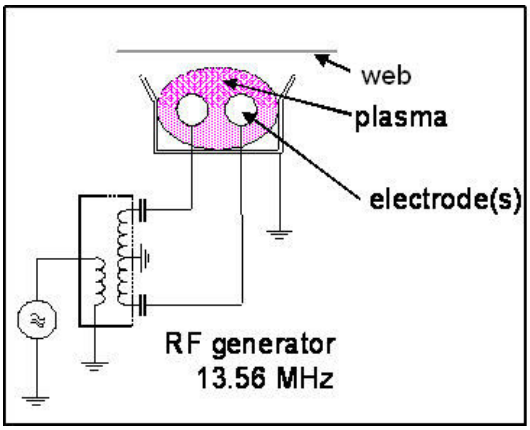

Figure 1: schematic drawing of the remote linear radio frequency plasma enhanced CVD system. The web carries the wafers (face down).

In the formation of the cell structure of a-Si:H(p)/c-Si(n)/a-Si:H(n), a-Si:H(n) layers were deposited in the n-chamber of rf-PECVD system with the same plasma source. (PH_3 + H_2) gas mixture was used as dopant gas for the n-type doping.

Post annealing was commonly applied right after the deposition in our experiments. It was performed in a conventional box furnace in air. The τ_{eff} was measured by the Sinton WT 120 in the transient mode and it was extracted at a charge carrier density of $10^{15}/cm^3$. The stability of surface passivation as a function of time was measured for a thin a-Si:H(p) layer (~20nm), which was kept in the dark and in the air. *ex-situ* ellipsometry (SE850, Sentech Instrument Gmbh) was used to determine the amorphous nature of the deposited layers. The dark conductivity measurement was carried out by the two probe method using a Keithley 595 Quasistatic CV Meter. The conductivity samples were simultaneously deposited on glass substrates; coplanar aluminum contacts were later evaporated by using the e-beam. To quantify the SHJ p/n/n cell structures, ITO layers were sputtered on both front and rear sides of wafer and a Ag layer was sputtered on the rear side as the back contact. SunsVoc measurements resulted in the pseudo fill factor and open circuit voltage (V_{oc}).

RESULTS AND DISCUSSIONS

Figure 2 plots the surface recombination velocity s of the a-Si:H(p) layers on Si(100) as a function of layer thickness. As shown in the inset of figure 2, the samples include a-Si:H(p) layer deposited on the front side of wafer and a high

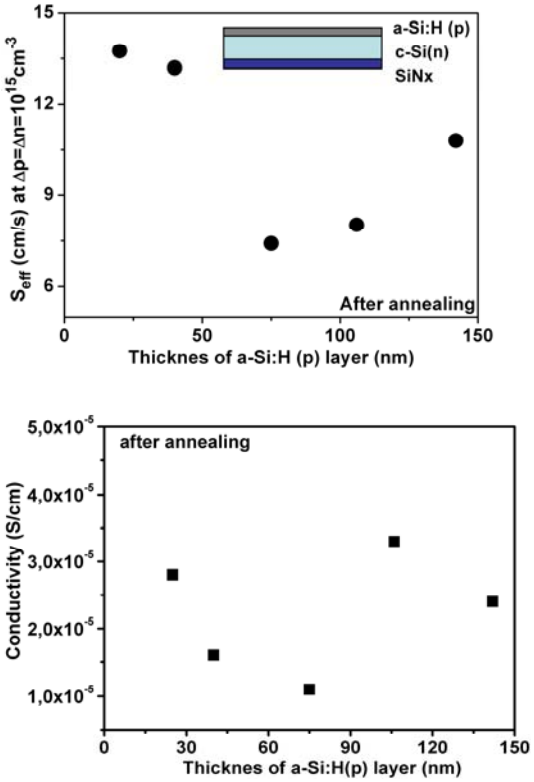

Figure 2: surface recombination velocity of annealed a-Si:H(p) layers as function of layer thickness (upper); dark conductivity obtained for the same a-Si:H(p) layers as function of layer thickness (lower).

quality SiNx layer deposited on the rear side of wafer, which can secure a very good surface passivation. The recombination velocity is converted from measured τ_{eff} and is approximated by the equation $\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{2S}{W}$, in which τ_{bulk} is the bulk lifetime assumed to be infinite; S is the recombination velocity and W is the wafer thickness. S is thus practically the average of the respective S of the SiNx and the a-Si(p):H. It is noticed that the smallest recombination velocity is obtained for the layer with a thickness of ~70 nm. Furthermore, it shows a comparable surface passivation to that of the a-Si:H(i) layer reported by Olibet et al. [11]. When reducing the layer thickness down to 20 nm, the recombination velocity increases to 2 times higher than that at 70 nm indicating the degradation of the surface passivation for thinner a-Si:H(p) layer. This shows a similar trend as the behavior of a-Si:H(i) and it is attributed to the insufficient relaxation of the thin layer [7]. In the lower part of figure 2, the dark conductivity has been extracted by using two probe measurements. Clearly, all the results are well above 1×10^{-5} S/cm strongly demonstrating that the deposited layers are effectively doped.

To investigate the structure of the deposited layer, we applied an *ex-situ* ellipsometry measurement. As shown in figure 3, layers with high τ_{eff} show the typical curve for amorphous Si. However, for the one with very low τ_{eff} = 35 μs, as shown by the blue dashed curve, a crystalline–like step is found. These results are well consistent with previous ellipsometry studies [12,13].

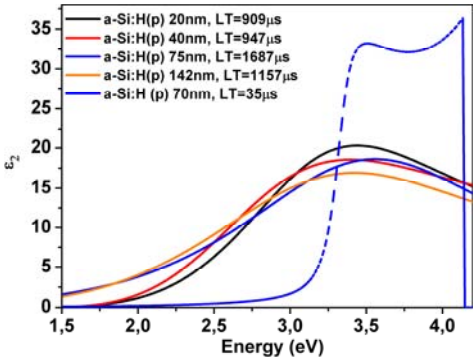

Figure 3: typical amorphous layer property is demonstrated from the ellipsometry measurement of the dielectric constant (imaginary part) as a function of wavelength.

Stability of surface passivation as function of time is another important issue because it can strongly impact to the performance of heterojunction solar cells. In this study, the surface passivation stability was investigated by means of measuring the τ_{eff} for an annealed a-Si:H(p) layer with a thickness of ~20 nm, which does not have any protecting capping layer and is stored in the dark, and in air. τ_{eff} was measured after every 10 days as shown in figure 4. Only slight fluctuations of the measured lifetime of less than 5% are noticed. There is no obvious degradation of surface passivation for the deposited thin a-Si:H(p) layer even for more than a month after the initial annealing. So far, we don't have the results concerning to the passivation stability of such kind of p-layer storing under the light yet.

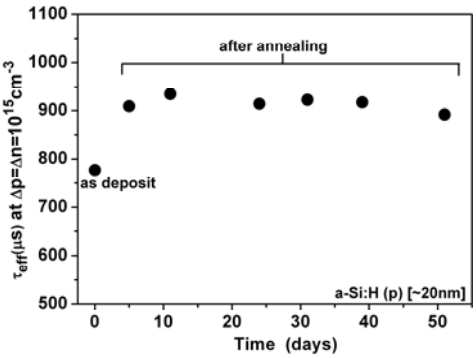

Figure 4 investigation of lifetime stability of deposited a-Si:H(p).

The influence of the dopant flow rate in the deposition on the surface passivation was also studied. The surface recombination velocity and dark conductivity after the annealing process, plotted as a function of dopant gas flow rate, are indicated in figure 5. The surface recombination velocity and dark conductivity both decrease with reduced flow rate of dopant gas. These results qualitatively suggest that reducing the dopant concentration in the deposited layer can suppress

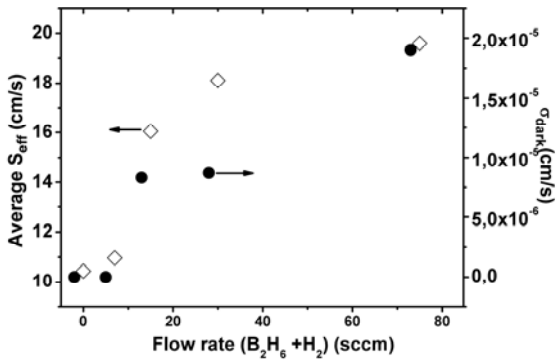

Figure 5 surface recombination velocity and dark conductivity of a-Si:H(p) [thickness = 50 nm] are indicated as function of applied dopant gas flow rate.

the density of defects which induce charge recombination at the interface. However, with a too low flow rate (i.e. <15 sccm), although the surface passivation is enhanced, there is a large decrease of the dark conductivity of deposited a-Si:H(p). Based on these results, we suggest that: 1) with very low flow rate in terms of very low dopant concentration, a higher quality amorphous layer, which is comparable to the a-Si:H(i), can be achieved. This is possibly assisted by the so called "microdoping", which may cause the field effect passivation at the interface [2]; 2) to achieve a reliable surface passivation and good conductivity simultaneously for the deposited a-Si:H(p) layer, a compromise doping process should be considered.

High quality doped a-Si:H(p) layers with and without a-Si:H(i) buffer layers were deposited as an emitter on the polished front surfaces of n-type

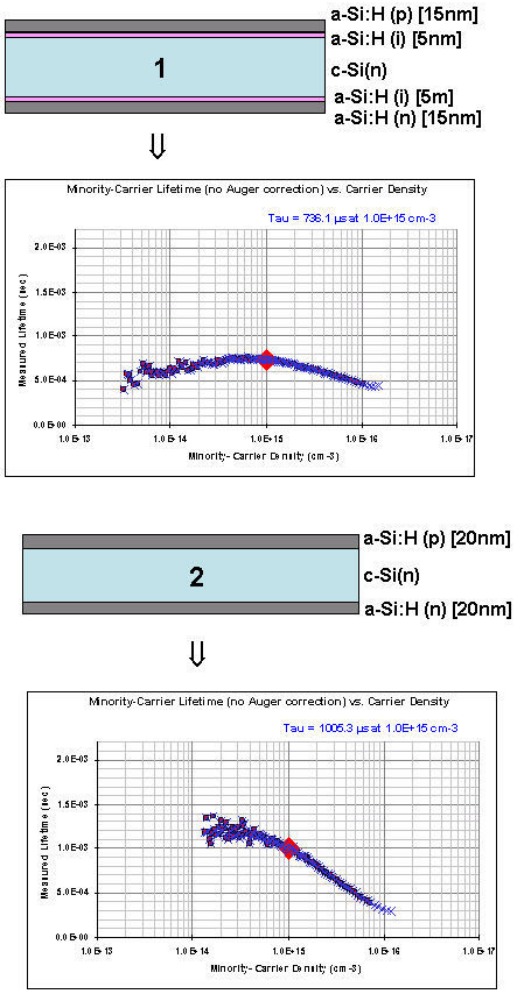

Figure 6 schematic drawing of stack layer 1 and corresponding minority charge carrier lifetime (upper); schematic drawing of stack layer 2 and corresponding minority charge carrier lifetime (lower).

float zone Si(100) wafer as shown in the schematic drawings of figure 6. An a-Si:H(n) layer was deposited on the rear side of wafer as BSF, also with and without intrinsic buffer layer. Stack 1 is formed by a-Si:H(p) /c-Si(n) /a-Si:H(n) and stack 2 is formed by a-Si:H(p) /a-Si(i) /c-Si(n) /a-Si:H(i) /a-Si:H(n). The a-Si:H(i) layers in stack 2 were introduced to improve the passivation and produced separately in either n or p chamber; the doped layers were deposited on top without breaking the chamber vacuum. The surface passivation quality of each stack is indicated accordingly in figure 6. A better surface passivation (τ_{eff} = 1.0 ms) is observed for stack 2 than for stack 1 (τ_{eff} = 0.74 ms). The surface passivation achieved for stack 2 is comparable to the single a-Si:H(p) shown in figure 4 indicating a consistent layer quality. The lower surface passivation for stack 1 is apparently related to the very thin (~5 nm) a-Si:H(i) layer.

In table 1, we compare the dark conductivity measured for single a-Si:H(p) layers with the a-Si:H(p)/a-Si:H(i) stack. After annealing, the conductivity is increased for both cases, but the conductivity of the i/p stack is about 2-3 orders of magnitudes lower than those of the single a-Si:H(p) layers. This indicates that the conductivity can be greatly improved by removing the intermediate a-Si:H(i) layer. Whilst still keeping a good surface passivation, such kind of a-Si:H(p) layer will be favored for the device fabrication.

	σ_{Dark} (S/cm) before anneal	σ_{Dark} (S/cm) after anneal
p-layer 1 [20nm]	**2.0E-7**	**8.3E-6**
p-layer 2 [20nm]	**7.2E-7**	**3.7E-5**
i[5nm]/p[15nm]	**1.0E-9**	**6.8E-8**

Table 1 dark conductivity measured on a-Si:H(p) layer and on a-Si:H(p) / a-Si:H (i) stack,.

By using the SunsVoc measurement, we further demonstrate the advantages of depositing the a-Si:H(p) layer directly on the Si wafer. In figure 7, pseudo J-V curves show the high quality silicon heterojunction without indicating any obvious shunt for both kinds of the stack layers. Pseudo fill factor and V_{oc} are extracted by averaging measurements on 5 different points on the wafers. As seen in figure 7, a high V_{oc} (> 670 mV) has been obtained for both stacks. It indicates that the surface passivation of both stack layers is still good after ITO deposition and Ag back contact deposition. A much higher pseudo fill factor FF = 0.84 is obtained for stack 2 than that (pseudo FF = 0.80) of stack 1. These results indicate that the stack layer without intermediate a-Si:H(i) has a better behavior than the one with the a-Si:H(i) when neglecting the series resistance. Hence, we

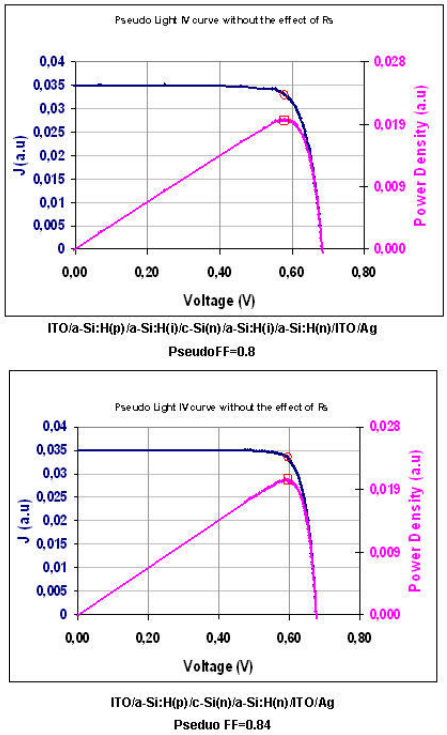

Figure 7 J-V curve is plotted for stack 1 (upper) & 2 (lower) respectively and the extracted pseudo fill factor is shown.

believe, also in the real solar cell, a better performance will be achieved on the stack layer 2 since it has also been demonstrated to have a better conductivity in the doped layers, and contact resistance can be expected to be further reduced in the absence of intrinsic buffer layers [14].

CONCLUSIONS

High quality a-Si:H(p) layer has been successfully deposited directly on the n-type float zone Si(100) wafer using remote linear rf-PECVD. The thin a-Si:H(p) layer (~20 nm) results in an effective surface passivation, which is comparable to that of the conventionally used a-Si:H (i) layer. It also shows stability of the good surface passivation with time, in the dark, and in air. Furthermore, the conductivity of the a-Si:H(p) layer has been greatly improved by annealing without losing the high surface passivation property. This indicates a potentially reliable application of the a-Si:H(p) layer for the silicon hereojunction solar cell resulting in a better conversion efficiency performance. Future studies will mainly be focused on front contact optimization and series resistance improvement.

ACKNOWLEDGEMENTS

We acknowledge the financial support by SenterNovem, for QCpassi, project no EOSLT 03011.

REFERENCES

1. S. Taira, Y. Yoshimine, T. Baba, M. Taguchi, T. Kinoshita, H. Sakata, E. Maruyama, M. Tanaka, 22nd, EPSEC, Milan, Italy, 3-7 September, 2007.

2. S. Olibet, E. Vallat-Sauvainm C. Balif, Phys. Rev. B, Vol 76, 035326,2007.

3. T.H. Wang, M.R. Page, E. Iwaniczko, D.H. Levi, Y. Yan, H.M. Branz and Q. Wang, 14th workshop on crystalline silicon solar cells and module, Winter Park, Colorado, August 8-11, 2004.

4. T.H. Wang, E. Iwaniczko, M.R. Page, D.H.Levi, Y. Yan, H.M. Branz, Q. Wang, Thin Solid Film, Vol. 501, 284 ,2006.

5. H. Fujiwara and M. Kondo, Appl. Phys. Lett. Vol. 90, 013503, 2007.

6. I. J. Pankove and M. L. Tarng, Appl. Phys. Lett. Vol. 34, 156, 1979.

7. S. Olibet, PhD thesis “Properties of interface in amorphous / crystalline silicon heterojunction”, Page 117, 2009.

8. K.V.Maydell, E. Conrad and M.Schmidt, Prog. in Photovolt: Res. Appl. Vol 14, 289, 2006.

9. W. Soppe, H. Rieffe, A. Weeber, Prog. in Photovolt: Res. Appl. Vol.13, 551, 2005.

10. H. Schlemm, M. Fritzsche, D. Roth, Surf & Coat. Tech., Vol. 200, 958, 2005.

11. S. Olibet, E. vallat-Sauvain and C. Ballif, 21st, European Photovoltaic Conference, Dresden, Germany, September 2006.

12. D. Levi, E. Iwaniczko, M. Page, Q. Wang, H. Branz and T. Wang, IEEE 4th world conference on Photovoltaic Energy Conversion, May 7-12, 2006.

13. H. Fujiwara and M. Kondo, Appl. Phys. Lett. Vol. 86, 032112, 2005.

14. S. Olibet, PhD thesis “Properties of interface in amorphous / crystalline silicon heterojunction”, Page 32-35, 2009.

9. High-density silicon nitride deposited at low substrate temperature with high deposition rate using hot wire chemical vapour deposition

V. Verlaan, R. Bakker, C.H.M. van der Werf, Z.S. Houweling, Y. Mai, J.K. Rath, R.E.I. Schropp. Surface & Coatings Technology **201**, 9285 (2007).

ELSEVIER

Available online at www.sciencedirect.com

ScienceDirect

Surface & Coatings Technology 201 (2007) 9285 – 9288

SURFACE & COATINGS TECHNOLOGY

www.elsevier.com/locate/surfcoat

High-density silicon nitride deposited at low substrate temperature with high deposition rate using hot wire chemical vapour deposition

V. Verlaan, R. Bakker *, C.H.M. van der Werf, Z.S. Houweling, Y. Mai, J.K. Rath, R.E.I. Schropp

Utrecht University, Faculty of Science, Department of Physics and Astronomy, SID-Physics of Devices, P.O. Box 80 000, NL-3508 TA Utrecht, The Netherlands

Available online 11 April 2007

Abstract

For application as barrier coatings in (opto-)electronic devices, it is important to deposit transparent silicon nitride (SiN_x) films with high mass density at low substrate temperatures. By using hot wire chemical vapour deposition (HWCVD) we were able to deposit transparent SiN_x coatings at temperatures below 230 °C. As determined with elastic recoil detection (ERD), these films have a density of 2.8 g/cm^3, which is only slightly lower than the density of 3.0 g/cm^3 obtained for samples deposited at 450 °C. The low 16BHF etch-rates of 18 nm/min and 7 nm/min, respectively, confirm the high compactness of the films. An interesting feature of these films is that the composition at which a maximum in mass density is obtained changes from slightly Si-rich towards stoichiometric when lowering the substrate temperature. The deposition rate of these high-density films is 3 nm/s. Moreover, these high-density films have very low absorption for the visible wavelength region, which enables the use in optical devices. Since this high transparency is obtained in combination with the high mass density and a high deposition rate (3 nm/s), we conclude that these HWCVD deposited SiN_x films have great potential for application in barrier coatings.

Keywords: Silicon nitride; Hot wire CVD; Low substrate temperature

10. Deposition of device quality silicon nitride with ultra high deposition rate (>7 nm/s) using hot-wire CVD

V. Verlaan, Z.S. Houweling, C.H.M. van der Werf, I.G. Romijn, A.W. Weeber, H.D. Goldbach, R.E.I. Schropp. Thin Solid Films **516**, 533 (2008).

Available online at www.sciencedirect.com
ScienceDirect
Thin Solid Films 516 (2008) 533–536

www.elsevier.com/locate/tsf

Deposition of device quality silicon nitride with ultra high deposition rate (>7 nm/s) using hot-wire CVD

V. Verlaan [a,*], Z.S. Houweling [a], C.H.M. van der Werf [a], I.G. Romijn [b], A.W. Weeber [b], H.D. Goldbach [a], R.E.I. Schropp [a]

[a] *Utrecht University, Faculty of Science, Department of Physics and Astronomy, SID-Physics of Devices, P.O. Box 80.000, 3508 TA Utrecht, The Netherlands*
[b] *ECN Solar Energy, P.O. Box 1. 1755 ZG Petten, The Netherlands*

Available online 18 June 2007

Abstract

The application of hot-wire (HW) CVD deposited silicon nitride (SiN_x) as passivating anti-reflection coating on multicrystalline silicon (mc-Si) solar cells is investigated. The highest efficiency reached is 15.7% for SiN_x layers with an N/Si ratio of 1.20 and a high mass density of 2.9 g/cm^3. These cell efficiencies are comparable to the reference cells with optimized plasma enhanced (PE) CVD SiN_x even though a very high deposition rate of 3 nm/s is used. Layer characterization showed that the N/Si ratio in the layers determines the structure of the deposited films. And since the volume concentration of Si-atoms in the deposited films is found to be independent of the N/Si ratio the structure of the films is determined by the quantity of incorporated nitrogen. It is found that the process pressure greatly enhances the efficiency of the ammonia decomposition, presumably caused by the higher partial pressure of atomic hydrogen. With this knowledge we increased the deposition rate to a very high 7 nm/s for device quality SiN_x films, much faster than commercial deposition techniques offer [S. von Aichberger, Photon Int. 3 (2004) 40].

Keywords: Silicon nitride; Hot-wire CVD; Multicrystalline solar cells; High deposition rate

11. Near-Infrared Quantum Cutting for Photovoltaics

Bryan M. van der Ende, Linda Aarts, and Andries Meijerink. Physical Chemistry Chemical Physics 11, 11081 (2009).

PERSPECTIVE www.rsc.org/pccp | Physical Chemistry Chemical Physics

Lanthanide ions as spectral converters for solar cells

Bryan M. van der Ende,*[ab] Linda Aarts[a] and Andries Meijerink*[a]

Received 10th July 2009, Accepted 19th August 2009
First published as an Advance Article on the web 10th September 2009
DOI: 10.1039/b913877c

The use of lanthanide ions to convert photons to different, more useful, wavelengths is well-known from a wide range of applications (*e.g.* fluorescent tubes, lasers, white light LEDs). Recently, a new potential application has emerged: the use of lanthanide ions for spectral conversion in solar cells. The main energy loss in the conversion of solar energy to electricity is related to the so-called spectral mismatch: low energy photons are not absorbed by a solar cell while high energy photons are not used efficiently. To reduce the spectral mismatch losses both upconversion and downconversion are viable options. In the case of upconversion two low energy infrared photons that cannot be absorbed by the solar cell, are added up to give one high energy photon that can be absorbed. In the case of downconversion one high energy photon is split into two lower energy photons that can both be absorbed by the solar cell. The rich and unique energy level structure arising from the $4f^n$ inner shell configuration of the trivalent lanthanide ions gives a variety of options for efficient up- and downconversion. In this perspective an overview will be given of recent work on photon management for solar cells. Three topics can be distinguished: (1) modelling of the potential impact of spectral conversion on the efficiency of solar cells; (2) research on up- and downconversion materials based on lanthanides; and (3) proof-of-principle experiments. Finally, an outlook will be given, including issues that need to be resolved before wide scale application of up- and downconversion materials can be anticipated.

12. Near-Infrared Quantum Cutting for Photovoltaics

Bryan M. van der Ende, Linda Aarts, and Andries Meijerink. Advanced Materials 21, 3073 (2009).

Near-Infrared Quantum Cutting for Photovoltaics

By *Bryan M. van der Ende, Linda Aarts,* and *Andries Meijerink**

13. Dowconversion for solar cells in NaYF4:Er, Yb

L. Aarts, B. M. van der Ende, and A. Meijerink, J. Appl. Phys. 106, 023522 (2009).

JOURNAL OF APPLIED PHYSICS **106**, 023522 (2009)

Downconversion for solar cells in $NaYF_4:Er,Yb$

L. Aarts,[a] B. M. van der Ende, and A. Meijerink
Condensed Matter and Interfaces, Debye Institute for Nanomaterials Science, Utrecht University, Princetonplein 5, 3584 CC Utrecht, The Netherlands

(Received 8 April 2009; accepted 19 June 2009; published online 24 July 2009)

Downconversion is a promising avenue to boost the efficiency of solar cells by absorbing *one* higher energy visible photon and emitting *two* lower energy near-infrared (NIR) photons. Here the efficiency of downconversion for the (Er^{3+}, Yb^{3+}) couple is investigated in $NaYF_4$, a well-known host lattice for efficient upconversion with (Er^{3+}, Yb^{3+}). Analysis of the excitation and emission spectra for $NaYF_4$ doped with 1% Er^{3+} and codoped with 0%, 5%, 10%, or 30% Yb^{3+} show that visible to NIR downconversion is inefficient. Downconversion by the scheme based on the reverse of the upconversion process is hampered by fast multiphonon relaxation from the $^4F_{7/2}$ level (the starting level for downconversion) to the $^4S_{3/2}$ level. Energy transfer from the $^4S_{3/2}$ level of Er^{3+} to Yb^{3+} is shown to be inefficient. Efficient downconversion from the $^4G_{11/2}$ of Er^{3+} level is observed, resulting in emission of two photons (one around 980 nm and one around 650 nm) after absorption of a single 380 nm photon. [DOI: 10.1063/1.3177257]

14. Downconversion for solar cells in YF_3:Nd^{3+}, Yb^{3+}

Janne-Mieke Meijer, Linda Aarts, Bryan M. van der Ende, Thijs J. H. Vlugt, and Andries Meijerink, Phys. Rev. B81, 035107 (2010)

PHYSICAL REVIEW B **81**, 035107 (2010)

Downconversion for solar cells in $YF_3:Nd^{3+}$, Yb^{3+}

Janne-Mieke Meijer,[1] Linda Aarts,[1] Bryan M. van der Ende,[1] Thijs J. H. Vlugt,[2] and Andries Meijerink[1,*]
[1]*Condensed Matter and Interfaces, Debye Institute for Nanomaterials Science, Utrecht University, Princetonplein 5, 3584 CC Utrecht, The Netherlands*
[2]*Process & Energy Laboratory, Delft University of Technology, Leeghwaterstraat 44, 2628 CA Delft, The Netherlands*
(Received 9 October 2009; published 12 January 2010)

Energy losses inherent to the conversion of sunlight to electricity in solar cells are mainly due to the so-called spectral mismatch: low energy photons are not absorbed while the energy of high energy photons is only partly used by the solar cell. The losses can be significantly reduced by adapting the solar spectrum. A promising avenue is the use of a downconversion material where *one* higher energy visible (blue-green) photon is "cut" into *two* lower-energy near-infrared photons that both can be used by the solar cell. Here the efficiency of downconversion for the (Nd^{3+},Yb^{3+}) couple in YF_3 is studied to investigate if efficient two-step energy transfer occurs from the $^4G_{9/2}$ level of Nd^{3+} (situated around 21 000 cm^{-1} or 470 nm) exciting two neighboring Yb^{3+} ions to the $^2F_{5/2}$ level (around 10 000 cm^{-1} or 1000 nm). Optical measurements of YF_3 doped with Nd^{3+} and Yb^{3+} show that there is efficient energy transfer from Nd^{3+} to Yb^{3+}, but downconversion from the $^4G_{9/2}$ level does not occur due to fast multiphonon relaxation. Relaxation from this level to lower-energy levels populates the $^4F_{3/2}$ level of Nd^{3+} from which efficient one-step energy transfer to Yb^{3+} occurs. Analysis of the luminescence decay curves for different Yb^{3+}-concentrations using Monte Carlo simulations reveals a high nearest neighbor transfer rate (3.3×10^5 s^{-1}) through a dipole-dipole interaction mechanism. Downconversion is observed from the $^4D_{3/2}$ level (situated in the UV, around 28 000 cm^{-1} or 360 nm) with an estimated quantum efficiency up to 140%. For application in solar cells this UV to 2 NIR downconversion will only result in a marginal reduction of spectral mismatch losses.

DOI: 10.1103/PhysRevB.81.035107 PACS number(s): 33.50.−j, 78.40.Ha, 78.47.−p, 78.55.Hx

15. Outlook

The proof of principle for back contact silicon heterojunction devices has been demonstrated. The potential for very high efficiency is demonstrated, based on a Voc of upto 695 mV and a design that should significantly reduce the optical losses compared to traditional SHJ cells. Proof of concept and proof of feasibility for industrial production will require a scaled-up effort on, among other aspects:
- analysis of the efficiency-limiting factors in the current back contact SHJ devices
- development of heterojunction deposition technology at the state-of-the-art (Sanyo) level
- test and development of process steps which allow low cost production

In this way, back contact SHJ devices offer the possibility of reaching 25% cell efficiency in the mid-future, higher than any other crystalline silicon technology presently known can be expected to deliver.

Also the proof of principle for photon multiplication by quantum cutting has been demonstrated. Follow-up research will have to work on sensitizers, in order to use more of the available UV spectrum, and on methods to incorporate the phosphors in cell design.
If this follow-up development is successful, quantum cutting can enhance the efficiency of crystalline silicon solar cells significantly beyond the fundamental limit of 25-26%.

A "public-private" consortium has been formed to address the remaining issues in the field of fully back-contacted silicon heterojunction solar cells and a Perspectief proposal (acronym Flash) has been submitted to STW.

The Stichting FOM is further pursuing the science and technology of photon manipulation (including photon conversion) in several projects in the Joint Solar Programme (see www.fom.nl).