Dual Transimpedance Amplifier for 43 Gbps applications

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A 3-stage dual TransImpedance Amplifier (TIA) on one 2x1.8 mm² GaAs chip with 0.2 μm pHEMT technology has been designed for fiberoptic communication applications. It uses cascode connected common source FETs in a Constant-K configuration. The operating frequency ranges from DC to 35 GHz. The TIA is designed for a diode capacitance of 120 fF. The equivalent input referred noise current is around 18 pA/√Hz for a gain of around 40 dBΩ or 6.5 dB. The matching at the output is better than 14 dB. Measured RF performance in combination with the small size makes it very suitable for WDM telecommunication systems. A comparison between simulations and measurements is also made.

INTRODUCTION

For the European communication infrastructure an increase in the number of optical wavelengths as well as an increase in data transfer per optical carrier is foreseen. To facilitate the latter there is a distinct need for 43 Gbps fiberoptic front-ends. In a fiberoptic front-end, the light is detected by a diode and converted into current. Since the diode is capacitive and the light is converted into current, it is important to have low input impedance for the amplifier, especially at high frequencies. These specifications translate into the need for a transimpedance amplifier.
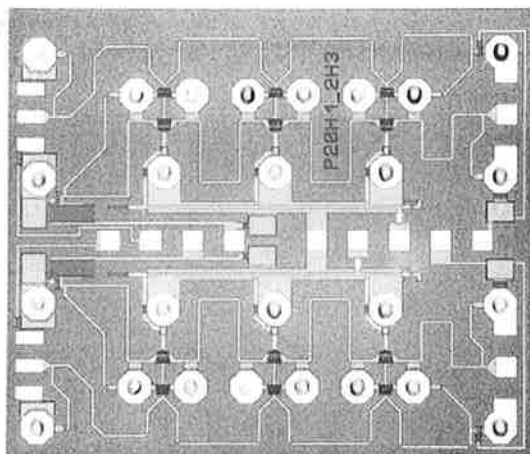

Figure 1: Chip photograph of the dual TIA (2×1.8 mm²).

The amplifier, as depicted in figure 1, has been designed to fit to a Wavelength Division (de)Multiplexer (WDM) with a diode spacing of 900 μm, limiting the width of the amplifier to 900 μm maximal (5), (6). Two dual TIAs side-to-side can be used if we want to facilitate more than two detector diodes. With the given width a scaling with respect to the number of diodes can be implemented (see figure 2).
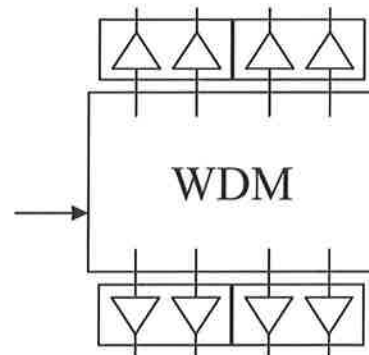

Figure 2: Block schematic of WDM with four dual TIAs.

DESIGN

The TIA was implemented as a GaAs MMIC with discrete diodes connected through bondwires. The process used is ED02AH from OMMIC. This process uses pHEMTs with a gate length of 0.2 μm. Three factors were limiting the practical bandwidth of the TIA.

The first factor was the inherent bandwidth of the TIA itself. By using a travelling wave amplifier (TWA) one can control the input-impedance of the TIA and the bandwidth of the TIA by scaling the FET sizes.

The second factor is the resonance of the diode-capacitance with the bondwire. This was solved using a small diode with a low capacitance and by reducing the length of the bond-wire used to connect the diode and the TIA to a minimum. The pad spacing and size have been adapted to match that of the diode, therefore bondwires can be made as small as possible.

A third factor is related to the input impedance of the TIA, which should be minimised as much as possible during design.

Since the bandwidth of the TIA can be chosen freely (within reasonable limits) the chosen bandwidth is set slightly higher than that of the diode bondwire combination. The bandwidth of 35 GHz is sufficient for 43 Gbps fiberoptic communication applications, since the required bandwidth is usually around 70% of the bitrate.

The diodes are biased via the amplifier, removing the need for off-chip bias tees.

The basic amplifier cells in the TWA are cascode connected Common Source (CS) FETs in constant-K configuration. The use of cascoded CS stages increases the isolation between gate and drain and therefore reduces the ripple on the S_{21}. The advantage of constant-K sections instead of constant-R sections is that the gain has no second order roll-off (2).

As can be seen in the simplified schematic the TWA utilises m-derived sections to improve the matching at the end of the band. Furthermore series connected inductance in the gate of the cascode FET is used to compensate loss (3), (4).
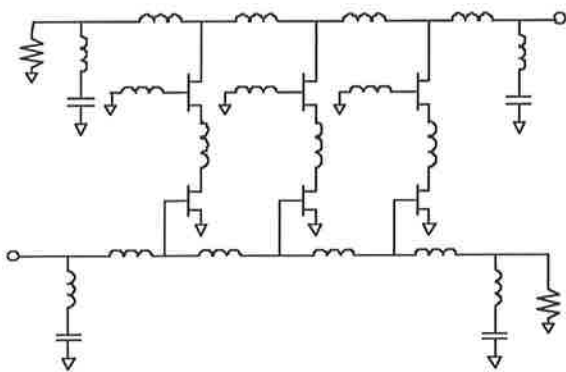

Figure 3: Simplified schematic of the TIA.

Due to constraints on the size of the TIA it is not possible to implement a TWA with a second tier such as in (1). A TWA with a second tier can realise a higher transimpedance

Measurements were performed on sample diodes at the start of the design. The diodes are the same as used in the WDM. A diode capacitance of 120 fF was measured. To show the effect of variation of the diode capacitance values of 80, 120 and 160 fF are used when the transimpedance is calculated.
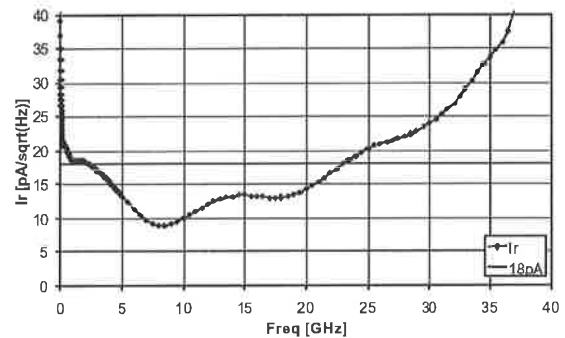

Figure 4: Simulated input referred equivalent noise current.

The simulated equivalent input referred noise current is around 18 pA/√Hz. Given the bandwidth of the TIA this is a rather good achievement.

MEASUREMENTS

Twenty-seven TIAs have been measured of which one device showed aberrant behaviour. The remainder of the devices has almost equal performance. The data shown is of such a normal device.

Figures 5 and 6 show the measured and simulated S_{21} and transimpedance. The transimpedance has been calculated from the measured S-parameter data for different diode capacitances. The measured S_{21} has a nice peak at the end of the band. The transimpedance, unfortunately, shows a dip of several dBs. The peak in the S_{21} nicely compensates for the roll-off due to the diode capacitance.

The in- and output matching shown in figure 7 and 8 is quite good. The S_{22} is below -10 dB up to 35 GHz.

From the measurement data the time response of the TIA for a single bit has been determined. The input is a 23 ps pulse filtered using a first order filter with the 3-dB point at 25 GHz. To calculate the Fourier transform Microsoft Excel is used. From figure 9 can be seen that there is a bit at the output of the TIA with little overshoot and the expected gain of slightly more than 100 times (40 dB). The delay is approximately 50 ps.

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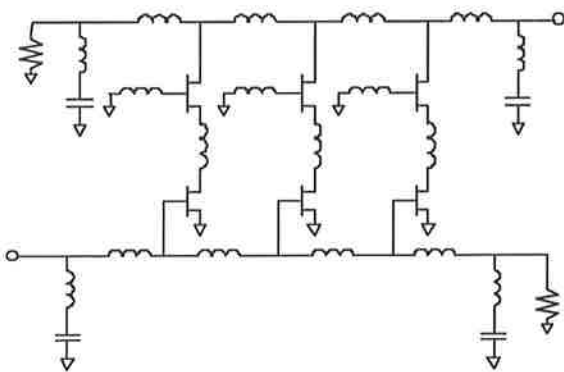

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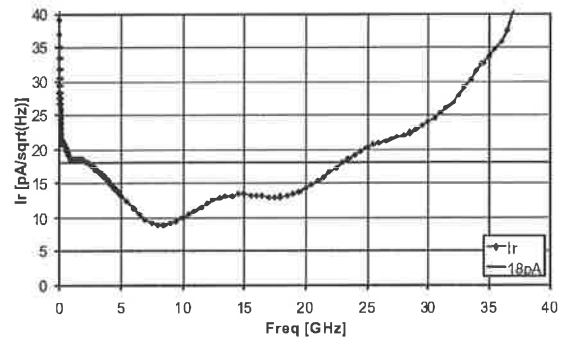

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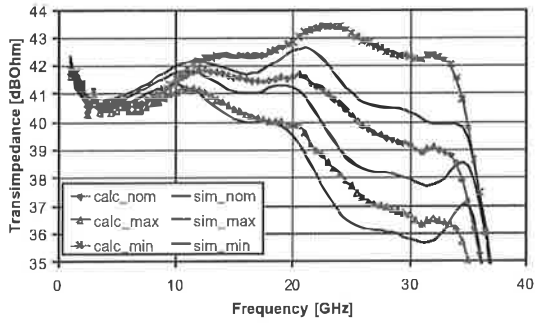
Figure 5: Calculated transimpedance for various diode capacitances with simulation- and measurement data.
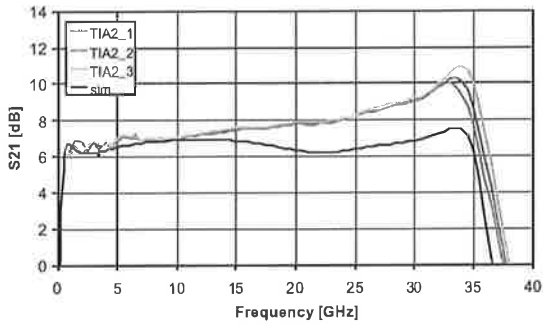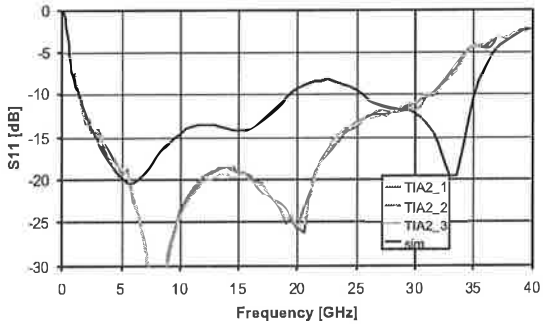

Figure 6: Simulated and measured S_{21}.

Figure 7: Simulated and measured input matching (S_{11}).
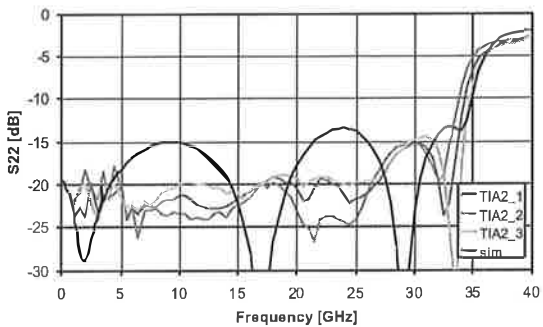

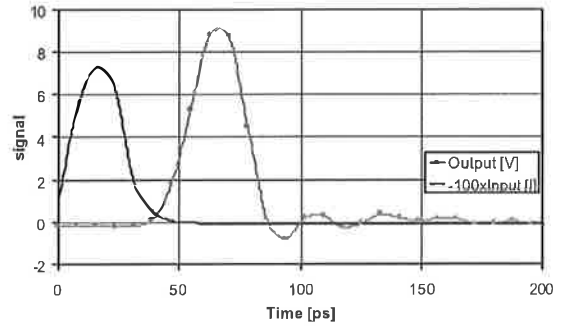*Figure 8: Simulated and measured output matching (S_{22}).*

Figure 9: Time-response calculated from measurement data.

The measured noise-figure shown in figure 10 is only slightly higher than the simulated noise-figure (3.8 vs. 3.4 dB at 15 GHz). Indicating that the actual equivalent input referred noise current for a diode as source is in agreement with the simulations.

Noise-figure measurements have only been done from 2 to 20 GHz due to limitations of the available equipment.

Figure 10: Simulated and measured noise-figure.

The measured average current consumption is 25 mA. The nominal applied drain voltage is 6 V.

CONCLUSION

A 43 Gbps TIA with low input referred equivalent noise current, on-chip support of diode biasing and having a bandwidth of 35 GHz is designed and measured. These characteristics, combined with the very small area per TIA of 0.9×2 mm², make the TIA very well suited for 43 Gbps fiberoptic communication applications.

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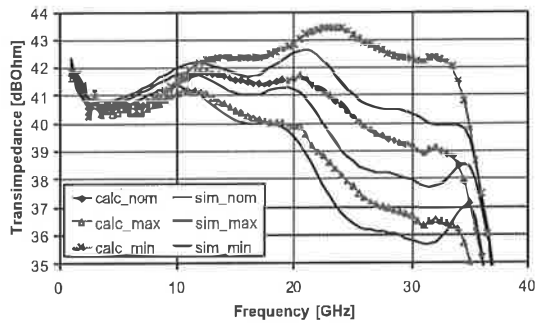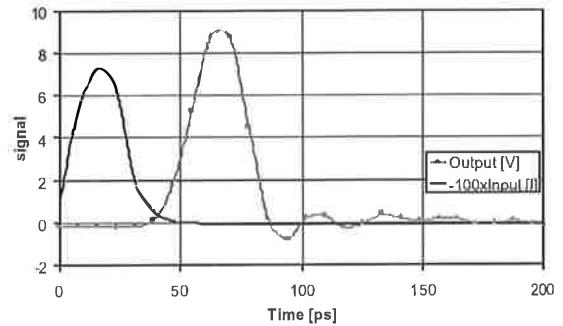Figure 5: Calculated transimpedance for various diode capacitances with simulation- and measurement data.
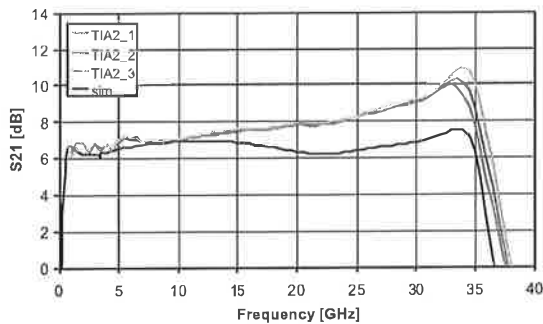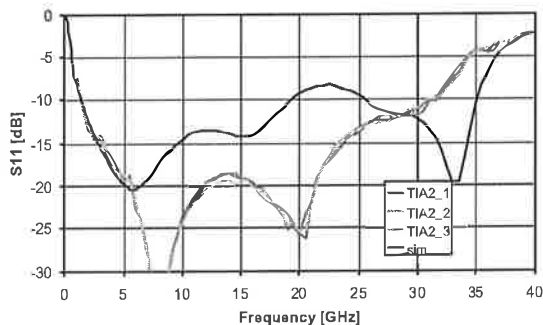

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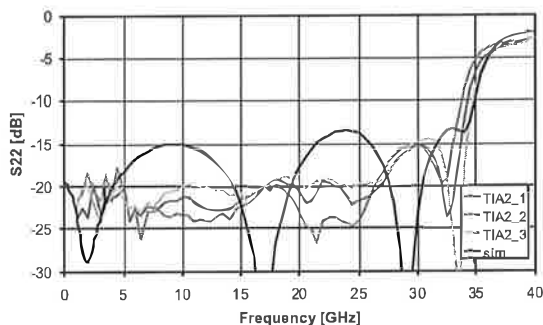Figure 8: Simulated and measured output matching (S_{22}).

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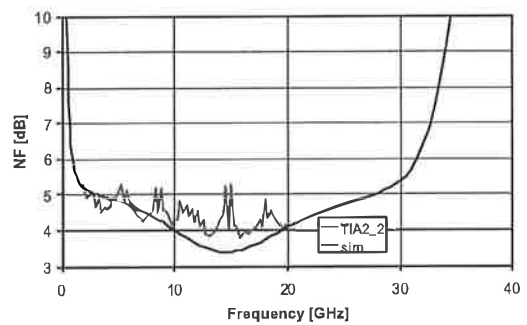Noise-figure measurements have only been done from 2 to 20 GHz due to limitations of the available equipment.

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