On-chip active gate bias circuit for MMIC amplifier applications with 100% threshold voltage variation compensation

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***Abstract* — In this paper the design and performance of an on-chip active gate bias circuit for application in MMIC amplifiers, which gives 100% compensation for threshold variation and at the same time is insensitive to supply voltage variations, is discussed. Design equations have been given. In addition, the boundary condition to make the circuit insensitive to supply voltage variations is given. The obtained measurement results demonstrate an excellent agreement with the simulation results.**

***Index Terms*— Voltage control, MMICs, FET circuits.**

I. Introduction

An increasing number of systems, ranging from mobile communication to radar, starts to exist that make use of MMICs for Transmit and Receive modules. It is essential to reduce the costs as much as possible to make such systems economically attractive. Therefore, the component count and the price of the used components needs to decrease. A way to improve both the yield and at the same time reduce the externally needed components is the use of an on-chip active gate bias circuit. The most important factor, which determines the yield of an amplifier, is the threshold voltage of the used transistors. An example of the effect of threshold variations on the drain current of a two-stage power amplifier is shown in figure 1. For this example, the gate voltage was kept at its nominal value. The depicted results clearly show the necessity to compensate for the effect of threshold voltage variation.

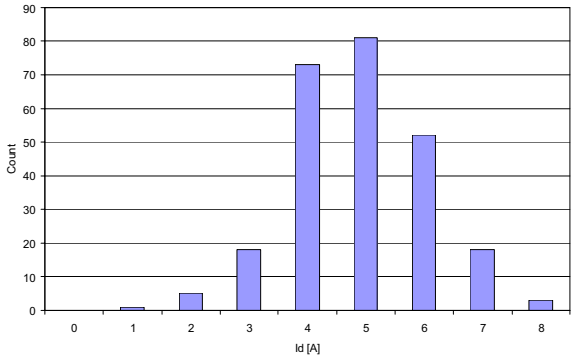

Fig. 1. Effect threshold variations on drain current amplifier (normal distribution with a standard deviation of 0.1 V).

In the next sections, the design and performance of active gate bias circuits will be discussed. As first step, the basic operating principle will be discussed in section II. In section III the design equations and results of the active gate bias circuit with 100% compensation of threshold voltage variation are given. Finally, in section IV the obtained measurement results are compared to the simulation results.

II. Active gate bias circuit principles

Requirements for the active gate bias circuit are besides setting of the correct gate voltage, compensation of threshold voltage variations and independency of supply voltage variations. The basic assumption made for the equations used for the design of the discussed gate bias circuit is that the I-V curves can be linearised as is depicted in figure 2. In this figure, also an often used building block for an active gate bias circuit is shown.

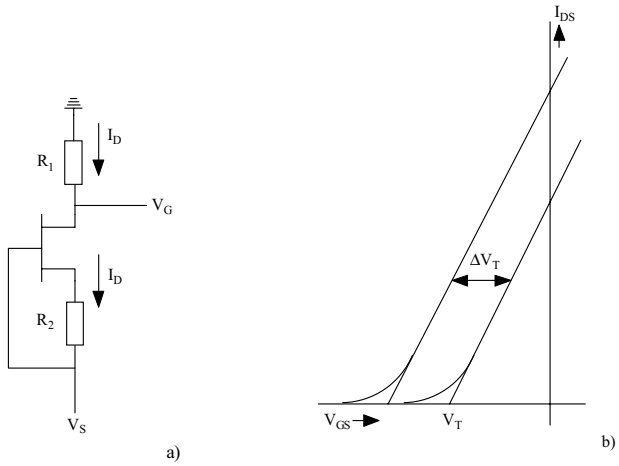

Fig. 2. Basis active gate bias circuit a) and linearised I-V curves b).

It is assumed that threshold variations only will result in a horizontal shift of the depicted I-V curves. The linearised I-V curve can be described with the following equation:

$$I_D = K_m \cdot (1 + \lambda \cdot V_{DS}) \cdot (V_{GS} - V_T) = g_m \cdot (V_{GS} - V_T) \quad (1)$$

In this equation V_T is a measure for the linearised threshold voltage of the transistor. At the same time g_m is a measure for the transconductance of the transistor. The

given equation closely resembles, in the saturated region, the one given by Curtice [1]. The indicated dependency of the drain-source voltage will be treated in the next section. For the moment a fixed drain-source voltage is assumed. For the gate bias schematic depicted in figure 2a the following equation for the gate voltage can be derived.

$$V_G = \frac{g_m \cdot R_1}{1 + g_m \cdot R_2} \cdot V_T \tag{2}$$

The equation suggests that the realized gate voltage in principle is independent of the negative supply voltage V_S. The feedback resistance R_2 can be used to reduce the sensitive of the bias circuit for transconductance and resistance variations. The variation of the gate voltage can be directly related to the variation of the threshold voltage.

$$\frac{\Delta V_G}{\Delta V_T} = \frac{g_m \cdot R_1}{1 + g_m \cdot R_2} = \frac{V_G}{V_T} \tag{3}$$

In general the absolute value of the required gate voltage V_G (e.g. -0.5 V) is smaller than the linearised threshold voltage V_T (e.g. -0.8 V). Therefore, 100% threshold voltage compensation is not possible. In the next section a gate bias circuit is discussed, which gives a 100% compensation of the threshold voltage variations and at the same time is insensitive to supply voltage variations.

III. Active gate bias with 100% compensation

To be able to set the gate voltage to its desired value and at the same time compensate the threshold voltage variation for 100% one could add an additional ideal current source in the circuit. Such a current source can be approximated by a resistor, which is connected between the drain and a positive supply voltage. A disadvantage of this approach is the additionally required bias supply and the associated sensitivity to positive supply voltage variations. To circumvent this problem, the solution shown in figure 3 has been developed. The threshold voltage compensation is realized with an additional resistor R_3, which is connected to the source of the transistor as is depicted in figure 3. Resistor R_3 makes it possible to set the required gate voltage independently from the threshold voltage compensation. In figure 3b the equivalent schematic is shown. The gate voltage can be described as follows:

$$V_G = \frac{g_m \cdot R_1}{1 + g_m \cdot R_q} \cdot \left(V_T + V_q\right) \tag{4}$$

The following requirement for 100% threshold voltage compensation can be derived.

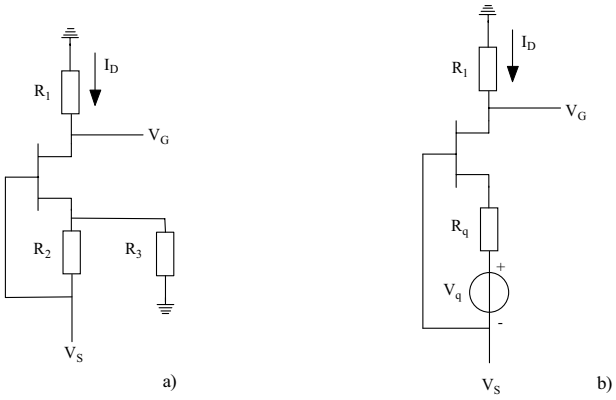

Fig. 3. Active gate bias circuit with 100% threshold compensation a) and equivalent schematic b).

$$\frac{\Delta V_G}{\Delta V_T} = \frac{g_m \cdot R_1}{1 + g_m \cdot R_q} = 1 \tag{5}$$

The equation shows that for a given process (V_T) the gate voltage can then be set with the appropriate setting of an equivalent voltage source V_q and an equivalent source resistor R_q, which in turn are determined by R_2 and R_3 and the negative supply voltage V_S. The value of V_q and R_q can be calculated with the following equations:

$$R_q = \frac{R_2 \cdot R_3}{R_2 + R_3} \tag{6}$$

$$V_q = -\frac{R_2}{R_2 + R_3} \cdot V_S \tag{7}$$

The gate voltage will vary as function of the negative supply voltage as is shown by equations 4 and 7. By selecting an appropriate gate voltage for the current source used in the bias circuit the effect of supply voltages variations can be eliminated as is shown in the following approximated equation (accuracy is better than 10%) for the output voltage of the bias circuit:

$$V_G \approx \frac{K_m \cdot R_1}{1 + K_m \cdot R_q} \cdot \left(V_T + V_q\right) \cdot \left(1 + \lambda \cdot \frac{R_3}{R_2} \cdot V_q\right) \tag{8}$$

This equation shows that when V_q is increased because the supply voltage has become more negative the factor V_T+V_q is becoming smaller. However, at the same time the last part of the equation is increased and under specific conditions the output voltage becomes independent of the supply voltage. The following equation gives the requirement for insensitivity to supply voltage variations:

$$\lambda \approx \frac{-1}{V_T + 2 \cdot V_q} \cdot \frac{R_2}{R_3} \tag{9}$$

The value of λ is technology and gate-source voltage dependent. This means that by proper selection of R_2 the right gate voltage and corresponding λ can be selected so

that at least the sensitivity to supply voltage variations is reduced.

In figure 4 the simulation results of a designed gate bias circuit are shown as function of the threshold voltage and the negative supply voltage variation.

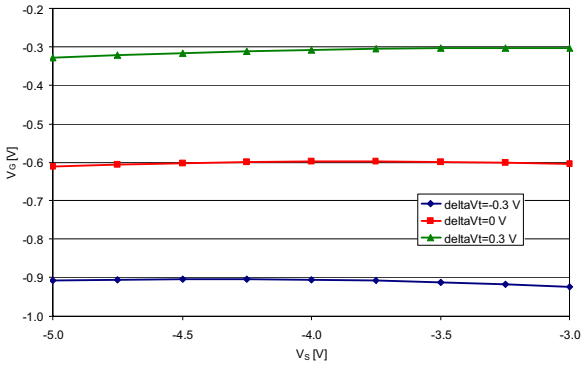

Fig. 4. Simulated performance of a fully compensating gate bias circuit as function of threshold variations and negative supply voltage variations (designed for V_G=-0.6 V at V_S=-4 V).

The depicted results demonstrate that the circuit hardly shows any sensitivity to supply voltage variations for a nominal supply voltage of -4 V and that an as good as 100% compensation for threshold voltage variations has been obtained. This compensation becomes less ideal when variations in the negative supply voltage V_S of more than 20% are present. Nevertheless, the performance is also in that case still excellent even with ±0.3 V threshold voltage variation.

IV. MESUREMENT RESULTS

The dicussed bias circuit is realised in the PH25 process of UMS. In figure 5 a picture of a few realized bias circuits is shown.

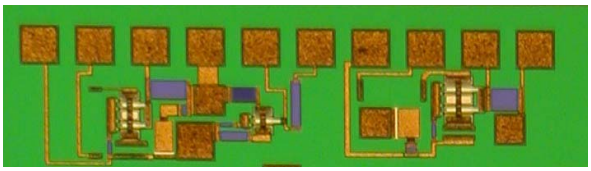

Fig. 5. Photograph of the realised gate bias circuits.

The output voltage of the realised gate bias circuit has been measured for 400 samples coming from two different wafers. In table 1 a comparison is listed between the deviations of the average value and standard deviation of the PCM transistor threshold voltage and the output voltage of the gate bias circuit compared to their nominal value. The obtained numbers show that for the average value, the difference between the nominally expected value and the measured value is small. The results also show an increase of the threshold voltage for both the PCM transistor and the gate bias circuit. A gate bias voltage correction of 90% of its threshold voltage variation has been obtained. In addition, the standard deviations are in good agreement proving that the transistor in the gate bias circuit is the major process related parameter.

Table 1: Measured deviations from the nominal performance for the PCM transistor and the bias circuit.

Wafer	PCM transistor		Bias circuit	
	Average	Stand. Dev	Average	Stand. Dev
1	0.098	0.013	0.086	0.015
2	0.110	0.015	0.100	0.019

In figure 6, the measured and simulated sensitivity to supply voltages changes is shown. The depicted results show a good correlation between the measured variation of supply voltages and the simulation result.

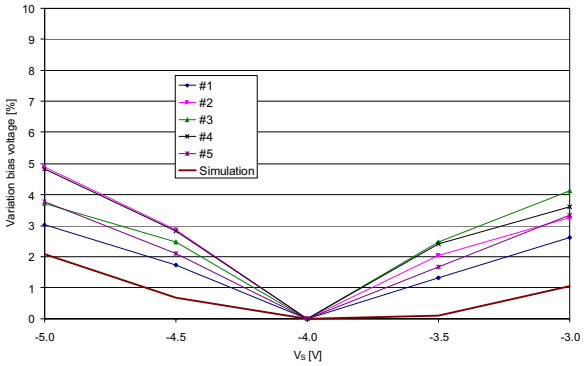

Fig. 6. Measured and simulated gate voltage variation as function of the supply voltage compared to the gate voltage at V_S=-4 V.

Temperature variations will influence the performance of the discussed bias circuit. The way the generated gate voltage should change as function of temperature depends on the application. For linear amplifiers, some degree of temperature pre-correction can be desired, in conjunction with the proposed 100% threshold voltage correction method. As an amplifier heats up, its gain decreases. Please note that temperature compensation is only applicable when the bias voltage of the amplifier lies in a region, in which the gain increases with increasing gate voltage, see figure 7.

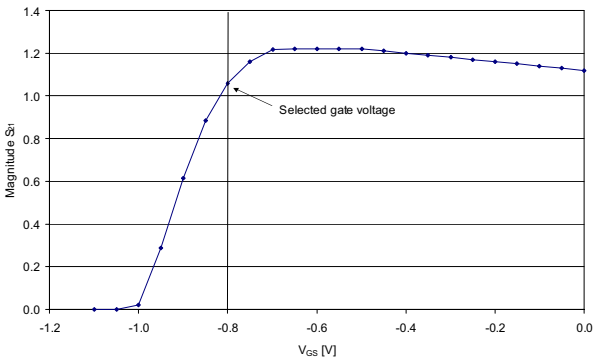

Fig. 7. Gain as function of gate voltage.

In other applications, it may be required not to have such correction. The circuit proposed in this paper can be made suitable to address both situations. Deliberate temperature variation, meant for pre-compensation, is introduced by using a relatively temperature independent resistor for R_1. As temperature rises, carrier mobility is decreased for majority carriers, due to lattice vibrations in

the active InP region, in both the FET and resistor R_2. Consequently, both the change in the FET and R_2 lead to a lower current. Therefore, the bias circuit generates a higher V_G at higher temperatures. The pre-correction effect is aggravated when for R_3 a resistor with negative temperature coefficient is used. Figure 8 shows this temperature effect on a bias circuit designed for a V_G = -0.255V at 10 ºC.

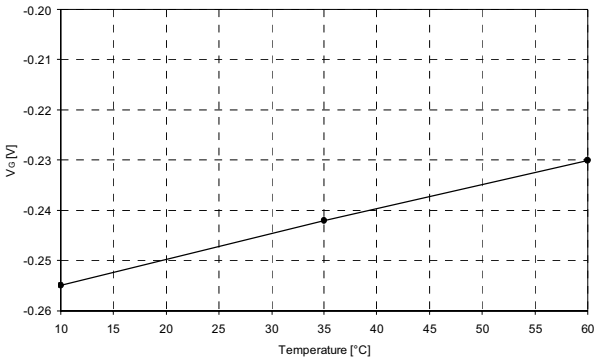

Fig. 8. Temperature pre-correction example.

When no temperature pre-correction is desired, a GaAs resistor can be used for R_1, the resulting change over temperature is negligible.

Resistor spread is noticeable and possibly already an issue with the basic circuit of Fig. 2. The effect of resistor spread on the proposed circuit is similar, only the additional resistor R_3 gives an extra uncertainty. Considering the value of the resistor, in the order of 1000 Ω, the size may become an issue unless materials can be used with a higher surface resistance, as TiWSi Unfortunately this material is quite subject to spread. Nevertheless, only some small additional spread is introduced by R_3. For example, with V_G = -0.5 V, K = 0.01 A/V, λ = 0.2, V_T = -0.8 V, R_1 = 100 Ω, R_2 = 55 Ω, R_3 = 1000 Ω, V_S = -4 V, a 20% variation of R_3 leads to an acceptable 2.6 % extra variation on V_G.

V. Conclusion

In this paper it is demonstrated that the use of an on-chip active gate bias circuit is essential to keep the circuit performance within acceptable limits. The design equations for an active gate bias circuit are discussed. It is demonstrated that it is possible to have a 100% compensation of threshold variations and still have a gate voltage that is insensitive to treshold voltage and supply voltage variations.

Remark

For the gate bias circuits discussed in this article, patents are pending.

References

[1] W.R. Curtice, "A MESFET model for Use in the Design of GaAs Integrated Circuits", IEEE Trans. Microwave Theory Tech., Vol. MTT-28, pp. 448-456, 1980.