Low-cost S-band Multi-function MMIC

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***Abstract*— This paper discusses the design and performance of a four port S-band multi-function MMIC. The multi-function chip consist of a 6-bit phase shifter, 6-bit attenuator, transmit receive switches, a low noise amplifier, a medium power amplifier and integrated LVCMOS control logic. It is shown that excellent results have been obtained for the presented multi-function chip which has been realised in the low cost high volume PP50-11 0.5 µm PHEMT process of WIN Semiconductors.**

I. INTRODUCTION

Internationally there is a trend towards the development of phased array radar systems, which combine both search and tracking capabilities in one radar system. S-band is the preferred choice as frequency band for such systems. Phased array radar systems can consist of several thousands of modules. Therefore, it is essential to reduce the costs of these modules as much as possible to make such systems economically attractive. The component count and the price of the used components need to decrease. This can be achieved through integration of the necessary functionality for beam steering and the low-noise and driver amplifiers necessary for transmit and receive onto a single multi-function MMIC.

The presented S-band multi-function chip is to the author's knowledge the first low-cost solution which is also commercially available. In addition, as far as we know the results of only one prototype S-band multi-function chip have been published [1]. Our multi-function chip has a greatly improved frequency band, gain, noise figure, attenuation and phase shifter accuracy when compared to the results presented in [1].

In the next sections, the design, layout and measurement results of the S-band multi-function chip will be discussed. As first step, the design will be discussed in section II. In section III an overview of the layout is given. Finally, in section IV the obtained measurement results are compared to the simulation results.

II. DESIGN MULTI-FUNCTION MMIC

For the multi-function chip a four port topology was selected, see figure 1. This topology was selected to have the maximum flexibility for the use of the chip in various applications ranging from phased array radar to telecommunication and instrumentation applications.

The multi-function chip consists of an SPDT switch at its input and output. A 2-stage low-noise amplifier at the input and a driver amplifier at the output of the chip are used. In between the amplifiers a 6-bits phase shifter and a 6-bit attenuator have been placed.

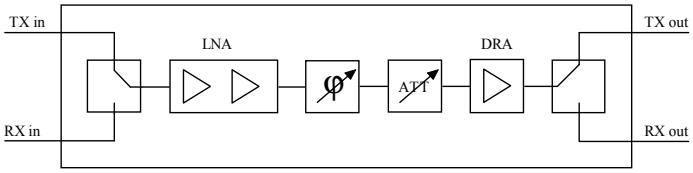

Fig. 1 Block diagram of the multi-function chip

An essential step in every chip design is the choice of the technology in which the chip will be realised. Factors that play a role in the technology selection are cost, yield, power performance and low noise performance. For the multi-function chip the PP50-11 process of WIN Semiconductors has been selected. This is a 0.5 µm PHEMT process, which is fabricated on 6" wafers. This process in our experience is very repeatable and has a high yield for relatively large MMICs (> 25 mm^2). Therefore this technology is very suited for the development of complex low-cost MMICs. A major advantage of the selected technology for the current application is the high gate-source breakdown voltage of more than 10 V. This high breakdown voltage allows for the selection of an off-voltage for the switches of -5 V which greatly enhances the compression level of the switch FETs used in the SPDT switches, phase shifter and attenuator. Since the selected technology is a power technology the noise figure is higher than can be achieved with other technologies. Nevertheless it is the authors believe that this minor disadvantage is more than compensated for by the high power performance of this technology, which improves the multi-chip performance for all other specifications. In addition, it should be realised that it is difficult to realise noise figures below 1 dB with multi-function chips as the one discussed. Therefore, for really low noise figures always a low-noise amplifier in front of the multi-function chip need to be used. In the remainder of this section the design of the individual building blocks will be discussed.

A. Single Pole Double Throw switches

The topology depicted in figure 2 is used for the SPDT switches. In each branch one series switch and two parallel switches are used. In the on-state the series switch is turned on

and the parallel switches are turned off. In the parallel branch the transistors are switched the other way around to improve the isolation as much as possible.

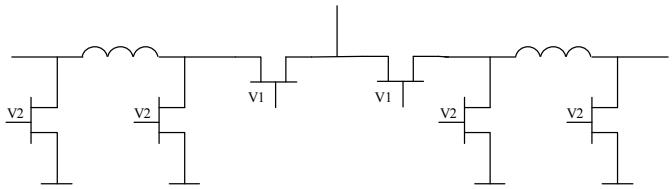

Fig. 2 Topology SPDT switch

The used -5 V in the off-state enables a high compression level of the switches. As a result no transistors need to be stacked to achieve the desired compression level of more than 25 dBm. In the on-state 0 V is used. This results in a low loss in the series switches. The depicted switch has a loss of better than 0.6 dB and an isolation of better than 50 dB. The inductors in between the parallel switches form an artificial 50 Ω transmission line. With the help of this line a matching of better than 25 dB has been achieved. The common input has a matching of better than 22 dB.

B. Amplifier design

For the multi-function chip an overall gain of more than 20 dB was specified. It turns out that three amplifier stages are needed to realise this gain.

To keep the noise figure as low as possible it was decided to design a two-stage noise amplifier (LNA), which is put directly after the SPDT switch. The targeted noise figure for the multi-function-chip is smaller than 2.5 dB. This number can be achieved when a two-stage LNA is placed inside the common leg. An alternative could have been placing the LNA in front of the SPDT switch. In this way the noise figure is further reduced with the loss of the switch. A disadvantage of this approach is that also for transmit additional gain either at the input or at the output of the chip need to be added. This results in an increased chip layout and the DC dissipation of the multi-function chip is unnecessarily increased with the dissipation of the added amplifier stage(s).

The LNA is classical in the sense that the first stage is realised with a transistor, which has an additional source inductance for optimal noise matching. In the second stage a feedback amplifier is used to make the output of the amplifier as good as possible 50 Ω. In this way a matching of better than 15 dB has been achieved. The LNA has a gain of 26 dB and a noise figure of 1.5 dB

As driver amplifier a one-stage feedback amplifier has been designed. Feedback has been used to flatten the gain as much as possible over the specified frequency band. A gain of 12 dB with a matching better than 15 dB has been realised. The one dB compression level of this amplifier is 16.5 dBm.

Both amplifiers are biased at a drain voltage of 5 V and a gate voltage of -0.95 V. The gate voltage has been realised with a gate bias circuit, which gives a 100% compensation for threshold variations [2].

The necessary DC dissipation at the one dB compression point is 475 mW for the LNA, 300 mW for the driver amplifier and 80 mW for the gate bias circuit.

C. 6-bit phase shifter design

The design of the 6-bit phase shifter is discussed in [3]. The smallest phase step is 5.625°. In between the phase shifter and the attenuator no buffer amplifier for the minimisation of the effect of the load and source variations between the different states has been placed. It turns out that the matching of both phase shifter and attenuator is so good that no significant impact is seen when they are connected directly together. A matching of better than 15 dB, an RMS phase error of less than 2° and an amplitude variation of less than 1 dB have been achieved.

D. 6-bit attenuator design

A 6 bit attenuator is designed for the multi-function chip. The smallest attenuation step is 0.45 dB and the largest is 14.4 dB. The desired attenuation is realized by switching between a through connection and an attenuator, see figure 3.

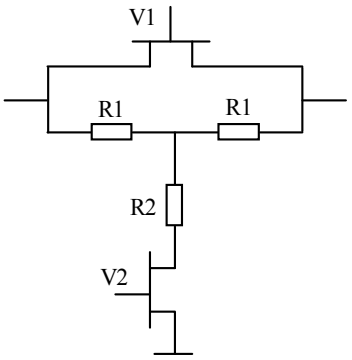

Fig. 3 Topology attenuator bits

For all attenuator bits a T section is used except for the 7.2 dB bit where a pi-section was used. To improve the matching for all bits except for the 0.45 dB and 0.9 dB bit resistor R2 is switched on and off with an additional transistor.

In simulation a matching of better than 15 dB and an RMS amplitude error of less than 0.2 dB and maximum phase error of better than 2.5° has been realised.

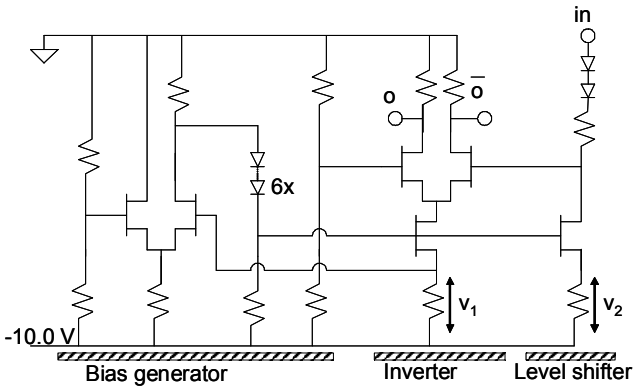

Fig. 4 Schematic of LVCMOS compatible level shifter inverter

E. *LVCMOS control logic*

The switch voltages are generated with the LVCMOS compatible level shifter inverter depicted in figure 4. The design of this control logic is discussed in detail in [4]. For the current design the off-voltage has been lowered from -3 to -5 V. For a proper working the supply voltage of this circuit had to be changed to -10 V.

III. LAYOUT

In this section the layout of the multi-function chip will be discussed. The used PP50-11 process has the following features 0.5 µm depletion mode power PHEMT transistors, TaN and GaAs resistors, MIM capacitors and viaholes through 100 µm thick substrates.

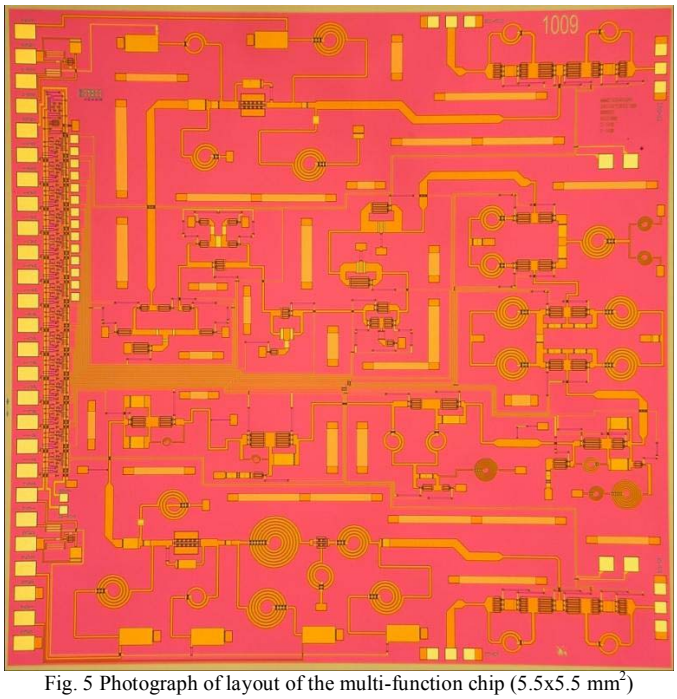

Fig. 5 Photograph of layout of the multi-function chip (5.5x5.5 mm^2)

A photograph of the realised multi-function chip has been depicted in figure 5. The control logic is visible along the left edge of the chip. The SPDT switches are located at the right bottom and upper corner. The LNA and the 6-bit phase shifter are visible at the bottom of the chip. The 6-bit attenuator is visible at the top of the chip. Between all vital parts of the multi-function chip screens consisting of metal lines with viaholes are placed. These screens help too improve the isolation between the various parts of the multi-function chip.

IV. MEASUREMENT RESULTS

The multi-function chip input matching and the small-signal gain are depicted in respectively figure 6 and 7. All measurement results have been obtained at an ambient temperature of 25 °C in the reference state of the attenuator and phase shifter. The depicted results show a good agreement between the measured and simulated performance. The RMS phase error is depicted in figure 8. Again an excellent agreement between simulation and measurement results has been obtained.

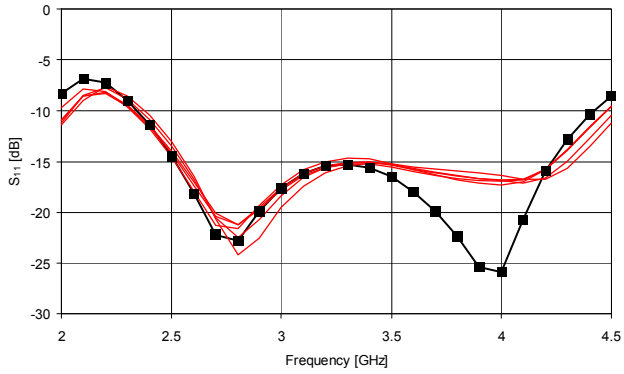

Fig. 6 Input matching multi-function chip in reference state (simulation black squares)

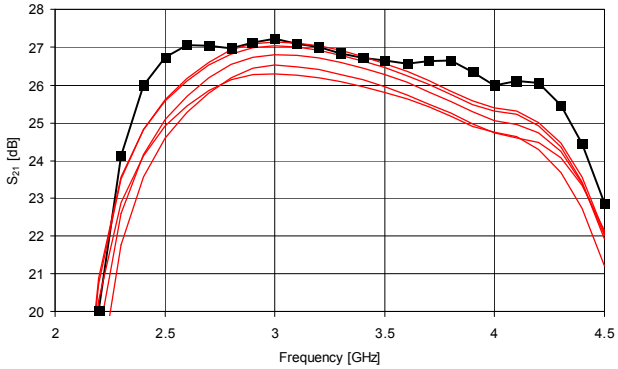

Fig. 7 Gain multi-function chip in reference state (simulation black squares)

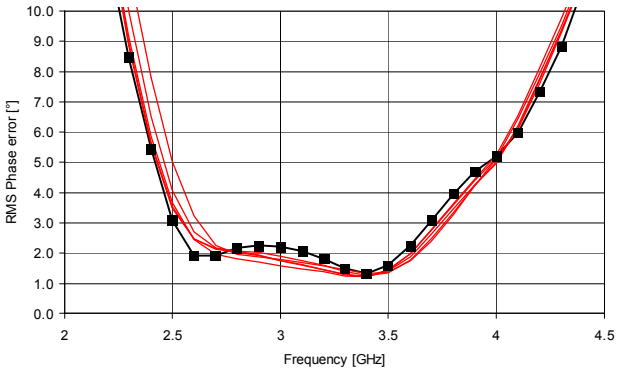

Fig. 8 RMS phase error multi-function chip (simulation black squares)

The RMS attenuation error is depicted in figure 9. The measurement results show that for the 3 – 4.5 GHz frequency band an RMS attenuation error of better than 0.2 dB has been obtained. Between 2.5 – 3 GHz the attenuation error is higher than simulated. Nevertheless an attenuation error smaller than 0.4 dB has been measured over mentioned frequency band. The measured noise figure is depicted in figure 10. The depicted results show that between 2.5 – 4 GHz a noise figure of approximately 3.5 dB has been measured. The measured

noise figure is 1.5 dB higher than expected on the basis of simulations.

The measured output power at a fixed input power of -10 dBm is depicted in figure 11. Again an excellent agreement between measurement and simulation results can be observed. The used input power will result in a compression level of approximately 2 dB. At this compression level an output power between 14 and 15 dBm has been measured.

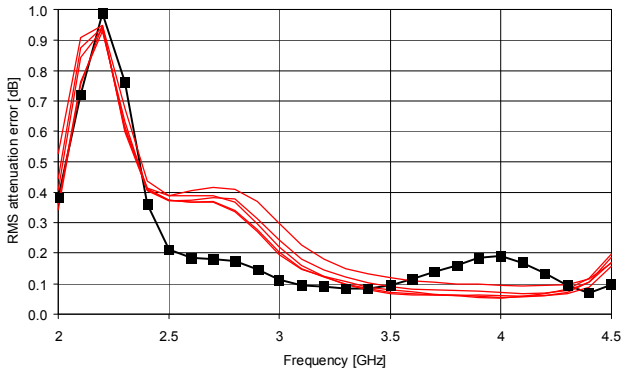

Fig. 9 RMS attenuation error multi-function chip (simulation black squares)

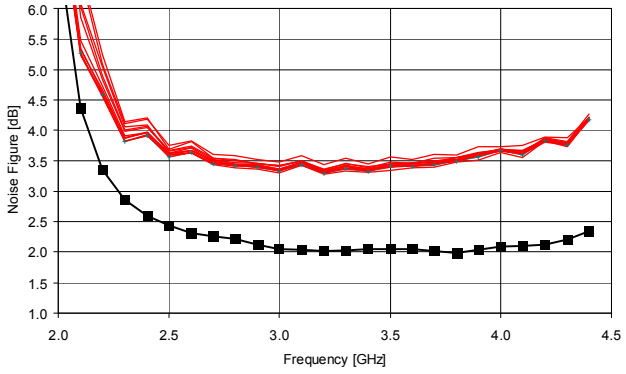

Fig. 10 Noise Figure multi-function-chip in reference state (simulation black squares)

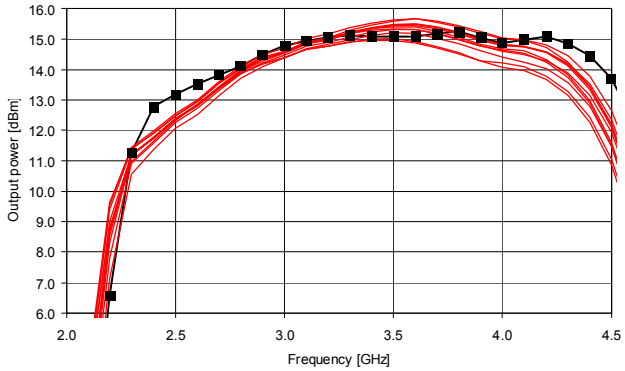

Fig. 11 Measured output power multi-function chip in reference state at an input power of -10 dBm (simulation black squares)

V. Conclusions

In this paper the design and measurement results of an S-band multi-function MMIC are discussed. An excellent agreement between measurement and simulations is demonstrated. The multi-function MMIC is realised in the low-cost high volume PP50-11 process of WIN Semiconductors. The obtained measurement results at 25 °C are summarized in table 1.

TABLE I
PERFORMANCE S-BAND MULTI-FUNCTION CHIP

	Measurement
Frequency [GHz]	2.8 - 3.5
Gain reference state [dB]	26.5 ± 0.5
Matching [dB]	< -13
Noise Figure [dB]	< 3.6
Phase control	360°/6-bit
RMS Phase error [°]	< 2.5
Attenuation control	28.35 dB/6-bit
RMS attenuation error [dB]	< 0.45
Pout-1dB [dBm]	> 13
Chip size [mm^2]	5.5 x 5.5

References

[1] N. Billström, H. Berg, K. Gabrielson, E. Hemmendorff, M. Herz, "T/R "core-chips" for S-, C- and X-band radar systems", European Microwave Conference Proceedings, October 2004.

[2] A.P. de Hek and E.B. Busking, "On-chip active gate bias circuit for MMIC amplifier applications with 100% threshold voltage variation compensation", Eumic conference proceedings, September 2006.

[3] A.P. de Hek, M. Rodenburg and F.E. van Vliet, "A Cost-effective High-Power S-band 6-bit Phase Shifter with Integrated LVCMOS Control Logic", Eumic conference proceedings, October 2007.

[4] M. van Wanum, G. van der Bent, M. Rodenburg, A.P. de Hek, "Generic robust LVCMOS compatible control logic for GaAs HEMT switches", Eumic conference proceedings, September 2006.