Sensing platform based on micro-ring resonator and on-chip reference sensors in SOI

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ABSTRACT

This article presents work on a Silicon-On-Insulator (SOI) compact sensing platform based on Micro Ring Resonators (MRRs). In order to enable correction for variations in environmental conditions (temperature, mechanical stress etc), a study has been performed on the performance of uncoated sensing MRRs, and of SU8- and SiO_2-covered reference MRRs. Excellent shielding for both cover materials has been obtained, however, water permeation into the SU8 causes a slow drift in sensor response. We believe that a user-friendly, low-cost and robust way for optical interfacing to MRR sensor chips is required for practical application in Point-Of-Care diagnostics, and that the cost and complexity of optical-electrical read-out systems must decrease. We have taken first steps to realize that vision, by building a prototype free-space optical coupling set-up, which enables non-photonic experts to characterize surface activation processes using MRRs. Moreover, we present our first steps towards on-chip read-out systems.

Keywords: Micro ring resonators, biosensing on chip, free space coupling, SU8, temperature compensation.

1. INTRODUCTION

Highly sensitive and cost-effective biosensors which are able to do monitoring in real-time are required in many applications such as disposable Point-Of-Care, control of industrial processes and in food industry [1]. Among the various technologies available based on integrated optics such as those based on interferometry , gratings, photonic crystals, nano opto mechanical devices etc, sensors based on micro ring resonators in SOI have specific advantages such as ease in design and fabrication, ability to multiplex, cost effectiveness, smaller foot print and high sensitivity [1].

The detection principle in a MRR is based on evanescent field sensing where the interaction of a gas/ bio molecule changes the effective refractive index of the guided mode propagating in the ring waveguide, causing a shift in comb of resonance wavelengths. However, the MRRs are also sensitive to unwanted variation in environmental conditions such as temperature and mechanical stress. Hence, to enable high sensitivity, the effect on MRRs by these environmental conditions needs to be monitored and cancelled out. An effective method for this is to incorporate additional on-chip reference sensors which can monitor unwanted changes in the sensing ring's environment. This can be achieved by having two MRRs fabricated on the same chip adjacent to each other. The uncovered ring (referred to as sensing ring) measures the desired evanescent field interaction, as well as any unwanted shifts due to temperature and mechanical stress. The other ring, referred to as reference ring, is covered by a coating layer, and measures the same unwanted shifts, but not the evanescent field interaction. By comparing the two, the shift due to evanescent field interaction can be extracted. Recently [2] has reported the use of SiO_2 and SU8 as effective covering materials for SOI based MRRs. They have demonstrated SiO_2 to be excellent shielding capabilities. SU8 on the other hand requires simple processing steps, but has the drawback of slow water permeation into the layer. In this work we look further into the possibilities of using these two materials as covering layers for reference sensors towards the realization of an photonic bio/gas sensing platform with on-chip compensation for temperature and mechanical stress, and possibly with on-chip read-out optics.

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1.1 Micro ring resonators

The framework of silicon photonics platform ePIXfab [3] has been utilized for fabricating micro-ring resonators, integrated with Out-Of-Plane grating couplers for optical interfacing. The devices are fabricated on a SOI wafer, using 193 nm deep-UV lithography process. The substrate was thinned to 250 µm after processing. The silicon device layer in the ePIXfab framework has a thickness of 220 nm, situated on a 2.0 µm thick SiO_2 bottom cladding. The waveguide width is 450 nm wide, so that the MRRs are single mode for TE polarized light at a wavelength of 1550 nm. No top cladding was applied to the devices, other than photo resist for temporary protection during dicing, and native oxide that will appear on an Si surface naturally. We used Multimode Interference (MMI) couplers to couple light between the ring and a straight bus waveguide, which is a very robust design approach. The MMI length and width are 57.15 µm and 6.9 µm, respectively.

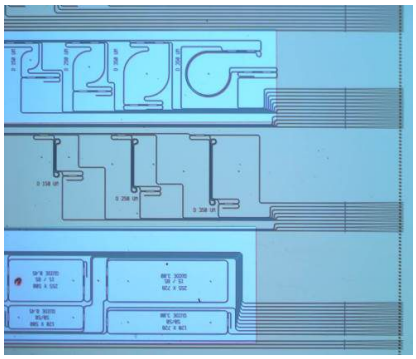

Figure 1: Microscopic image of the MRRs fabricated in SOI

Following the MRR fabrication, the wafer is diced into smaller pieces of 1.0 x1.4 cm each for post processing. Optimized post-processing steps to deposit 2 µm thick SU8 and SiO_2 layers on reference rings has been developed (Table 1Table 2). The process step for SU8 coating is straight forward, requiring only to spin coat SU8 and then to selectively remove it. The measured thickness of the SU8 layer deposited for this experiment is 1.95µm. SiO_2 on the other hand requires a thin Si_3N_4 layer to be pre-deposited as an etch stop layer for its plasma etching step. Without this etch stop, the SiO_2 buffer layer underneath the waveguides may be etched while locally removing the shielding SiO_2 layer, causing serious modification of the mode properties. However, this also results in a thin Si_3N_4 layer remaining on the sensing ring, which will slightly reduce the sensitivity of the sensing ring. The measured thickness of the Si_3N_4 layer and the SiO_2 layers are 184 nm and 1787 nm, respectively, resulting in total covering layer thickness of 1971 nm. Figure 1 shows a microscopic image of the fabricated MRRs together with their access waveguides. The chip contains many different types of rings, we see circular (top row), folded straight (center row) and square rings (lower row), designed to support a variety of applications. In our experiment, the upper row was used for the uncovered sensing rings, and the second row was used for the covered reference rings. Figure 2 shows a schematic of the post-processing steps performed on the SOI MRRs to realize the covered reference rings.

Table 1. The process flow for depositing SU8

Steps	Process	Parameters
1	Dicing	Die size 1.0 x1.4 cm
2	Remove resist protection layer	Rinsing with Acetone and Iso propyl Alcohol (IPA).
3	Dehydration	In hotplate at 200 ºC for 10 min
4	SU-8 coating	Spin resist SU-8 at 2000 rpm (to get a layer thickness of 1.95 µm); Soft bake for 1 min at 65 ºC.
5	Exposure	Exposure time 13 sec; Post Exposure Bake 1 min at 65 ºC for 1 minutes.
6	Developing and inspection	Time:1 min in SU-8 developer and rinse with IPA and dry.

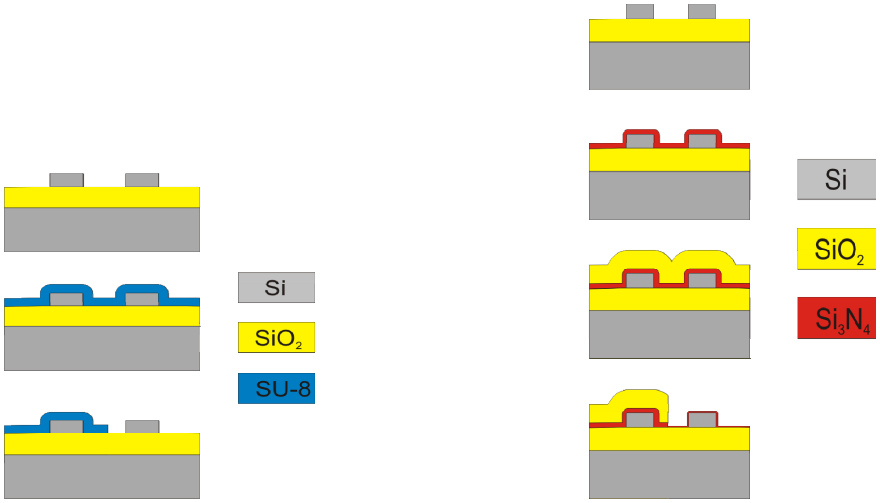

Figure 2. A schematic illustration of the post processing steps performed on the SOI devices to deposit the covering layers. The left picture shows the steps for a SU8 coating whereas the right picture shows that for a SiO_2 coating.

Table 2. The process flow for depositing SiO_2 layer

Step	Process	Parameters
1	Dicing	Die size 1.0x1.4 cm
2	Remove protection layer and cleaning	Rinsing with Acetone and IPA.
3	PECVD Si_3N_4 layer	Temperature: 300ºC; N_2 flow 300 sccm, Pressure 1000 mtorr; SiH_4 flow:20 sccm; NH_3 flow:20 sccm; N_2 flow:980 sccm; Pressure:650 mtorr; Grow rate Si_3N_4 13 nm/min
4	Thickness measurement	Woollam ellipsometer
5	PECVD SiO_2 layer	Temperature: 300ºC; N_2 flow 300 sccm, Pressure 1000 mtorr; SiH_4 flow:8.5 sccm; N_2O flow:710 sccm; N_2 flow:162.5 sccm; Pressure:1000 mtorr; RF power:20 W; Reflected power:1 W; Grow rate SiO_2 72.5 nm/min
6	Thickness measurement	Woollam ellipsometer
7	Photoresist (AZ5214)coating	Spin HMDS; 3000 rpm; 2 min hotplate 175ºC; Spin resist AZ5214; 1300 rpm (layer thickness 2.2 µm); soft bake for 30 min at 90 ºC
8	Exposure	Exposure Time: 9 sec; Soft contact.150 mJ/cm^2
9	Developing	Time:120 sec and hard bake for 30 min at 125ºC
10	Etching SiO_2 layer	Pressure 2.6x 10^{-3} mbar; RF1 2500 W; SH RF2 300 W; Bias 37.5V; Gas flow C_4F_8: 20 sccm; H_2 100 sccm; CH_4 10 sccm; Etch rate SiO_2: 216 nm/min and Etch rate AZ5214:131 nm/min.
11	Remove resist remaining's	Rinsing with Acetone and IPA.and drying

2. CHARACTERISATION

Transmission spectra of the MRR were measured using a C-band (near 1550 nm) broad-band source (Er-doped ASE source) in combination with an optical spectrum analyzer. The photonic chip is mounted on a Peltier element for accurate temperature control. Figure 3 shows a typical spectrum of one of the MRR before post-processing. The Free Spectral Range (FSR) is 500 pm, and the on-off ratio is better than 15 dB.

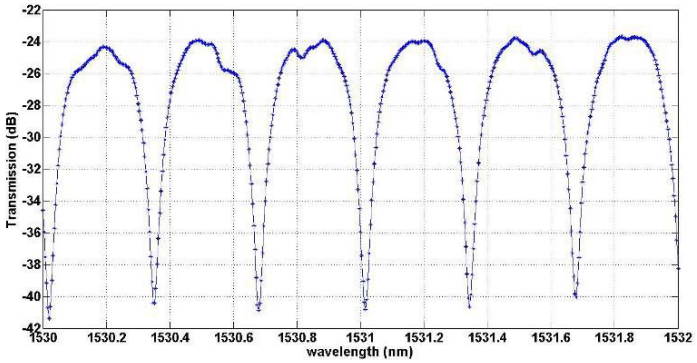

Figure 3. A measured through port transmission spectrum of a MRR before post-processing.

The transmission spectra of both the sensing ring and the reference rings are measured at different temperatures. The temperature is varied from 20 ºC to 40 ºC in steps of 2 ºC and the change in its resonance wavelength is monitored. Figure 4 shows the change in resonance wavelength with respect to temperature for both the sensing and the reference rings, both for SU8 and SiO_2 covering layers. The sensing rings show a sensitivity of 67.1 pm/ºC and 52.7 pm/ºC for the SU8 processed chip and the SiO_2 processed chip, respectively. The difference of nearly 15 pm/ºC is quite remarkable. Possibly, this is caused by the remaining thin Si_3N_4 layer on the SiO_2 processed chip. It indicates that for high accuracy sensing the temperature sensitivity should be calibrated, not on every sample, but possibly from batch to batch. Also the temperature sensitivity of the reference rings varies a bit, from 55.4 pm/ºC and 60.9 pm/ºC for the SU8 processed chip and the SiO_2 processed chip, respectively, again indicating the need for prior calibration. Also the dependence will depend on the ambient (aqueous or air-like). Still, the effect of temperature on all four rings are comparable, indicating that both coatings are good candidates as reference rings. Further, the effect of ambient index change on the MRRs has been measured for both SU8 and SiO2 processed chips as given in Figure 5, by measuring the response to varying salt concentrations in de-ionized water. For both cases; as required, the reference rings are unaffected by the ambient index change. However in the case of the sensing rings, there is a substantial reduction in ambient index sensitivity for a SiO_2 processed chip compared to that of an SU8 processed chip. This is attributed by the presence of the Si_3N_4 etch mask layer still remaining on the sensing ring.

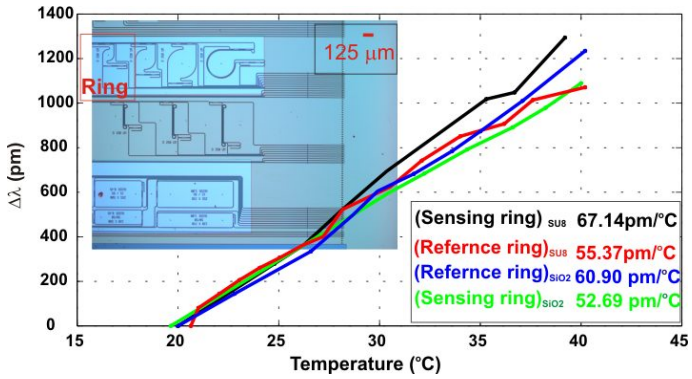

Figure 4. Effect of temperature on change in resonance wavelength of sensing and reference MRRs with the microscopic image of MRRs shown in inset.

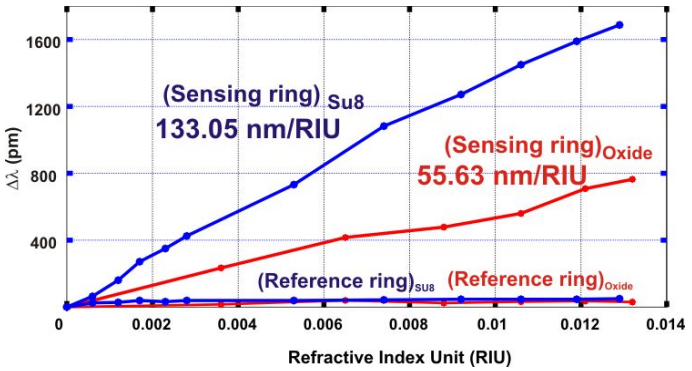

Figure 5. Effect of ambient index on change in resonance wavelength of sensing and reference MRRs.

We also analyzed the stability over time of the SU8 and SiO_2 cover layers in water, and found that the SU8 causes a slow drift in MMR response over tens of pm due to water permeation, until stabilization occurs after approximately 40 minutes. In practice, this would mean that a measurement is done during this drift, and should not take longer than 1-2 minutes, or each sensor would need a 'wetting' time of 1 hour at least. In practice, both strategies are rather inconvenient, and we believe that SiO_2 cover layers are preferred.

3. OUTLOOK: OPTICAL COUPLING AND ON-CHIP INTERROGATION

We have developed a concept to have a low-cost, robust and user-friendly multi-channel optical connection to a chip (Figure 6). Non-photonic experts can perform photonic chip characterization within only a few hours of training. The system is free from close-proximity fibers to establish the optical connection, since these typically get damaged rather easily. Placing a chip with a flow cell in the device, getting it aligned, and starting the measurement is a matter of typically 2 to 3 minutes. The system can be upgraded with thermal control, more optical channels, and is suitable for miniaturization: the current system is the size of a desk top PC, however, we envision implementation the size of a mobile phone.

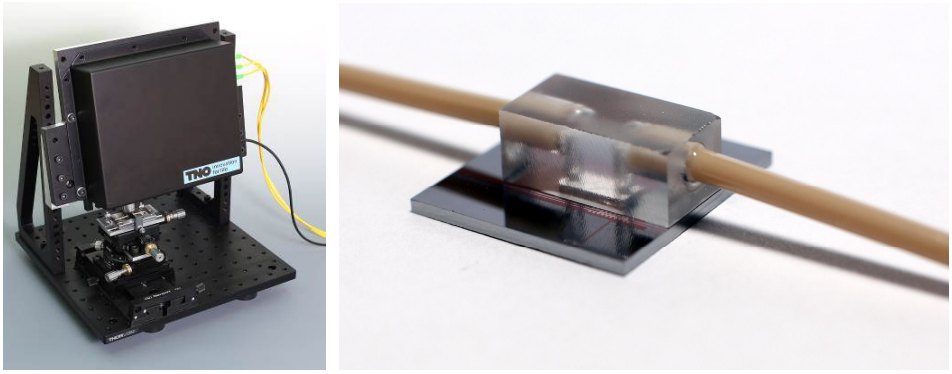

Figure 6. Picture of FRESCO set-up and chip with flow cell

The main cost driver for a read-out system is in the optics. Either one needs a broadband light source in combination with a spectrometer, or a scanning narrow-band source in combination with a broadband detector. Typically, the spectrum analyzer cannot meet a 1 pm resolution or better, and tunable lasers costs several 10s of k$. We believe that the most cost-effective way to have a small-size read-out unit is to make use of a low-cost tunable laser. This can be a temperature-tuned DFB laser for example (speeds in the order of 1 Hz are typically OK), or a Vertical Cavity Surface Emitting Laser (VCSEL), the wavelength of which depends strongly on the drive current. A tuning range of a few times the MRR FSR, so typically a few nm at most, is sufficient. To achieve high accuracy, real-time wavelength tracking of the scanning laser wavelength is essential. We have a large experience in the use of 3-port interferometers for wavelength tracking, both in fiber-optics and in integrated optics. We have taken first steps to incorporate on-chip reference sensors and a 3x3 interferometer [4,5] in obtain a single integrated sensing platform. The 3-port interferometer enables on chip interrogation for this sensing platform, with its three outputs which are at a 120º mutual phase difference.

This makes sure that at any input wavelength there is at least one output which has sufficient amplitude and a derivative with respect to wavelength. In our current tests, the interferometer provides a wavelength accuracy in the order of 1% of its periodicity, which can be easily tuned by customizing the optical path length difference. This sensing platform with its on-chip reference sensor, on-chip interrogator and optical coupling platform will give rise to a new step towards the commercialization of cost effective, multiplexed cheaper solutions for gas and bio sensing.

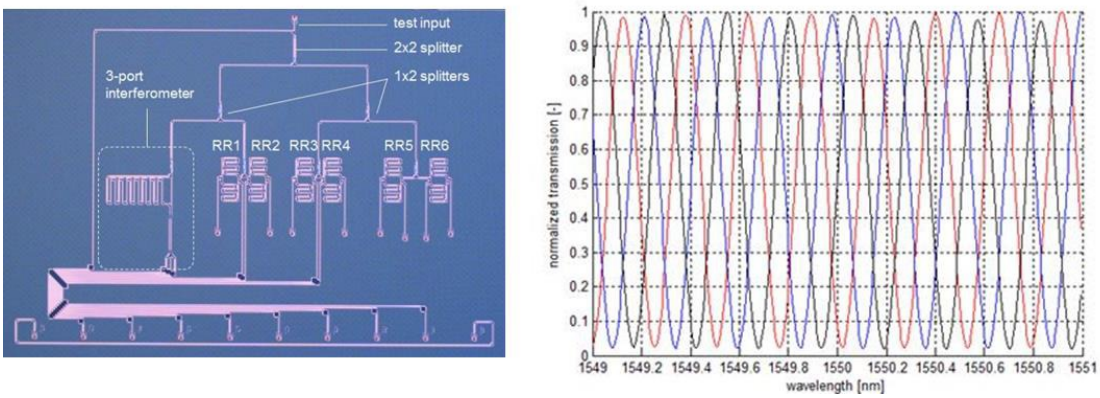

Figure 7: A microscope image of a sensing platform which consists of six MRRs and a 3x3 interferometer (left), and interferometer response (right).

4. CONCLUSIONS

We report on the development of a Silicon-On-Insulator (SOI) compact photonic sensing platform. The sensor elements are Micro Ring Resonators (MRRs), integrated with reference MRRs on a single chip. We have developed a dedicated easy-to-use optical coupling setup to enable testing without the need for tedious fiber-chip attachment. In order to enable correction for variations in environmental conditions such as temperature and mechanical stress, we have studied the performance of uncoated sensing MRRs, and of SU8- and SiO_2-covered reference MRRs. The sensitivity to ambient refractive index was determined by measuring the response to varying salt concentrations in de-ionized water, and ranges from 50 to 130 nm/RIU depending on the MRR configuration. The reference MRRs showed negligible sensitivity to ambient index. We also analyzed the stability over time of the SU8 and SiO_2 cover layers in water, and found that the SU8 causes a slow drift in MMR response over tens of pm due to water permeation, until stabilization occurs after approximately 40 minutes. Even though the use of SU8 is beneficial for ease of processing and costs, we believe that SiO_2 is the material of choice for typical applications. In addition, we present our optical coupling set-up, which enables us to quickly align and perform tests on MRR sensors, typically in combination with microfluidic flow cells. The platform allows non-photonic experts to characterize surface activation processes using MRRs. We believe that such a concept is essential for the use of MRRs in biosensing research.

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