Suitability of Integrated Protection Diodes from Diverse Semiconductor Technologies

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***Abstract*— In this article diodes from three different semiconductor technologies are compared based on their suitability to protect a receiver. The semiconductor materials involved are Silicon, Gallium Arsenide and Gallium Nitride. The diodes in the diverse semiconductor technologies themselves are close in performance, but the possibility to integrate high quality passives will give better performance for Gallium Arsenide and Gallium Nitride based protection diodes.**

I. INTRODUCTION

The constantly increasing demand of advanced sensors and communications systems aboard military and civilian platforms (e.g. ships, manned and unmanned aircrafts, base stations, land vehicles, etc.) requires accommodating on a limited space a large number of antennas. This poses stringent constraints in terms of available space and weight with respect to the optimal siting needed to maintain the desired coverage. Moreover, in the design of the overall platform, many different parameters have to be kept under control to limit Radar Cross Section, Electromagnetic Interference, and vulnerability. In view of this, new platform concepts are based on the structural integration of the antenna with the platform.

Phased array antennas are particularly suitable for integration. The space occupation is minimised by scanning the beam electronically instead of mechanically and the overall antenna size can be limited by choosing a printed design. However, one of the most vulnerable points of phased array antennas is the Transmit and Receive (TR) module. A high power signal impinging on the antenna can lead to the destruction of one or more modules. Such signal could be generated by an enemy system in a military scenario, as for example a jammer, or by an own system (e.g. transmitter leakage, large reflections or antenna disconnect).

Typically, limiters are used to protect the front-end of a phased array. In this article the suitability of integrated diodes for the protection of circuits in diverse technologies is evaluated. In most modules the protection is handled by circuits outside of the integrated circuit that contains the receiver. To enable further integration it is desired to enbody the protection in the integrated circuit. For this purpose several diodes designed in different semiconductor MMIC processes have been evaluated. Specialized processes have not been used since also active RF circuitry has to be integrated. This remainder of this article is divided into 4 sections. The first section discusses results obtained for Silicon based diodes. The second section handles GaAs-based diodes. The third section presents GaN-based diodes. In the last section the semiconductor technologies are compared and conclusions drawn.

II. SILICON BASED DIODES

The first semiconductor evaluated is Silicon. To protect a receiver input an anti-parallel pair of diodes can be placed in front of the input stage. In contrast to ESD protection devices, these diodes can not be placed outside the RF-path. In BiCMOS processes the base-collector diode forms a low-capacitance diode and is thus an ideal candidate for protection. This of course adds capacitance and loss and thus increases the noise figure. To evaluate the suitability of the base-collector diode, 20 and 50 µm wide diodes have been placed on a test-cell. To increase the maximum power the active area in the diode has been layout using dots with a 6 µm pitch. NXP Semiconductors QUBiC4X BiCMOS process was used for the design. This is a 0.25 µm process.

The maximum CW current for a 20 µm diode based on design rules is 35 mA. This is equivalent to a power of 13 dBm according to:

$$P_{AVS} = \left(\frac{I_{Short}}{2} \right)^2 \cdot R \qquad (1)$$

The factor 2 is due to the fact that the short circuit current of a source is twice the current when the source is matched. The effect of forward voltage or residual resistance is here ignored. It is assumed that the RF part of the current has no influence on the maximum current rating.

For the 50 µm devices the current and the resistance scale so the maximum power according to design rules is 20 dBm.

Large signal measurements have been performed on the actual devices using the measurement set-up shown in figure 2.

The measurement results show that the maximum CW power is 1 W for a period of several seconds for the 20 µm devices, for the 50 µm devices the maximum power is 2 W and for an anti-parallel connected pair of 50 µm devices 5 W can be tolerated. Figure 3 shows the measurement results for 20 µm devices with a 50 Ω DC ground return. Due to the half-wave rectifying the output power is not constant after the onset of limiting.

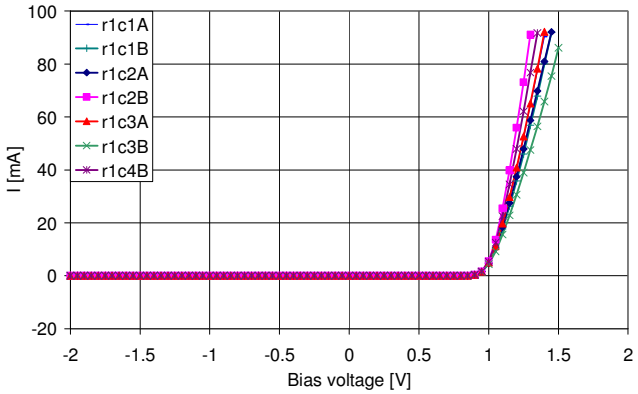

Fig. 1 DC measurement result of a 20 µm shunt-connected diode.

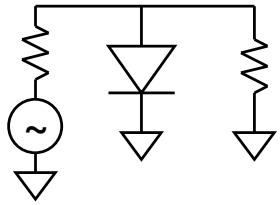

Fig. 2 Schematic view of RF measurement set-up used for the diode.

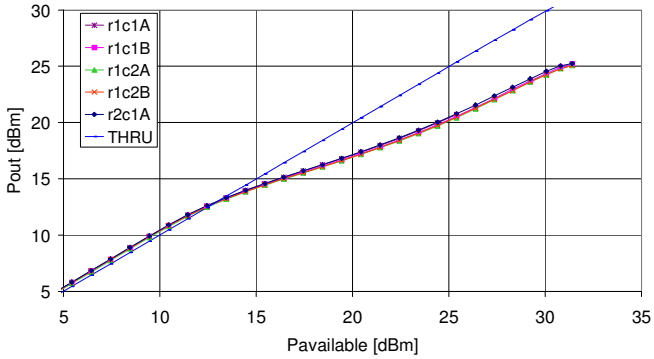

Fig. 3 Measurement result of a 20 µm shunt-connected diode at 3 GHz with 50 Ω ground return. The straight blue line gives the reference measurement of a THRU.

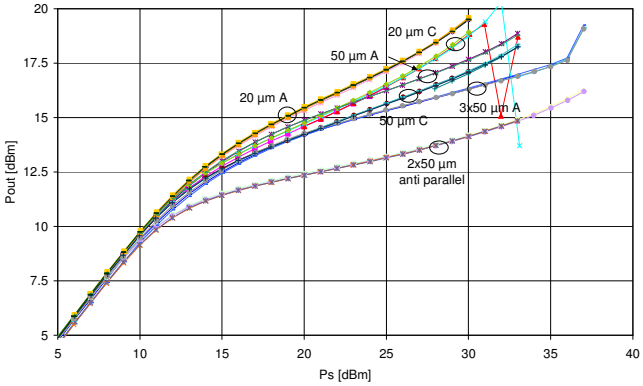

Fig. 4 Measurement result of all diodes with a DC short ground return.

Figure 4 shows the measurement results for all diodes with a DC short as ground return. The A indicates that the anode is connected to the line and a C indicates that the cathode is connected to the line. It can be seen that the output power is lower for larger diodes and that for the same size of diode the cathode connected to the line gives better limiting. The anti-parallel pair gives the best limiting and is independent on the ground return provided. The dips and peaks at the right part of the traces indicate diodes that are damaged during the measurement.

A DC measurement of the diodes after application of power gives for some devices an increased series resistance of up to 100% indicating that the diode is damaged by the large power applied. It can therefore be concluded that the diodes can survive the power levels applied for a short period of time of several seconds.

The extracted capacitance at a diode voltage of 0 V is 23 fF for a 20 µm anode connected device and the power loss is so small that it could not be accurately measured using the available equipment. For a cathode connected device the capacitance is doubled. This indicates that it is possible to obtain protection for Watt-level pulsed input powers on low-voltage Silicon receivers without a significant impact on performance. Although Watt-level protection is not sufficient for many applications it will relax the specifications of the main-limiter. Using the maximum current and the diode capacitance a figure of merit can be defined. In particular, a suitable figure of merit is the current/capacitance ratio because it expresses how much capacitance is required to allow a certain current flowing. For the evaluated Silicon diode the figure of merit is 1.52 A/pF (35 mA/23 fF). When the measured current capability of 90 mA is used the figure of merit is even 3.91 A/pF.

To asses the effect of long lasting input power a thermal analysis of a combination of three 50 µm diodes has been performed. Figure 5 shows the steady-state temperature on the surface of the chip when 334 mW is dissipated.

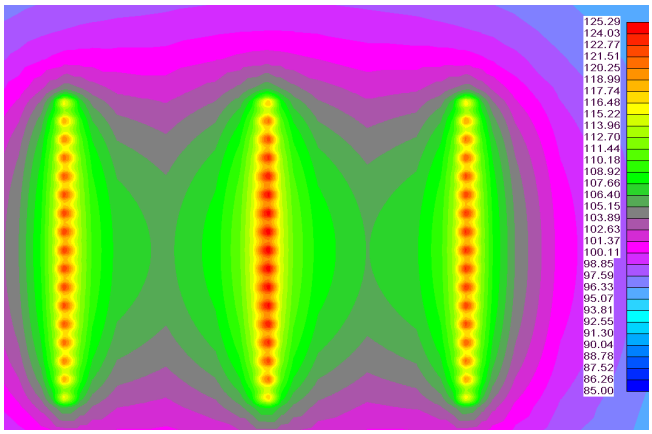

Fig. 5 Thermal simulation result of three 50 µm diodes with a dissipated power of 334 mW, the indicated temperature is in °C.

From a reliability point of view a temperature of 125°C is considered a safe value. The backside of the chip has a temperature of 85°C. Assuming a forward voltage of 1 V the allowed current is 334 mA. This is only 25% higher than the

current value needed to comply with the design rules. This is equivalent to the short circuit current of a 50 Ω source with an available power of 1.4 W.

III. GaAs based diodes

The second semiconductor evaluated in this study is Gallium Arsenide. Due to the lower thermal conductivity a lower thermal load is allowed per area. The diode is created by employing the Schottky gate contact of the pHEMT. The source and drain contacts are shorted. The diode current is limited by either the maximum current through the gate metal or the current through the 2DEG layer. An optimum is found by using short gate fingers. In the WIN PP50-11 process a diode is created using 4 gate fingers and a finger width of 5 µm. The WIN PP50-11 process is a 0.5 µm pHEMT process optimized for power performance. Figure 6 shows the DC measurement result of such a diode.

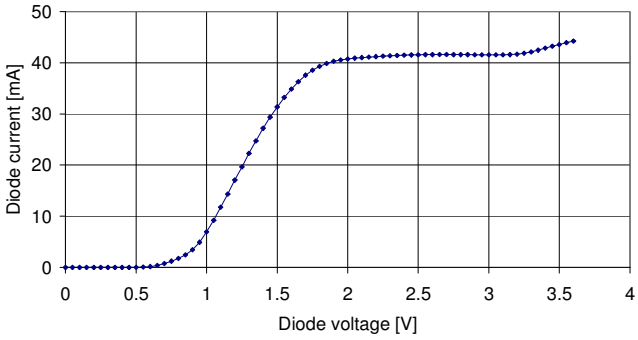

Fig. 6 Measured I-V curve of a GaAs diode with 4 fingers of 5 µm.

The diode current behaviour is due to the 2DEG layer. The measurements can be fitted with the simulation results obtained using a diode model and a GaAs resistor model for the resistance between the Schottky diode and the contact. In figure 7 the measurement result of a GaAs semiconductor resistor is shown. It can be seen that the current first increases linearly with the voltage and at 6 V saturates. The reduction in current after 9 V is due to self heating. After 13 V the resistor is destroyed and the simulated temperature of the resistor is 275°C at that point.

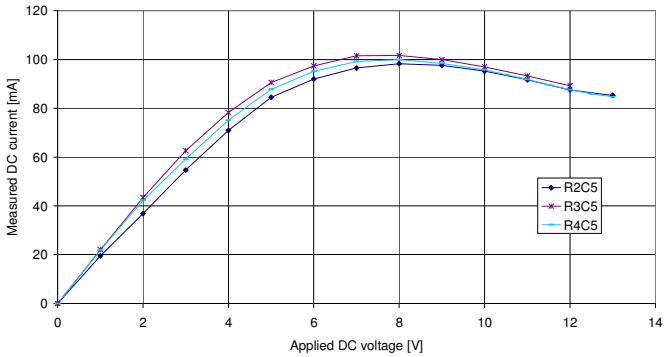

Fig. 7 Measurement result of a GaAs semiconductor resistor; W/L=100/20 µm.

The resistor can be empirically modelled using the following equation [3]:

$$I_{RES} = W \cdot I_{MAX} \cdot \tanh\left(\frac{V_{RES}}{R \cdot W \cdot I_{MAX}}\right) \qquad (2)$$

The current through the resistor (I_{RES}) is calculated using I_{MAX} as the maximum current per width (W). V_{RES} is the voltage across the resistor and R is the small signal resistance.

To improve the fit a part of the resistance can be modelled using a linear resistor. It is believed that this part is the contact resistance due to the ohmic contact.

The maximum current through the diode is 41 mA for a diode capacitance of 39 fF at a voltage of 0 V. The defined figure of merit is 1.1 A/pF. This is equivalent to a power of 23 dBm. The current starts to increase again with the voltage just before the diode is destroyed. When the diode it destroyed it forms a short circuit. If the diode is used as a limiter, the voltage across the diode increases fast once the maximum current value is reached. After this point, the dissipation also increases to the point that the diode is destroyed. In [1] this type of diode is used to create a 5 W limiter with 1 to 2 dB loss. In such a limiter the high capacitance of the diodes is compensated by inductors. This is possible because of the low loss of the substrate.

IV. GaN based diodes

The third semiconductor evaluated is Gallium Nitride. Due to the fact that a thin GaN layer is epitaxially grown on Silicon Carbide, the effective thermal conductivity will be dominated by the superior thermal conductivity of SiC. Also in this case the diode is created using the gate contact of a transistor with drain and source shorted. In particular, the designed diode has 2 fingers of 50 µm and a gate length of 0.5 µm. This is not optimal with respect to the current through the thin gate finger.

Figure 8 shows the measured I-V curve of this diode. For a voltage higher than 5 V the diode is damaged and half of the current flows, so probably one gate finger is destroyed.

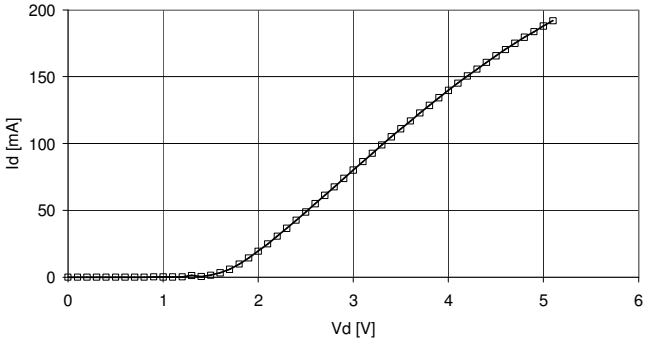

Fig. 8 Measured I-V curve of a GaN diode with 2 fingers of 50 µm.

According to this figure, no limiting effect can be observed in the diode current. However, it can be reasonably expected that the limiting behaviour with respect to the current will

occur in diodes with a shorter gate width and more gate fingers. The capacitance of this structure is 0.16 pF. This brings the figure of merit to 1.2 A/pF, a value similar to that already observed for the Si and GaAs diodes.

A maximum current limit has been observed for another GaN diode. This is a GaN diode in another process with a gate length of 2 µm. The measurement result is depicted in figure 9. Due to the long gate length of 2 µm the diode capacitance is 5 pF and the current capacitance ratio is only 0.17 A/pF.

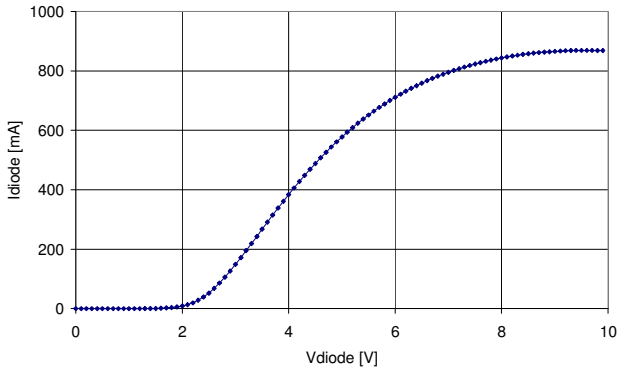

Fig. 9 Measured I-V curve of a GaN diode with 8 fingers of 50 µm.

V. Conclusions

In this paper the suitability of diodes designed in three different semiconductor materials to protect a receiver from high power input power levels has been investigated. The measured performances of GaAs and GaN diodes appear similar. The current capacitance ratio of the Si diodes is more than 3 times higher than of the GaAs and GaN diodes examined. The advantage of GaAs and GaN diodes with respect to Si is that the high quality passives enable the compensation of the diode capacitance without excessive losses.

A diode with a high figure of merit should have a high number of fingers. The gate fingers employed must have a short gate width to reduce the maximum current in the gate metal and have short gate length to reduce the capacitance.

TABLE I
Comparison of Semiconductor diodes at 300 K

Semiconductor material	**Thermal conductivity [2]**	**Current capacitance ratio**
Si	130 W/mK	3.9 A/pF
GaAs	55 W/mK	1.1 A/pF
GaN	130 W/mK	1.2 A/pF
SiC	370 W/mK	n.a.

The advantage of GaN with respect to GaAs is the higher thermal conductivity of the SiC layer directly under the GaN substrate which allows for a more compact design. The higher forward voltage is no problem when the receiver is also integrated in GaN since the GaN input stage transistor can handle higher input levels. Table I lists the thermal conductivity of the used substrate materials and the current capacitance ratio found.

Acknowledgment

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