

1 GHz GaAs Buck Converter for High Power Amplifier Modulation Applications

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Abstract—A fully integrated 1 GHz buck converter output stage, including on-chip inductor and DC output filtering has been realized, in a standard high-voltage breakdown GaAs MMIC technology. This is a significant step forward in designing high-speed power control of supply-modulated HPAs (high power amplifiers). Agile power controlled HPAs are intended to find application in high-efficiency transmitters for both radio communication and radar applications, especially in which phased array transmit chains are used. Rapid, accurately controlled, power efficient power supplies, with rapid ramp-up and ramp-down, provide control over HPA output signal envelope rise and fall-times versus spectral switching side-lobes. Simultaneously power efficient tapering of a phased array transmit antenna is possible without the need for applying special fixed attenuators or modified antenna elements.

Keywords - Buck converter; switch mode power supply; MMIC; GaAs 1 GHz;

I. INTRODUCTION

Phased array systems today will face integration of sub-blocks, as is taking place in development of e.g. mobile phones, consumer electronics and satellite systems.

Phased array element functionality has increased over time: In passive phased-array systems, where only a large number of phase shifters were present, more electronics are presently applied, including RF HPA, LNA, phase shifters and RX/TX switching means. Even A/D conversion is often integrated, allowing for digital beam-forming.

One of the last remaining not fully distributed functionalities is the power supply unit and its regulation. With one single power supply for the entire array, all transmitters could only be controlled in parallel, no elements would be individually controllable. Note that the transmitting HPA's operate in their saturated region and can practically only be controlled by altering their supply voltage, as alternatively, controlling their input levels would yield inaccurate output powers and phases of the HPA's, because of present spread and differing temperature dependency of the HPAs. Phase and power deviation of HPAs thus can be reduced and kept within acceptable values, when regulating the supply individually. Altogether, the full distribution of the final DC power converter into several small converters, would allow for more flexible control of the HPA's pulse power, over time and array position.

A number of integrated DC/DC converters have been reported for low to medium power [1], also in GaAs technology [2], with some demonstration of power converter

integration with the RF amplifier, but limited to low voltage / power levels [3], all of this mostly directed to telecom HPA applications. For phased array systems, integration of the drain-supply pulse switch has been reported [4], [5]. Several other reported converters merely produce a fixed output voltage, which would not address tapering and ramp-up/down as mentioned above.

We report here the design and test of a 1 GHz DC/DC step-down switching buck converter output stage, manufactured in a high breakdown voltage GaAs technology, which can in a later phase be integrated with a HPA on the same chip onto a full power controlled MMIC HPA. The 1 GHz frequency was chosen to investigate effects as loss mechanisms, inductor aspects and overall efficiency. A block schematic is shown in Figure 1; the circuit in the dashed block was implemented. In an ideal buck converter, with a capacitor value assumed infinite, the inductor current would have a triangular waveform. In the chosen implementation this will not be the case, yet operation as buck converter is maintained.

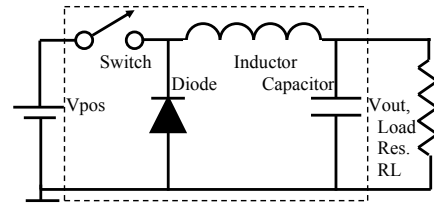


Figure 1 Buck output stage principle

II. CONCEPT DESIGN

A. Switching frequency

Switching at a frequency of 1 GHz helps to decrease filtering requirements. Optionally, shifting the switching frequency, spurious frequencies from a HPA mentioned above, could be shifted to a favorable frequency, either to fulfill spurious emission requirements or to reside outside of the receiver bandwidth.

Concerning the high switching frequency, note that before the design phase could start, a dedicated modeling wafer has been manufactured, and a complete design kit established at TNO, used in the simulations. The process was WIN PP50-20 having e.g. a breakdown voltage $V_{dg} \approx 35 \text{ V}_{max}$ @ $V_{gs} = -3 \text{ V}$, $IDSS \approx 175 \text{ mA/mm}$ and $f_T \approx 12.5 \text{ GHz}$ @ $V_{ds} = 4 \text{ V}$. The buck converter output stage was fully integrated and contains FET-switches, diodes, buck inductor and output filter, all on one MMIC.

B. Inductor

Chip inductors as they are usually applied on GaAs chips, give rise to resistive losses and low allowed maximum current, due to the used thin gold metal applied in narrow traces. With inductors on silicon chips, these problems increase, due to the use of aluminum being a worse conductor than gold and because of substrate coupling, capacitive and inductive.

In the current design a row of gold bond-wires is placed on the MMIC in an advantageous fashion, as to create an inductor, yielding a substantially lower loss than the standard inductors and a higher current capability.

The behavior on harmonics, of a bond-wire inductor differs substantially from that of a real inductor and of an ideal inductor. The bond-wire inductor, in a buck converter arrangement, has a current waveform which is not triangular as mentioned in the introduction, on either of its two ports. It is beneficial to enhance efficiency of the buck converter, by changing the waveforms, applying "harmonic tuning". This can be done by manipulation of the bond-wire structure. In HPA design the terminology "harmonic tuning" is used, whereas in power supply design, a corresponding terminology exists including the terms "Zero-Voltage Switching (ZVS)" and "Zero Current Switching (ZCS)" [6]. In the current realization, the bond-wire structure as implemented, was adequate to obtain promising efficiencies. Further topology-tuning of the bond-wire structure, will lead to even higher efficiencies, as was revealed in an experimental simulation with "harmonic tuning" applied.

C. Output filter

The output filter is placed after the buck inductor. A notch filter architecture was chosen to suppress the switch frequency, see Figure 2. It has a lower capacitance than a single capacitor providing the same ripple suppression. In this manner the capability for rapid ramp-up and ramp-down is improved, meanwhile keeping the filter size as low as possible. There is a small effect on the current waveform in the bond inductor, but this is negligible.

D. Switch

Ideally, for a buck converter with positive supply, the switch would be a P-channel device, which has its source connected to the positive supply rail, while the gate is driven between gate and source. The pulse generator charging the gate capacitance then only has to provide a small drive voltage swing, in the order of 1...2 Vpp, while providing gate charge current, to obtain full on- and off switching of the FET-switch. However, in current GaAs and GaN processes, no P-channel devices are available. Thus resorting to an N-channel device, and maintaining the concept of driving the FET-switch between gate and source would require a "floating" driver. Because the main objective is the feasibility of applying the buck converter principle at 1 GHz, the design of such a pulse generator, having its own specific issues as having its dedicated efficient supply, was studied and simulated, yet postponed, to be solved in future work. Therefore in this study, the FET-switch is driven at the gate, refer to Figure 2.

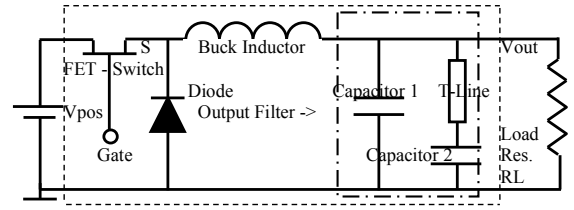


Figure 2 Buck output stage schematic

E. Switch driver for test

A square wave signal of over 20 Vpp would be needed at the gate of the output FET-switch. While testing on a probe station, the drive signal would have to be applied through probes, to the FET-switch gate.

To avoid the issue of preserving a square waveform, it was chosen to place a square-wave driver on-chip, for testing purposes only, see Figure 3. At the RF input of this driver a sine-wave drive signal is applied of 0.5...4 Vpp, as is available from standard RF generators. The driver is designed to convert the applied sine wave into a variable duty-cycle 20 Vpp square wave drive signal, which is then on-chip applied to the gate of the buck FET-switch. (The power dissipation of this driver is not taken into account in the performance figures as it is not the definitive driver).

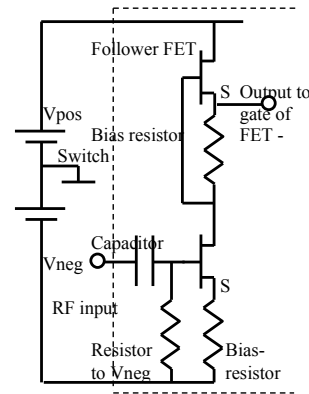


Figure 3 Switch driver for test - schematic

F. Loss aspects

When operating at high switching frequencies, parasitic components (capacitances in combination with resistances) have a significant impact on the overall performance of the buck output stage. Effects include

1 Static loss:

- FET-switch on-resistance R_{on}
- Inductor resistive loss

2 Dynamic switching losses:

- As the switch goes on, the diodes go from conduction into non-conduction, whereby their junction capacitance charge has to be removed.

- As the switch goes off, in roughly 10% of the cycle time, the inductor current (which with an ideal inductor is at its maximum) flows through the switch, giving dissipation.
- The switch itself has considerable parasitic capacitances being charged and discharged.

As remedy ZVS or ZCS techniques [6] could be applied, but with care, because these techniques involve resonators (cq harmonic tuning) which could let FET-switch junction voltages exceed breakdown. Lowering V_{in} to cope with this would then give suboptimal operation.

III. TECHNOLOGY CHOICE

Concerning the transistor drain source breakdown voltage to be switched by the buck transistor, including the transients, a supply of half of the breakdown voltage is the maximum limit to allow for a maximum switching voltage swing of the source of the buck FET-switch. This dimensioning appears very different for GaN technology, where maximum RF power density is limited by thermal and reliability requirements, and not by the breakdown voltage or current density. This is a distinctive advantage of GaN, which makes it the ideal technology to integrate power conditioning circuits onto a HPA die. On the other hand, GaN remains today, at least for its integrated IC technology version, either difficult to access and expensive, or not fully industrialized nor stable. In the frame of this project, it has thus been decided to rely on a mature GaAs technology to implement a proof-of-concept demonstrator. As mentioned, the WIN-semiconductors PP50-20 technology has been applied, which can provide for drain-gate breakdown voltages around 35 V, which is notably higher than found in most standard processes. The design has been performed targeting an eventual implementation in GaN, scaling down the primary voltage to allow for the same step-down ratio between primary and secondary drain voltage.

IV. IMPLEMENTATION

Figure 2 schematically shows the external supply (indicated with V_{pos}), the FET-switch, diode, inductor, simplified output filter capacitor network and external load resistor.

A. FET-switch

The buck converter switch consists of two FET-switches of a moderate size 8x240, in parallel. An issue to be taken seriously is the gate width: TNO did a noteworthy modeling effort on PP50-20, which revealed that at large ($> 300 \mu\text{m}$) gate finger lengths, switching speed $d(I_{ds})/dt$ would drop unacceptably for this application, even with V_{ds} held constant. As a result, FET-switch channel on-resistance loss during the longer switching transients would increase. For example, when the FET-switch is switched off, its channel resistance becomes larger than the lowest value R_{on} at $V_{gs} = 0V$. This resistance varies over time, so the integral of nonzero buck inductor current ($i_L(t)$) times the voltage ($v(t)$) across the FET-switch channel, will result in more overall loss thus in reduction of efficiency. The primary voltage has been kept at a maximum of 20 V for this process. For future GaN implementation, this voltage will be higher and dictated by HPA supply requirements.

B. Diode

There are 3 diodes used in parallel, each diode is dimensioned having 20 fingers with each $16 \mu\text{m}$ length. These fingers are kept short as not to exceed maximum allowed current at the finger connection point and to keep series resistance low.

C. Inductor

Using Ansoft HFSS, an arrangement was sought which would provide an inductance of $\sim 13 \text{ nH}$ at 1 GHz. The outcome was that this is achieved using 5 bond-wires of diameter $25 \mu\text{m}$ and span $1300 \mu\text{m}$, which are bonded on 5 multilayer traces of $100 * 1400 \mu\text{m}$. This was simulated with wire heights $H = 250 \mu\text{m}$ and $300 \mu\text{m}$. Wire spacing $\approx 150 \mu\text{m}$, see Figure 4.

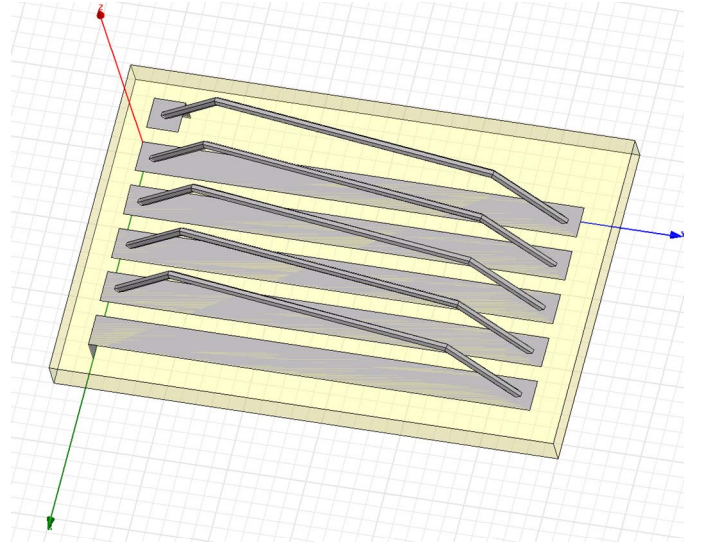


Figure 4 Bondwire inductor HFSS layout

D. Output filter

The ladder structure consists of transmission-lines with two capacitors, a series resonant notch and an extra capacitor suppressing higher harmonics, see Figure 5, right.

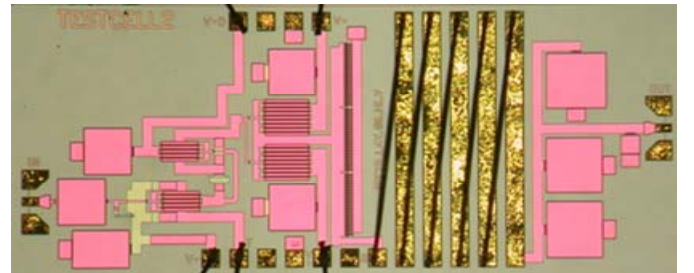


Figure 5 Driver and buck converter incl. bondwire inductor

V. TEST RESULTS

The manufactured chip is shown in the microscope image in Figure 5, showing the bondwire inductor.

The buck output stage has been measured over 3 load resistances (55.6, 100 and 122 Ω). Some measured efficiency examples are listed in TABLE 1. Efficiency (EFF) is defined as:

$$EFF = P_{out} / P_{in} * 100\%$$

whereby P_{in} is drawn from the supply. Supply voltage was 20 V. The drive signal of 1 GHz is applied to the input port of the driver (Figure 3 "RF input", Figure 5 left) through a coaxial probe, while V_{out} (DC) is extracted through another coaxial probe (Figure 2 V_{out} , Figure 5 right). (For testing, V_{pos} is connected to BarCap®-decoupling capacitors of 100 nF, not visible in Figure 5).

TABLE I. BUCK OUTPUT STAGE MEASUREMENTS, FREQ = 1 GHz

Test	Test results		
	RL	V_{out}	$EFF(\%)$
1	55.6	8.9	49.8
2	100	10.0	56.8
3	122	6.2	46.7
4	122	7.6	50.3
5	122	10.0	59.1

In Figure 6 measurements are compared to ADS simulations. The blue curve is obtained simulating with the HFSS S-parameters of the originally intended bond-wire structure. The pink curve is obtained in a similar manner, only 3 nH was subtracted on the input side of the bond-wire inductor, to approximate the mechanical shape after actual bonding.

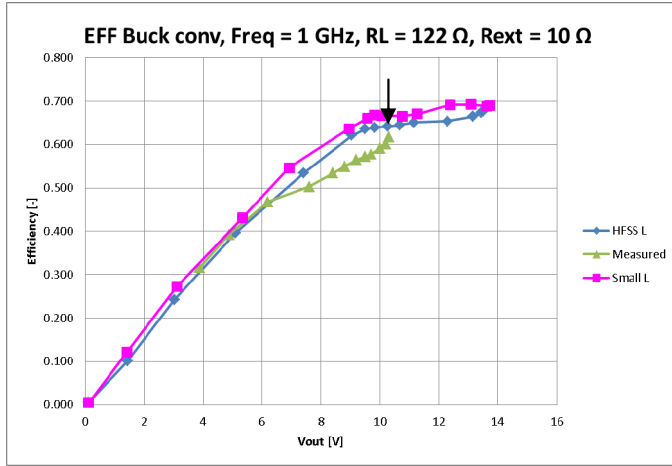


Figure 6 Measurement vs. simulations

The green trace represents measurements. Considering the loads applied, the buck output stage appears to perform best at $RL = 122 \Omega$. For example, in Figure 6, the rightmost point of the trace "Measured" corresponds to an efficiency of 61.8% at $V_{out} \approx 10.3$ V, $P_{out} \approx 0.869$ W. The closest simulation result is represented on trace "HFSS-L", (see arrow), associated with $V_{out} \approx 10.2$ V and an efficiency of 64.2% at $P_{out} \approx 860$ mW.

Some corresponding time-domain plots are shown in Figure 7: V_s (source voltage), V_{gs} (gate to source voltage) and V_{out} (output voltage).

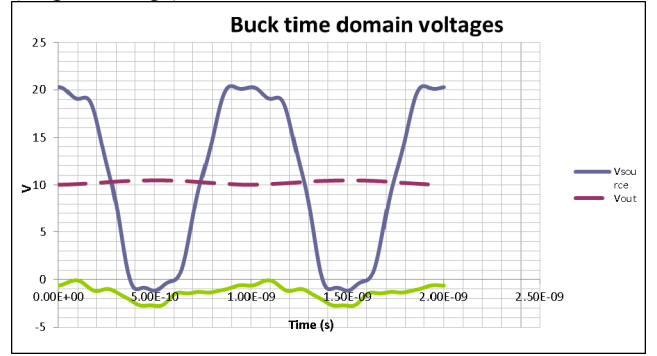


Figure 7 Simulated time signals for $V_{out} = 10.2$ V

Tests were performed at different switching frequencies (500-1000 MHz), but the buck output stage performed best close to the design frequency of 1 GHz.

VI. CONCLUSION

It has been demonstrated that a buck converter output stage, with all components on-chip, including a bond-wire inductor, and output filter, switching at 1 GHz, despite FET-switch switching losses, performs notably well. Such a converter can be integrated with control circuit, supplying a HPA, enabling power control on a chip-to-chip basis.

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