Set of X-Band distributed absorptive limiter GaAs MMICs

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***Abstract*— A set of X-band absorptive limiter GaAs MMICs has been designed and realised using both the PPH25x foundry process from UMS and the PP50-10 process from WIN semiconductors. The innovative limiter concepts have been extensively characterised by both pulsed and CW measurements. Both passive and active topologies have been implemented. The passive limiter design has a typical small-signal insertion loss of 1.5 dB at 10 GHz, and it can withstand (absorb) up to 4 Watts (36 dBm) of CW power without degradation or damage, while keeping the output power level below 100 mW (20 dBm). The active limiter handles up to 10 Watts of CW input power, at the cost of higher small-signal insertion loss. For all designs the input reflection remains low for any input power level. The used GaAs surface ranges from 2 to 3 mm^2.**

I. INTRODUCTION

Limiters are used to protect the sensitive input of the low-noise amplifier (LNA) of a T/R-module inside a phased-array radar system. A typical limiter will reflect high input power levels back to the circulator and the power amplifier (PA).

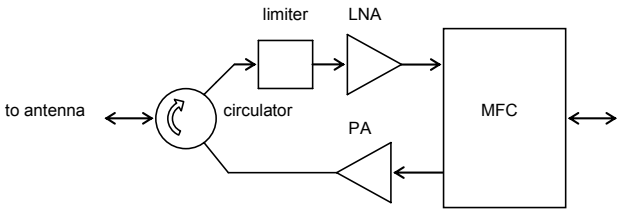

Figure 1 Typical limiter application in a T/R-module

In phased-array radar systems where the PA needs to be protected from high reverse power levels, the reflected signal could be routed to a high-power load by adding an extra circulator. This effectively creates an absorptive limiter but results in a bulky and costly design. When an absorptive limiter is realised using MMIC technology, a low-cost and small-sized circuit becomes possible as well as the integration with the LNA on a single chip.

When the absorptive limiter achieves losses, comparable to those of the combination of a ferrite isolator and a reflective limiter, there will be no degradation of the system noise floor.

II. MMIC TECHNOLOGY

The MMIC technology used for the first limiter design is the PPH25x process from United Monolithic Semiconductors (UMS). This is basically a process meant to be used for high-power amplifiers although the limiter does not use any active devices. For the second limiter design, the PP50-10 process from Wireless Information Networking (WIN) semiconductors is used.

III. PASSIVE LIMITER DESIGN

The passive limiter design is based on the use of Schottky diodes operating as current controlled switches. The advantage of using Schottky diodes is that there is virtually no delay in the response of the limiter. High-power UWB or RF pulsed sources will be limited just as well as CW sources.

In order to make the limiter absorb all of the applied input power, some special arrangement has to be made. In this case, an impedance transforming circuit is used which takes care of switching the excess input power to the on-chip high-power load resistors. For low input power levels the signal is routed to the output of the limiter. For high input power the signal is routed to the load resistors.

Another issue is keeping the diode currents below the maximum value for the process. To maximize the maximum input power, a distributed version is designed in which both the load resistors and the limiting function itself has been split up into several branches. Using this technique, the combination of maximum attenuation and maximum input power capability for the selected process is possible.

Both Agilent's ADS, Momentum and Orcad's PSPICE were used to design and predict the performance of the limiter. Foundry-supplied ADS models for the diodes, inductors and resistors were used.

The lumped-element equivalent schematic of the limiter is shown in figure 2.

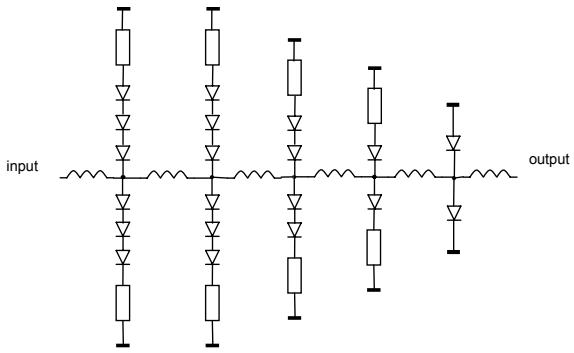

Figure 2 Lumped element equivalent schematic of the limiter.

IV. Active Limiter Design

The active limiter is based on the use of FETs operating as voltage controlled switches, where the envelope of the RF input signal is detected and drives the switches. The consequence is a needed delay of the RF input signal. In this design the current handling of the limiter is not dependent on the Schottky junction of diodes, but on the drain-source junction of the switch FETs.

The RF signal is delayed by a 5th order LC band pass filter to achieve enough delay to be able to trigger the switch unit before the RF signal reaches the output. The switch unit consists of three parallel FETs connected to load resistors, which absorb the incoming signal and a series switch to create a high impedance node at the output of the limiter.

The parallel and series switches are controlled by the input signal via positive and negative peak detectors. A bias voltage is needed for the level shifter to drive the positive peak detector.

A block schematic of the active limiter concept is presented in figure 3.

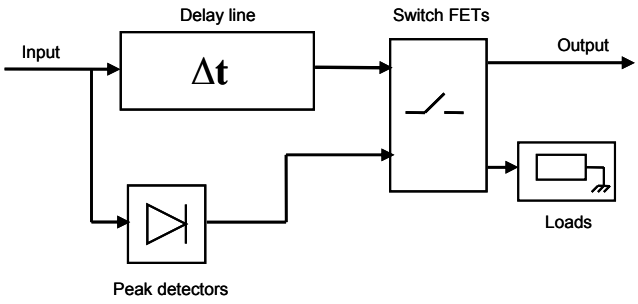

Figure 3 Block schematic of the active limiter.

A second active limiter version is designed with an external delay line, which can be made as a 50 Ω line on a PCB. This solution exhibits less loss than the 5th order band pass filter, but more circuit-area is needed to realize the external delay line.

V. Realisation

Figure 4 shows a photograph of the realised passive limiter using the UMS process. The total circuit measures about 1.3 x 1.9 mm^2.

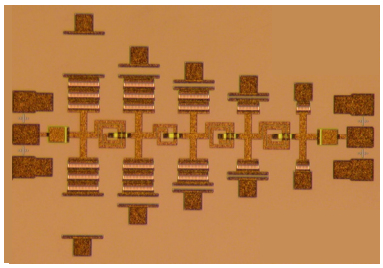

Figure 4 Passive limiter realised in the UMS PPH25x process

In figure 5 and 6 the passive limiters are presented that have been realised in the WIN PP50-10 process. The MMIC sizes are 1.2 x 3.0 mm^2 and 0.8 x 3.0 mm^2 respectively.

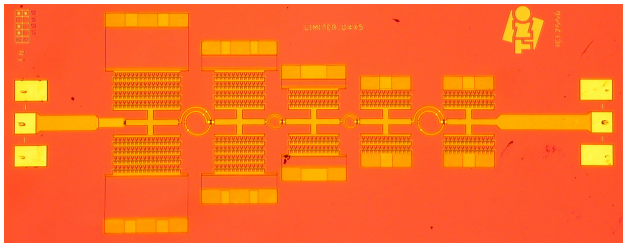

Figure 5 Passive limiter realised in the WIN PP50-10 process

In the modified limiter design, the diodes were adapted (from the foundry-standard layout) to include the effectively needed resistances, leading to a more compact limiter design with enhanced performance.

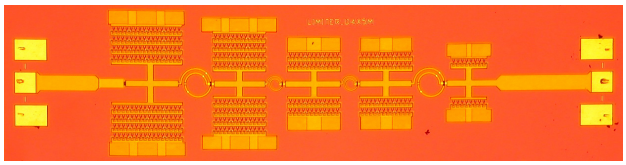

Figure 6 Modified passive limiter realised in the WIN PP50-10 process

In figure 7, a photograph of the realised active limiter with on-chip delay line is presented. This circuit measures 1.9 x 1.6 mm^2.

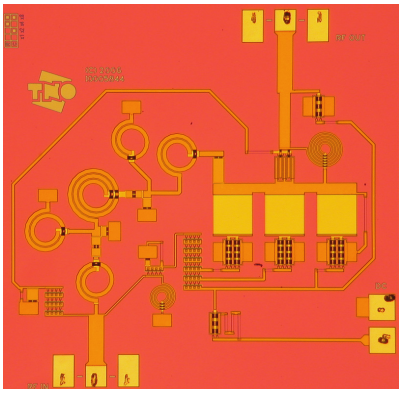

Figure 7 Active limiter MMIC realised in the WIN PP50-10 process

VI. Measured Performance

Both small-signal and high-power measurements were carried out on the limiters. The basic performance of the passive limiter realised in the UMS process is shown in figure 8, where both the absorptive behaviour and the limiter functionality are shown. The measurements were reasonably close to the (shown) simulated performance even though the foundry models used were not verified for these extremely high current and voltage levels.

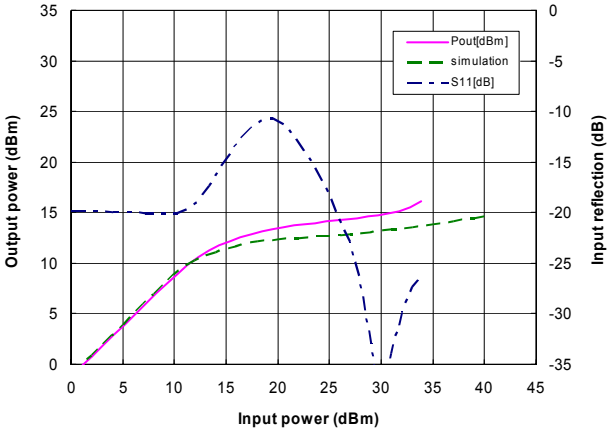

Figure 8 Passive limiter (UMS process) input reflection and output power versus input power at 10 GHz.

Figure 9 presents the measured power transfer curves of the designed passive and active limiters in the WIN process, for input powers up to and above 40 dBm. Clearly visible is the degradation of the performance of the passive limiters at input power levels above 35 dBm since the output power starts to increase rapidly.

In the active limiter, due to the fact that the output is effectively switched off at a certain input power level, the output power drops very fast, whereas in the passive limiters a more or less constant output power is generated.

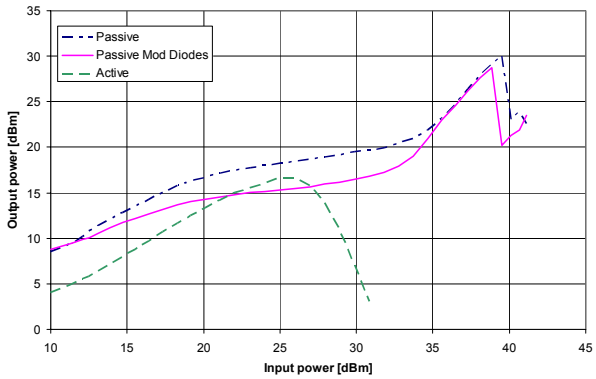

Figure 9 Transfer curves of active and passive limiters (WIN process), with standard diodes and modified diodes.

The small signal measurement results (S_{21} and S_{11}) are presented in Figure 10 and 11. It can be seen clearly in figure 8 that the active limiter has more insertion loss than the passive limiters, due to the losses in the 5th order band pass filter delay line.

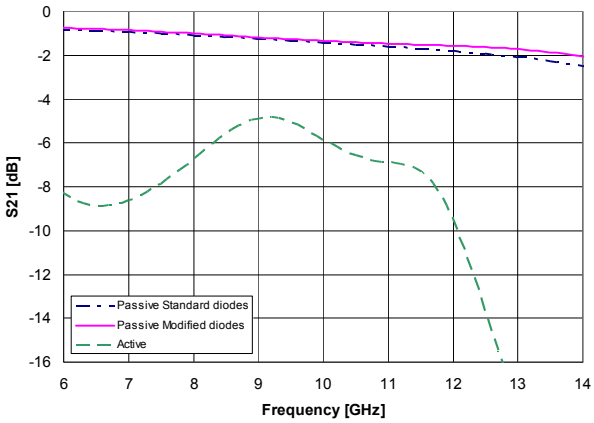

Figure 10 S21 of the designed limiters in the WIN process

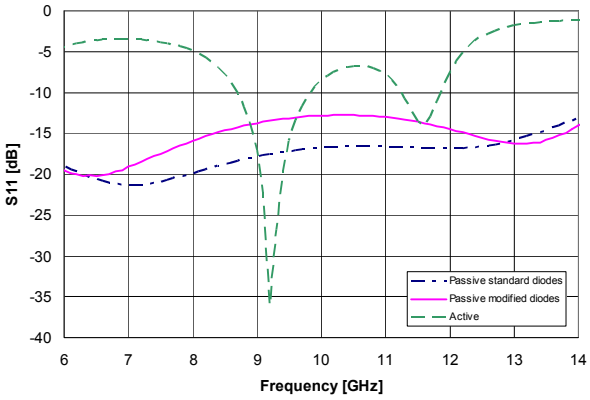

Figure 11 S11 of the designed limiters in the WIN process

Pulsed RF power measurements have been performed which show the fast response of the passive limiter. As an example, the measured RF pulse transfer characteristic of the modified passive limiter realised in the WIN process is shown in figure 12.

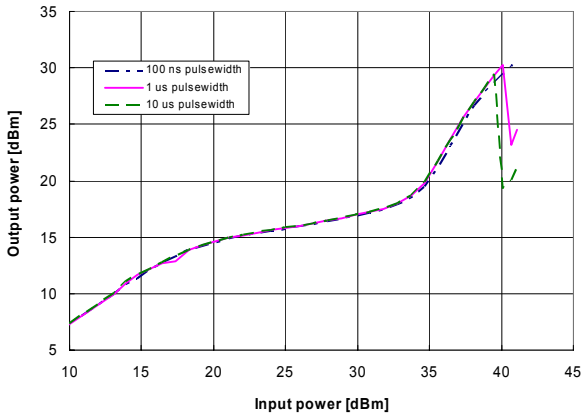

Figure 12 Pulsed RF transfer characteristic of the modified passive limiter realised in the WIN PP50-10 process

VII. EVALUATION

Evaluation of the measurements gave more insight in the observed output power increase at input levels above 35 dBm and the break down of the passive limiters. The passive limiters tend to break down above 39 dBm CW input power.

Figures 9 and 12 clearly show that the output power starts to increase rapidly until it drops after break down. These effects were not visible in the simulations using the foundry-supplied diode models ("model e" in figure 13).

Measurements of diode test-structures showed a current limiting effect of the diodes at voltages higher than 1.5 V across the diode. The diode model was modified to include this current limiting effect by curve-fitting of the diode measurement results. The "limiter model tanh" curve in figure 13 presents the limiter simulation result using the modified diode model.

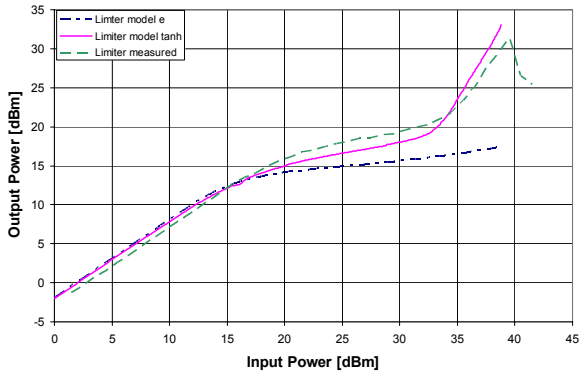

Figure 13 Comparison of the measurement result and simulation results with different diode models, for the passive limiter design in the WIN process.

VIII. CONCLUSION

A set of X-band distributed absorptive limiter GaAs MMICs has been successfully designed and realised. The measured performance shows the potential for these designs.

The active limiter shows promising results; it can withstand 10 Watt CW input power but at the cost of a relatively high small-signal loss

The passive limiter handles up to 4 Watts CW input power with low small-signal loss. For the passive limiter principle, an international patent application has been filed.

ACKNOWLEDGMENT

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