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# Ferroelectric switching of poly(vinylidene difluoride-trifluoroethylene) in metal-ferroelectric-semiconductor non-volatile memories with an amorphous oxide semiconductor

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Ferroelectric polarization switching of poly(vinylidene difluoride-trifluoroethylene) is investigated in different thin-film device structures, ranging from simple capacitors to dual-gate thin-film transistors (TFT). Indium gallium zinc oxide, a high mobility amorphous oxide material, is used as semiconductor. We find that the ferroelectric can be polarized in both directions in the metal-ferroelectric-semiconductor (MFS) structure and in the dual-gate TFT under certain biasing conditions, but not in the single-gate thin-film transistors. These results disprove the common belief that MFS structures serve as a good model system for ferroelectric polarization switching in thin-film transistors. © *2015 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4913920]

Ferroelectric materials have a spontaneous electrical polarization, which can be reversed by applying an electric field. The polarization can be retained after the biases are removed, provided the ferroelectric polarization charge is compensated for by for instance a metal or a semiconductor. This makes these materials useful for electronic nonvolatile memory devices. The last decade has witnessed a revival in the interest in polymer ferroelectric polymers such as poly(vinylidene difluoride-trifluoroethylene) (P(VDF-TrFE)).[1,2] P(VDF-TrFE) exhibits a high remanent polarization, a short switching time, and low process temperatures (120–140 °C).[3] As the mechanism of ferroelectric switching lies at the basis of the technological potential of these materials for use as non-volatile reprogrammable memories, polarization in P(VDF-TrFE)-based ferroelectric transistors (FeFETs) and metal-insulator-semiconductor (MIS) devices has been studied in combination with organic[4–9] as well as inorganic semiconductors.[10–16]

One of the main outstanding questions concerns the role of depolarization fields and compensation charges in determining the remanent ferroelectric polarization (the polarization remaining within the film after the removal of an external voltage) in the transistor channel. The remanent polarization is an important quantity, as the difference between the remanent polarizations of the two stable states is used to store information in a ferroelectric memory. When there is an inadequate supply of charge to compensate the polarization, a depolarization field develops that can significantly reduce the polarization available for information storage.[17,18] This can occur in ferroelectric transistors: the low carrier density in the semiconductor may result in insufficient charge near the ferroelectric/semiconductor interface, leaving a residual depolarization field. This field can lower ferroelectric polarization in the transistor channel and/or result in reduced data retention time.

Many groups have studied ferroelectric polarization/depolarization in MFS (metal-ferroelectric-semiconductor) diodes, assuming that the results translate directly to transistors. Furukawa *et al.* have reported that polarization reversal in Au/P(VDF–TrFE)/n-Si is impeded owing to the high depolarization field during the depletion of the semiconductor but is finally completed.[19] The polarization can be compensated by both the accumulation and inversion layers for silicon–semiconductor-based FETs. For unipolar semiconductor devices, Naber *et al.* have shown that polarization reversal in MFS diodes using organic poly(3-hexylthiophene) (P3HT) as a semiconductor layer does not progress after depleting the semiconductor, namely, switching between the polarized and depolarized condition, yielding one-half polarization changes.[20] This behavior was recently modeled.[21] On the other hand, Nakajima *et al.*[22] and Kam *et al.*[23] showed close to full polarization reversal in MFS diodes using a molecular semiconductor, pentacene. Similar studies using oxide semiconductors have not been reported until now, despite the fact that some of the best ferroelectric transistor memories reported are based on this novel class of semiconductors.[10,13,24–26] Considering the promising technological applications of these ferroelectric memories, we have conducted a systematic investigation of ferroelectric polarization switching of P(VDF-TrFE) in a series of progressively more complex device structures: from simple capacitors with and without additional dielectric interlayers, to MFS diodes and to single gate thin-film transistors (SG TFT) and dual gate thin-film transistors (DG TFT). In the latter device structures, indium-gallium-zinc oxide (IGZO) was used as the semiconductor material. We find that the ferroelectric can be polarized in both directions in the MFS structure and in the DG TFT under certain biasing conditions, but not in the SG TFT. These results disprove the common belief that MFS structures serve as a good model system for ferroelectric polarization switching in thin-film transistors.

MFM (metal-ferroelectric-metal), MFS, and transistors were fabricated using a P(VDF-TrFE) copolymer (77/23 %wt./wt., Mw 220kD) obtained from Solvay Specialty Polymers. Source-drain electrodes consisted of a 5 nm

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titanium adhesion layer followed by 25 nm of gold and were patterned using standard photolithography techniques. A 20 nm thick a-IGZO layer was RF-sputtered from an IGZO target with a 2:2:1 In:Ga:Zn metal ratio at 1 mTorr pressure at nominal room temperature. A partial pressure of oxygen in argon of 2% was maintained throughout the deposition in the sputter chamber. IGZO was annealed at 150 °C for 5 min in air. P(VDF-TrFE) films were prepared by spin coating a filtered 6 or 8 wt. % solution of P(VDF-TrFE) in cyclohexanone at a speed between 1000 and 2000 rpm for 60 s to obtain films with different thicknesses. The resulting films were annealed at 135 °C for 10 min in air. Finally, 50 nm thick gold top electrodes were evaporated through a shadow mask. All devices were fabricated on heavily doped n-type Si wafers with a 200 nm thermally oxidized $SiO_2$ layer (acting as bottom gate and gate insulator, respectively, in the dual gate transistor configuration).

Charge displacement versus voltage (D-V) hysteresis loops were measured at a hysteresis frequency of 100 Hz using an TF Analyzer 2000 from aixACCT and the so-called PUND scheme. The origin of D = 0 is calculated by averaging the maximum polarization, so at +/−20 V.

D-V hysteresis loops (Figure 1) were measured on MFM and MIFM capacitor structures, where M denotes Au electrodes (thickness 50 nm, evaporated), F is the ferroelectric polymer P(VDF-TrFE) copolymer (430 nm thickness in these structures), and I denotes a thin $Al_2O_3$ layer that was deposited by atomic layer deposition prior to spin coating of the P(VDF-TrFE) films from cyclohexanone. The thickness of the $Al_2O_3$ layer was varied from 0 to 10 nm. The 430 nm thick P(VDF-TrFE) film was annealed at 135 °C for 10 min in air.

For the MFM capacitor, i.e., no $Al_2O_3$ layer, the coercive field ($E_c$) is ca. 80 MV/m, similar to previously reported values.[8] The remanent ferroelectric polarization, or the polarization at zero applied voltage, $P_r$, equals 6.8 $\mu C/cm^2$, again in line with previously reported values. Insertion of a 2-nm-thick $Al_2O_3$ dielectric layer results in a slight suppression of the ferroelectric response. A 5-nm-thick and 10-nm-thick $Al_2O_3$ layer in series with the ferroelectric film causes a strong reduction in $P_r$, from 6.8 to 4.6 $\mu C/cm^2$ and 0.7 $\mu C/cm^2$, respectively (see Fig. 1). For these thicknesses, the hysteresis loop also becomes more skewed. Figures 2(b) and 2(c) illustrate the sensitivity of the remanent polarization to the $Al_2O_3$ thickness and the amount of compensating charge, respectively. $C_0/(C_0 + C_{ferro})$ is the fraction of polarization charge, P, that is compensated by charges in the electrodes.[17] Even when P is 98.5% compensated, the remanent polarization is reduced to 2/3 of its full value.

Figure 2 shows the D-V hysteresis loops of the MFS structures, where S is a 20 nm thick a-IGZO layer that was RF-sputtered from an IGZO target with a 2:2:1 In:Ga:Zn metal ratio. A partial pressure of oxygen in argon of 2% was maintained throughout the deposition in the sputter chamber. IGZO was annealed at 150 °C for 5 min. When a positive electric field is applied, the polarization switches from −P to +P abruptly and reacts similar to the MFM capacitor. IGZO is an n-type semiconductor, so the polarization charges are effectively compensated by the majority carriers in the accumulation layer when a positive bias is applied.. Meanwhile, the transition from +P to −P is skewed. Under negative bias conditions, the semiconductor layer is partially depleted. This results in a depletion layer acting as a capacitor in series with the ferroelectric insulator. The voltage needed to reverse the ferroelectric polarization will be higher because part of the electric field now drops over the (depleted) semiconductor layer: in our devices by ~5 V. The depletion width in turn also increases with increasing (negative) voltage (for an n-type semiconductor), leading to a less steep transition from +P to −P. The maximum difference in remanent polarization of the two states, $\Delta P_r$, of the MFS structure is 11.73 $\mu C/cm^2$, very close to the value of the MFM capacitor of $2 \times 6.8 = 13.6$ $\mu C/cm^2$. This suggests that the ferroelectric in the MFS structure is almost fully polarized in two stable states. When we compare the depolarizing effect of the 20 nm IGZO layer to that of the $Al_2O_3$, the 20 nm IGZO is equivalent to 3–4 nm $Al_2O_3$.

Transistor currents were measured as a function of top gate voltage ($V_{TG}$) for different values of the bottom gate voltage ($V_{BG}$). The $I_d$ - $V_{TG}$ (transfer curve) and $I_g$ - $V_{TG}$ characteristics measured at a source-drain bias of 0.1 V are presented in Figure 3 for different bottom gate biases. The counter-clockwise hysteresis in the drain current can be explained by polarization switching of the gate dielectric and its influence on the channel charge. The remanent polarization in the ferroelectric layer changes the charge carrier density of the semiconductor and produces distinctly different conductivity states at a given potential depending upon the degree and direction of polarization. The conductivity state

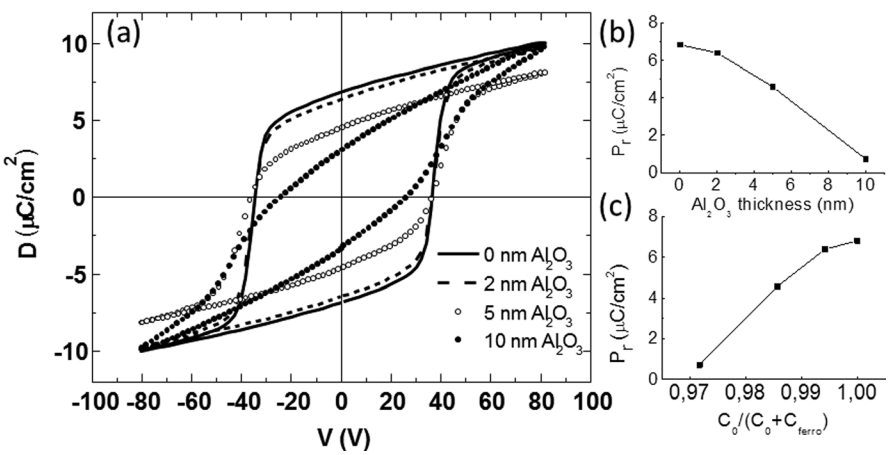


FIG. 1. (A) Electric displacement versus applied voltage (D-V) of bilayer P(VDF-TrFE)/$Al_2O_3$ capacitors, measured at 100 Hz. The $Al_2O_3$ layer thickness was varied from 0 to 10 nm. The thickness of the P(VDF-TrFE) films is 430 nm. Device area is 1.4 $mm^2$. (Right panels) Remanent polarization, $P_r$, as a function of $C_0/(C_0 + C_{ferro})$ where $C_0$ and $C_{ferro}$ correspond to the capacitance of the P(VDF-TrFE) (B) and $Al_2O_3$ layer (C), respectively.

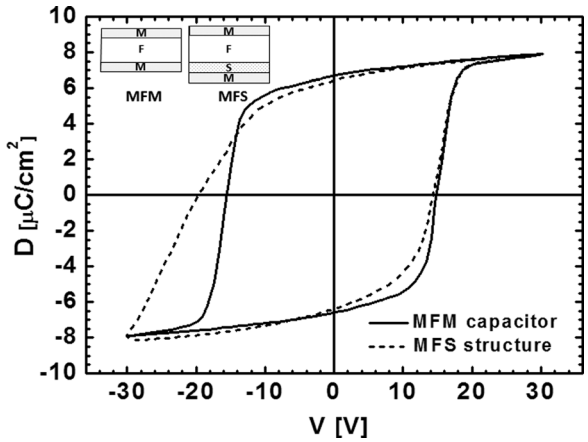


FIG. 2. Electric displacement versus applied voltage (D-V) of MFS structure with 20 nm IGZO and 430 nm P(VDF-TrFE), measured at 10 Hz. Device area was 0.46 mm$^2$. MFM capacitor data of Figure 1 are shown here again for comparison.

can be read out at a low voltage that does not disturb the ferroelectric polarization. Thus, FeFETs provide the advantage of non-destructive read-out (NDRO) functionality. This makes them particularly attractive.

When a negative bottom gate bias is applied, the bottom gate voltage modifies the charge carrier distribution in the channel accumulated by the top gate, and the transfer curve shifts to the right. The transition from OFF to ON becomes more abrupt. This effect has been previously seen in single-gate ferroelectric transistors and has been attributed to the formation of an injection barrier.[23] When a positive bottom gate bias is applied, the drain current remains higher, regardless of bottom gate voltage, than the corresponding curves recorded with negative bottom gate biases. This is most prominently seen when $V_{TG} < 0$ V but also holds for positive ($V_{TG} > 0$ V) top gate voltages. This leads us to the conclusion that a sufficiently positive bottom gate bias creates a second accumulation channel at the bottom interface. This creates the additional current. It effectively decreases the modulation between the ON and OFF state, but even for $V_{BG} = +60$ V, we observe counterclockwise hysteresis due to ferroelectric polarization reversal. These current-voltage characteristics are qualitatively similar to those of previous dual-gate ferroelectric ZnO transistors.[27] The aforementioned characteristics differ however in detail from other dual-gate IGZO transistors with P(VDF-TrFE) gate dielectrics.[28] In the latter case, the transfer characteristics could be shifted both towards positive and negative voltages. This resembles conventional (non-ferroelectric) dual gate transistors, where—in first order approximation—the shift in threshold voltage, $\Delta V$, is understood by a simple analysis of electrostatic potential and gate field induced charge carriers, so that $\Delta V$ is linearly proportional to the applied (second) gate voltage multiplied with the ratio of both gate dielectric capacitances. Although the exact reason of the different behavior remains elusive at this point, we can rule out that the bottom gate voltage strongly influences the (top-gate) voltage at which the ferroelectric switches based on an analysis of the measured gate currents (shown in Figures 3(b) and 3(d), and discussed in the next paragraph). Rather, we speculate that the ferroelectric polarization-induced channel charge of the transistor in the ON state is so high that it effectively overwhelms the electrostatic influence of the bottom gate voltage, effectively pinning the transition at which the drain current changes from high to low values. Upon scanning back from $V_{TG} = +20$ V the ferroelectric is polarized such that a high electron density is induced at the semiconductor-ferroelectric interface. A high current is measured. At a top gate bias around $-10$ V, the coercive field is reached, and the ferroelectric polarization changes sign. This explanation is in line with the analysis presented below.

Additional information can be obtained from the measured gate currents. When the polarization switches from one

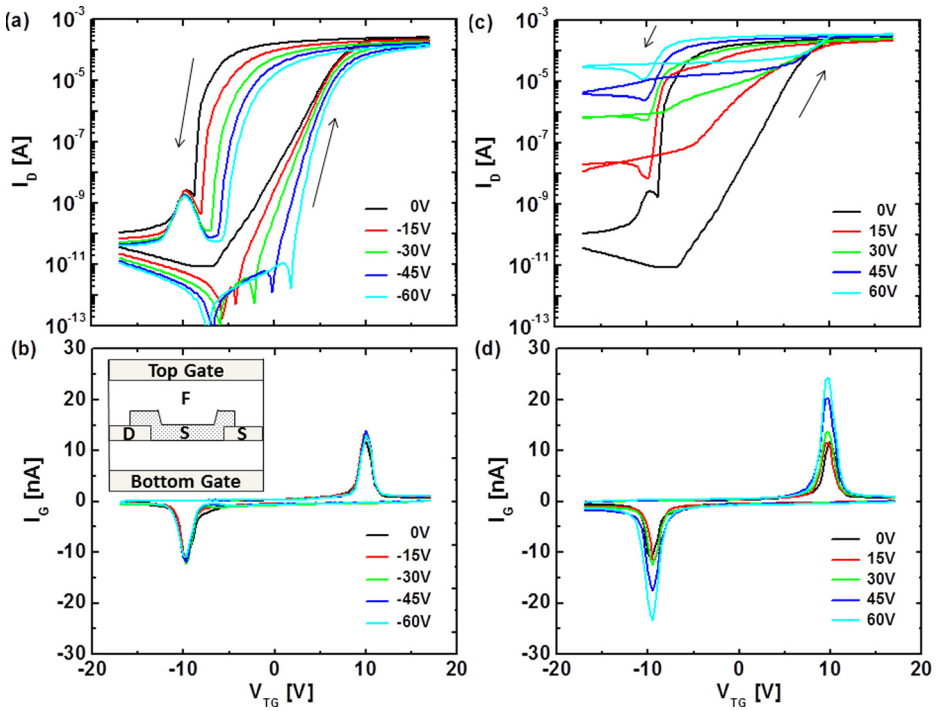


FIG. 3. Hysteretic drain current-voltage (VTG) ((a) and (c)) and gate current-voltage (VTG) ((b) and (d)) of dual gate IGZO (layer S) transistor with 200 nm thick $SiO_2$ bottom dielectric and 200 nm thick P(VDF-TrFE) (layer F) top dielectric. Currents were recorded by sweeping the top gate electrode from $-20$ V to 20 V and back to $-20$ V for different constant values of bottom gate voltage, mentioned in the legend. $I_G$ is the current supplied through top electrode. Measurements with positive and negative $V_{BG}$ are displayed in different panels for the sake of clarity. The curves were recorded at a drain bias of 0.1 V. Channel width and length were 40 $\mu$m and 5 $\mu$m, respectively. Width of the source and drain electrodes was 5 $\mu$m. Arrows in (a) and (c) show the direction of hysteresis.

state to the other, charge is displaced across the ferroelectric insulator. The accompanying switching currents are observed as sharp features in the gate current, $I_G$. The position of the switching peak in gate current does not change with $V_{BG}$. This illustrates that the switching voltage is independent of the second (bottom) gate potential. It is only related to the coercive electric field and layer thickness of the P(VDF-TrFE) gate dielectric. For negative bottom-gate voltages, the height of the switching peak is constant. For positive bottom-gate voltages, however, it increases, suggesting an increase in total switching charge. We attribute this increase to an increase in ferroelectric polarization due to the formation of the (second) accumulation layer in the semiconductor. Up to $V_{BG}$ of +60 V, no sign of saturation is seen, suggesting partial channel polarization.

Enhanced polarization of the channel can be rationalized in at least two ways. First, as a result of the formation of the bottom accumulation channel, more charge carriers are available as counter images to stabilize ferroelectric polarization. Second, the bottom accumulation layer effectively causes the electric field to orient essentially in the vertical direction, as in the MFS diodes, resulting in lower voltage drop across the semiconductor and thus depolarization field. It is in principle possible that the charges in the bottom accumulation layer compensate the ferroelectric polarization directly. This is however unlikely. These charges form within the IGZO film close to its interface with the bottom gate dielectric. They are therefore spatially separated from the P(VDF-TrFE) film by the bulk of the IGZO film that has a total thickness of 20 nm. A residual depolarization field will therefore develop similarly as in the MFS structure. We have seen however that this lowers the remanent polarization by only 5%. We therefore believe that the enhanced channel polarization is primarily the result of field line redistribution by the formation of the second bottom channel rather than direct compensation of the ferroelectric polarization by the additional charges. These observations can explain some of the controversy reported in literature in relation to switching mechanism and state of the polarization in the channel in transistors.

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