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Dielectric interface-dependent spatial charge distribution in ambipolar polymer semiconductors embedded in dual-gate field-effect transistors

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The spatial charge distribution in diketopyrrolopyrrole-containing ambipolar polymeric semiconductors embedded in dual-gate field-effect transistors (DGFETs) was investigated. The DGFETs have identical active channel layers but two different channel/gate interfaces, with a CYTOP™ organic dielectric layer for the top-gate and an octadecyltrichlorosilane (ODTS) self-assembled monolayer-treated inorganic SiO_2 dielectric for the bottom-gate, respectively. Temperature-dependent transfer measurements of the DGFETs were conducted to examine the charge transport at each interface. By fitting the temperature-dependent measurement results to the modified Vissenberg–Matters model, it can be inferred that the top-channel interfacing with the fluorinated organic dielectric layers has confined charge transport to two-dimensions, whereas the bottom-channel interfacing with the ODTS-treated SiO_2 dielectric layers has three-dimensional charge transport. *Published by AIP Publishing.* [http://dx.doi.org/10.1063/1.4960096]

Solution-processable organic ambipolar semiconductors, wherein both *p*- and *n*-type charge transport can occur, are attracting significant research interest because of their advantages that potentially allow easy fabrication of light-emitting transistors or inverting logic circuits.[1–5] A promising class of organic materials for such ambipolar characteristics is based on diketopyrrolopyrrole (DPP)-containing copolymers that consist of DPP-acceptor and a large variety of donor blocks and exhibit a high mobility up to $>10\,cm^2/V\,s$, as has been reported by several groups.[6] An improved understanding of the physical properties of ambipolar charge transport is required in order to expedite progress in the performance of DPP-based organic electronic applications. For this purpose, Kronemeijer *et al.* recently reported the confined two-dimensional charge-transport behavior in top-gated field-effect transistors, wherein organic gate dielectrics were located on the top of the semiconducting layers, and several polymeric semiconductors, including DPP-based polymers, were used as active channel materials.[7] However, their results contradicted those reported by Brondijk *et al.*, who observed that SiO_2 bottom-gated field-effect transistors with polymer semiconductor films are well-described by the three-dimensional charge transport model.[7,8]

In order to address these conflicting observations, we study the charge transport properties of DPP-based ambipolar semiconducting polymers embedded in dual-gate field-effect transistors (DGFETs) comprising two separate dielectric/semiconductor interfaces in a single transistor.[9,10] In fact, the DGFET structure is the best platform for studying the effects of different dielectrics upon device performance with minimal influence from external parameters, such as sample-to-sample variation, because the devices share an identical active semiconductor layer.[9,10] In the present work, we perform temperature-dependent transfer-curve measurements on the DGFETs in the range of 120–260 K. Based on these measurements, we analyze the spatial charge-transporting behavior of holes in the active DPP-based semiconducting layer interfacing with the organic top-gate (TG) and SiO_2 bottom-gate (BG) dielectric layers. We also correlate key charge-transport parameters with the dielectric layers that we have studied.

Figure 1(a) shows a schematic of the DGFETs and the chemical structure of poly[(diketopyrrolopyrrole)–*alt*–(2,2′-(1,4-phenylene)bisthiophene)] (PDPPTPT) used as an active channel layer.[11,12] Fabrication of the DGFETs starts with a heavily doped (n^{++}) Si substrate that also serves as a bottom-gate electrode. On the top of the Si substrate, a 200 nm-thick silicon dioxide (SiO_2, $\varepsilon_r = 3.9$) dielectric layer with a capacitance of 17 nF/cm^2 is thermally grown. For the source and drain (S/D) electrodes, a 30 nm-thick gold (Au) layer with a

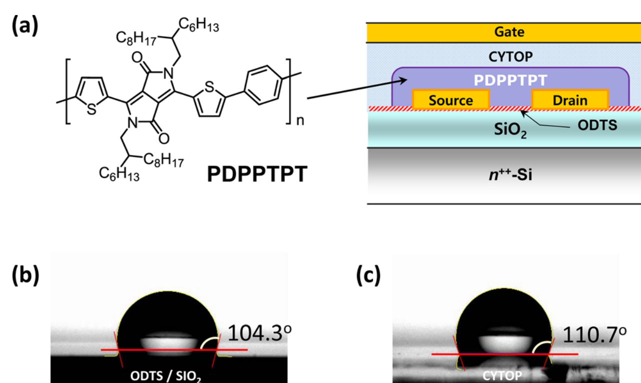

FIG. 1. (a) Schematics of the transistor and the chemical structure of the PDPPTPT used in this study. Deionized water contact angles with (b) ODTS-treated SiO_2 and (c) CYTOP surfaces.

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5 nm-thick titanium (Ti) adhesion layer is thermally evaporated onto the SiO_2 surfaces and photolithographically patterned. The width and length of the comb-shaped interdigitating S/D electrodes are 5 mm and 10 μm, respectively.

To passivate hydroxyl groups on the SiO_2 surfaces that are known to act as electron-trap sites, the substrate is immersed in a 10 mmol octadecyltrichlorosilane (ODTS)-concentrated *n*-hexane solution for 30 min after UV-ozone cleaning. The substrate is then rinsed with ethanol and baked for 30 min at 120 °C in ambient air to accelerate the surface reaction. The ODTS monolayer on top of the SiO_2 surfaces has a contact angle of >104°, as shown in Figure 1(b). Next, the PDPPTPT (synthesized according to a previously reported procedure[11]) is spin-coated from a 10 mg/ml solution in hot chloroform, and the semiconducting polymer films are annealed at 200 °C for 30 min in the glove box with an atmosphere <0.1 ppm oxygen and water. The PDPPTPT-based polymer film's thickness, as measured by atomic force microscopy, is ~50 nm. Subsequently, a fluorinated polymer, CYTOP™ ($\varepsilon_r = 2.1$, purchased from Asahi Glass Co.) is spin-coated and annealed at 150 °C in vacuum for 24 h to be used as a top-gate dielectric layer. The thickness of the CYTOP dielectric layer is ~750 nm, resulting in a capacitance of ~2.4 nF/cm^2, and the surface of the CYTOP layer has a contact angle of >110° (Figure 1(c)), which indicates the highly hydrophobic state of the CYTOP surface. Finally, the top-gate electrode is applied by thermally evaporating Au (50 nm) through a shadow mask. The DGFETs were characterized using a Keithley 4200-SCS semiconductor analyzer connected to a Desert Cryogenics vacuum probe station with a chamber pressure below 10^{-3} Torr at room temperature (RT).

The electrical characteristics of the DGFETs are shown in Figure 2. For both the TG and BG channels, the typical transfer and output characteristics of ambipolar operating behavior are observed. In particular, Figures 2(a) and 2(b) show the transfer characteristics of both channels for positive and negative drain biases (V_D), which have symmetric V-shaped curves indicating the transition from *n*- to *p*-type and vice versa. A large ON/OFF ratio of $>10^4$ at $|V_D| = 20$ V for both channels is found in their transfer curves. From the slope of negative V_G *vs.* $\sqrt{|I_D|}$, the hole-mobility of the saturation region is calculated to be ~0.39 and ~0.06 cm^2/V s for the TG and BG channels, respectively, and the electron mobilities extracted from the slope of positive V_G *vs.* $\sqrt{|I_D|}$ are ~0.18 and ~0.06 cm^2/V s for TG and BG, respectively. For both hole and electron transport, the charge-carrier mobility in the TG channel is more than three times higher than that in BG channel, although the thermally grown SiO_2 BG dielectric has a higher capacitance value compared with the CYTOP TG dielectrics, resulting in a substantially larger field-induced charge density in the BG channel. The origin of the different charge carrier mobilities will be discussed later. Figures 2(c) and 2(d) show the output characteristics with proper saturation at high gate biases. However, particularly for the electron-accumulation mode, we also observe a super linear drain current increase at low gate biases ($|V_G| \leq 50$ V).[13] In this bias condition, the minority carriers (i.e., holes in the *n*-type mode and electrons in the *p*-type mode) flow dominantly as the drain also works as a source when the $|V_{GD}|$ is larger than $|V_{GS}|$.

In order to further examine the charge transport, temperature-dependent transfer-measurements were conducted on the PDPPTPT-based DGFETs in the range of 120–260 K. Figures 3(a) and 3(b) show the measured temperature-dependent transfer curves at a V_D of -40 V in the TG and BG channels, respectively. We note that the drain currents of the output curves shown in Figures 2(c) and 2(d) display a non-linearity at low drain-bias conditions (i.e., in the linear regime) due to poor charge injection that is generally found in DPP-containing polymer-based ambipolar transistors with single Au S/D contacts.[5] Therefore, we measure the drain currents of the DGFETs in the saturation region of $V_D = -40$ V to minimize potential errors. As expected in thermally activated transport, the charge-carrier mobilities of both electrons and holes increase with increasing temperature. Figures 3(c) and 3(d) show plots of the charge-carrier mobility versus inverse temperature for both hole- and electron-accumulation modes with

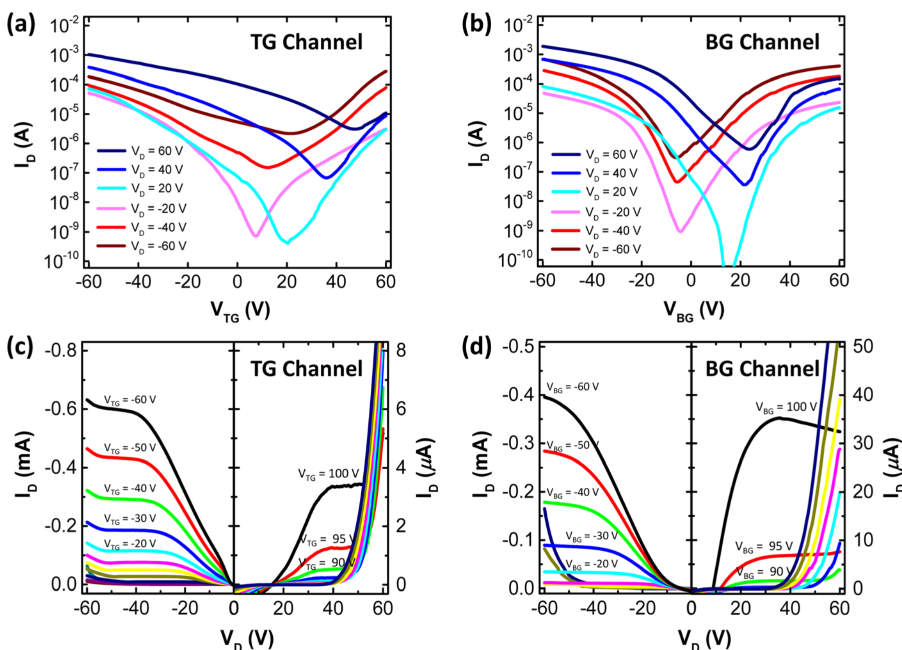

FIG. 2. Transfer characteristics of (a) the TG channel and (b) the BG channel at different source-drain bias conditions. Output characteristics of (c) the TG channel and (d) the BG channel.

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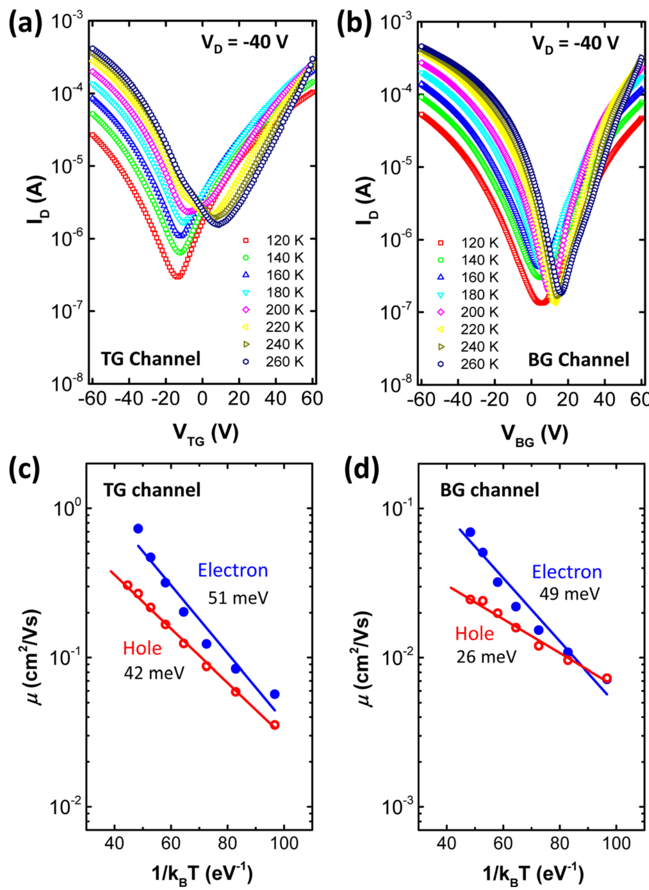

FIG. 3. Temperature-dependence of the transfer characteristics at $V_D = -40$ V of (a) the TG channel and (b) the BG channel in the ambipolar DGFETs. The plots of the saturation mobilities of both holes and electrons as functions of inverse temperature in (c) the TG channel and (d) the BG channel.

applied gate biases (depending upon polarity). The activation energies extracted from the Arrhenius plots are determined to be 42 meV for holes and 51 meV for electrons in the TG channel and 26 meV for holes and 49 meV for electrons in the BG channel. For both channels, the activation energy for electron transport of ~50 meV is higher than for holes, as expected from their mobility values. A higher activation energy for electrons compared with holes in polymer semiconductors has been previously reported;[14] however, in this case, it is attributed to the relatively poor injection efficiency of electrons due to the non-linearity of the drain currents shown in the output characteristics (Figures 2(c) and 2(d)).

For further analysis of the charge transport in the PDPPTPT-based polymeric semiconductor films, we apply the Vissenberg–Matters model to the measured temperature-dependent transfer characteristics.[15] Vissenberg and Matters derived their analytical model to express the conductivity in organic field-effect transistors using percolation theory and the concept of variable range hopping (VRH) in an exponential density of localized states. Note that the exponential density of states (DOS) used in the analytical model is an empirical simplification of a Gaussian DOS that better represents disordered organic semiconductors. However, despite this limitation stemming from a lack of physical meaning, the Vissenberg–Matters model has been successfully applied to interpret the charge-transport phenomena in organic semiconductors.[16–18] The analytical model originally employed a three-dimensional carrier density profile in the accumulation layer that decreases quadratically with distance from the dielectric.[15] For the analysis of self-assembled monolayer transistors, however, Brondijk *et al.* revised the analytical model with a two-dimensional carrier-distribution profile in the accumulation layer of the transistor, in which the charge density is constant up to a certain limited thickness from the dielectric.[7,8] Recently, Kronemeijer *et al.* modified the Vissenberg–Matters model again to be appropriate to the charge transport in the saturation regime of the transistors as follows:[7]

$$I_D^{2D} = A\frac{W}{L}d_{sc}^{1-(T_0/T)}\left(\frac{C_i}{e}\right)^{T_0/T}\frac{T}{T_0+T}(V_G-V_t)^{(T_0/T)+1}, \quad (1)$$

$$I_D^{3D} = \frac{A}{e}\frac{W}{L}\left(\frac{1}{2K_bT_0\varepsilon_0\varepsilon_r}\right)^{(T_0/T)-1}C_i^{2T_0/T-1} \times \frac{T}{2T_0}\frac{T}{2T_0+T}(V_G-V_t)^{2T_0/T}, \quad (2)$$

with

$$A = \sigma_0\left(\frac{\left(\frac{T_0}{T}\right)^4\sin\left(\pi\frac{T}{T_0}\right)}{(2\alpha)^3B_c}\right)^{T_0/T}, \quad (3)$$

where T_0 is the characteristic width of the exponential density of states, α^{-1} is the wave-function overlap localization length, σ_0 is a conductivity prefactor, and B_c is the critical number for the onset of percolation. The parameter d_{sc} is the thickness of the confined two-dimensional charge sheet. More importantly, the above complicated equations are reduced to an approximate power-law dependence of the source-drain current on the gate voltage without the Taylor expansion. Consequently, both the two- and three-dimensional models lead to direct power laws, i.e., $I_D \propto a\,(V_G–V_t)^{\gamma}$, where a is a fitting constant that comprises several physical parameters (e.g., A in Equation (3) and device geometry factors) and the exponent γ is a function of temperature (e.g., $\gamma_{2D} = (T_0/T) + 1$ and $\gamma_{3D} = 2T_0/T$ in the saturation regime), which carries information about the spatial charge-transport behavior.[7,8]

Figures 4(a) and 4(b) show plots of the temperature-dependent transfer curves on a double logarithmic scale for the TG and BG channels, respectively. We note that there are instability of the turn-on voltages and drain-gate leakage currents that are slightly greater than the source-drain currents at the elevated temperature for the electron-accumulation mode.[19] For this reason, only hole-transport is analyzed using the modified Vissenberg–Matters model. Solid lines are obtained for all temperatures by fitting the measured data to the reduced power-law dependence of the source-drain current as a function of the gate-overdrive voltage ($V_G - V_t$), where the V_t values were -1.5 V and -11 V for the TG and BG channels, respectively. The γ value is also extracted from the measured transfer curve for each temperature and is then plotted against inverse temperature ($1/T$).[7,8,15] Figure 4(c) shows the γ versus $1/T$ plots constructed for both the TG and BG channels. The extrapolated line of the TG channel crosses the exponential axis at a value of 1, indicating that the two-dimensional charge-carrier profile is presented in the top-channel, whereas the extrapolated line of

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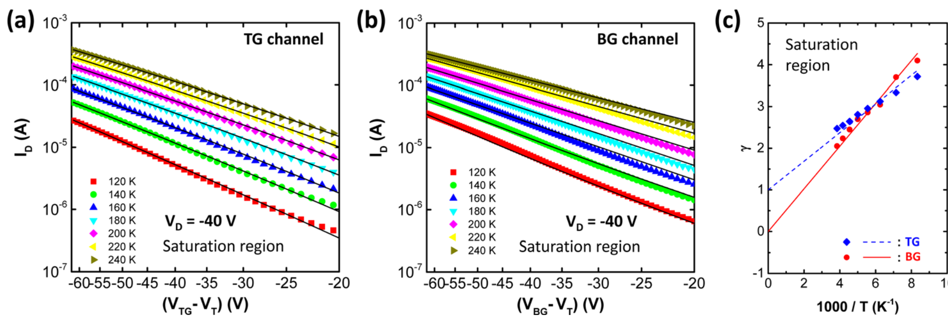

FIG. 4. Replotted transfer characteristics of (a) the TG channel and (b) the BG channel on a double-logarithmic scale. Black solid lines are fits to extract the parameter, γ, for each temperature. (c) Extracted values of γ for the TG and BG channels plotted against inverse temperature. The extrapolated dashed linear fit yields the intersection with the exponential axis.

TABLE I. Summary of key charge transport parameters: room-temperature mobility μ_{RT}, activation energy E_a, width of the density of localized states k_BT_0, and information about the dielectric layers.

		Electron		Hole		
Channel	Dielectric (ε_r)	μ_{RT} (cm^2/V s)	E_a (meV)	μ_{RT} (cm^2/V s)	E_a (meV)	k_BT_0 (meV)
Top	CYTOP (2.1)	0.18	51	0.39	42	29.5
Bottom	SiO_2 (3.9)	0.06	49	0.06	26	44.1

the BG channel has an exponential axis intercept of $\gamma = 0$, which means that the three-dimensional profile is proper for describing the charge carrier distributions in the bottom-channel.[7] A summary of key charge transport parameters and information about the dielectric layers is presented in Table I, where we use fluorinated organic layers with a relatively low dielectric constant for the TG-insulating materials and ODTS-treated SiO_2 dielectrics, which have dielectric constants that are almost two times higher than those of the organic layers used as BG dielectric layers. Given the fact that the surface of the ODTS-treated SiO_2 is hydrophobic, as confirmed with the contact angle measurement (Figure 1(b)), we assume that the interfacial states of both channels have similar quality; thus, we infer that differences in the electrostatic interaction with the gate dielectric arise from the different dielectric constant values of the TG- and BG-dielectric layers. Therefore, the difference in the spatial charge distributions may originate from the different gate dielectric layers affecting the active channel, resulting in a substantial broadening of the density of the localized states (dipolar disorder).[8,20,21] This interpretation is also supported by the values of T_0 (i.e., the characteristic width of the exponential density of states) extracted from the slopes of the linear fits in the γ *vs.* $1/T$ plots. However, the higher charge-carrier mobility of the TG channel with higher thermal activation energy could not be explained. Compared with the ODTS-treated SiO_2 dielectrics, the fluorinated organic CYTOP layer with a low dielectric constant induces a relatively small number of charge carriers in the TG channel under the same bias condition onto the BG dielectric layer. Although this small number of charges is insufficient to fill the adjacent trap sites and leads to a higher thermal activation energy, the narrow width of the density of the states resulting from the electrostatic interactions with the low-k organic TG dielectrics allows an efficient hopping process of the induced charges; this results in the higher charge-carrier mobility of the TG channel[8,20–22]

In summary, we have investigated the spatial charge transporting properties in a PDPPTPT-based ambipolar polymeric semiconductor embedded in a DGFET consisting of two separate dielectric/semiconductor interfaces in a single transistor. Temperature-dependent measurement results on the TG channels interfacing with the low-dielectric constant organic fluorinated insulating layer are compared with the results obtained from the BG channel contact with ODTS-treated SiO_2 dielectrics. The modified Vissenberg–Matters model indicates that the top-channel has a two-dimensional charge-distribution profile, whereas the bottom-channel has a three-dimensional charge distribution.

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