A cost-effective 10 Watt X-band High Power Amplifier and 1 Watt Driver Amplifier Chip-set

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***Abstract* — An X-band power amplifier chip-set for communication and radar applications has been developed and tested. The chip set consists of a two- and three-stage high-power amplifier, which have an output power of 10 Watt over the 8.5 – 10.5 GHz frequency band and a driver amplifier with an output power of more than 1 Watt over the 8.5 – 11.5 GHz frequency band. The amplifiers have been developed in the 6-inch 0.5 µm power pHEMT process (PP50-10) of WIN Semiconductors. The use of this process in combination with the used innovative design approach results in a cost effective chip set, which is competitive in both performance and price with any available solution.**

I. Introduction

High-Power Amplifiers (HPAs) are crucial for a rapidly increasing number of systems ranging from mobile communication to radar systems. This paper describes the development and performance of such HPAs in a cost-effective high volume GaAs process. A requirement from the start of the design work was the demand that the power amplifier chip-set should be usable in both existing Transmit Receive (TR) modules and two-chip TR modules that are currently under development by TNO. The latter TR modules consist of the in this paper discussed HPAs in combination with a core-chip [1], which controls the amplitude and the phase of the RF signal in both the receive and transmit mode.

A two-stage and a three-stage HPA have been developed to be able to support different TR module topologies. In addition, a driver amplifier has been developed. The design and measurement results of these amplifiers will be discussed in the next sections.

II. PP50-10 power HEMT technology

The amplifier designs have been realized with the help of the PP50-10 power pHEMT process of WIN Semiconductors, which has a gate length of 0.5 µm. The amplifiers have been realized on 100 µm thick substrates. The use of this process is attractive because of the 6" wafer size and good reproducibility resulting in a high-yield and a relatively low price per amplifier.

At 10 GHz the PP50-10 process has an output power density of approximately 650 mW/mm, a PAE of 54% and a gain of 10.5 dB at the 3-dB compression point. These results are given at the load impedance, which gives a compromise between maximum output power and maximum power added efficiency.

The output power density was measured for samples coming from two different wafers, see figure 1.

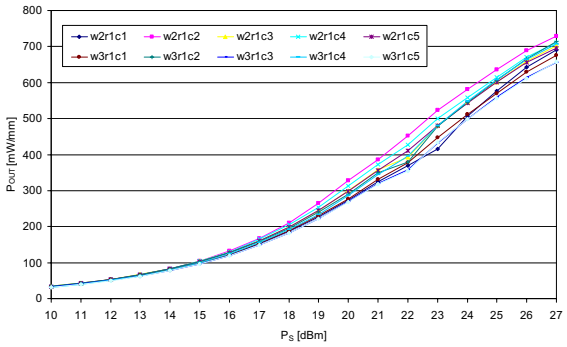

Fig. 1. Output power density of a 8x150 µm transistor measured at f=10 GHz, V_{DS}=8 V, V_{GS}=-0.8 V and Γload=0.5/143°.

III. Amplifier design

The discussed amplifier designs have been based on a transistor, which has 8 gate fingers with a gate width of 150 µm. This transistor has groups of four fingers that are spaced 19 µm apart. Those groups of four fingers are surrounded by source viaholes, see figure 2. This results in a very compact transistor layout.

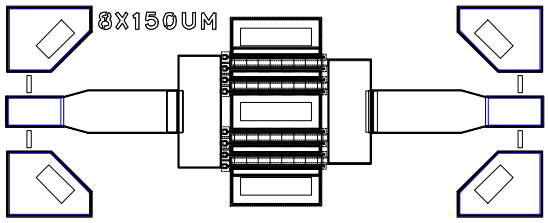

Fig. 2. Layout of transistor used in amplifier design.

A potential drawback of this compact transistor layout is the maximum channel temperature, which might become too high. Therefore, a careful thermal analysis [2] and bias point selection has been performed at the start of the amplifier designs. The results of this analysis have been depicted in figure 3 for various ambient temperatures and power dissipations. A maximum channel temperature of 150 °C at an ambient temperature of 90 °C was considered the upper limit for a reliable

operation of the transistor. This results in an MTTF of more than 10^7 hours. The gate bias supply voltage was selected in such way that the dissipated power remains below the 600 mW over the entire input power range.

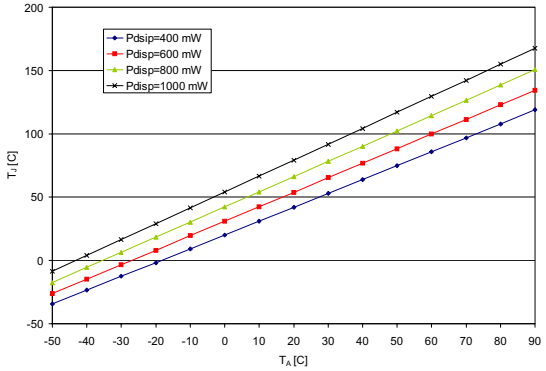

Fig. 3. Maximum channel temperature of two 8x150 µm transistors in parallel.

As next step in the design, the optimum load impedance was determined with the help of load-pull measurements. For the HPAs a topology is used, which uses 16 transistors in parallel in the output stage. For the three-stage amplifier and the driver amplifier a load impedance that gives a compromise between output power and efficiency has been used. The two-stage amplifier uses a load, which reduces the total drain current for the amplifier to a value of less than 4 A. As a result, the output power of the two-stage amplifier is 1 dB lower than that of the three-stage amplifier.

During the design, special emphasis has been put on the stability of the individual transistors and the complete amplifier. Stability enhancement techniques have been used [3] resulting in from an RF point of view unconditionally stable amplifier design. In addition, the stability via the bias supplies has been improved.

The matching networks have been designed with the techniques discussed in [4] and have been completely optimized with the help of an electromagnetic field simulator.

The gate bias of the amplifiers is provided with the help of an active gate-bias circuit, which is able to compensate 75% of the effect of threshold voltage variations. The use of TaN thin film resistors, which have a negative temperature coefficient, results in a gate-bias circuit that also partly compensates for temperature variations.

IV. Three-stage 10-Watt HPA performance

The three-stage HPA has 16 transistors in the output stage, 8 transistors in the second stage and 2 transistors in the first stage, see figure 4. These stages have a total gate width of respectively 19.2, 9.6 and 2.4 mm.

The measurement results as have been depicted in figure 5 show an excellent average output power of 10 Watt over the 8.5-10.5 GHz frequency band. The depicted results are coming from four different wafers. All results discussed in this paper have been measured with a pulse repetition frequency of 10 kHz, a pulse width of 10 µs and an ambient temperature of 25 °C.

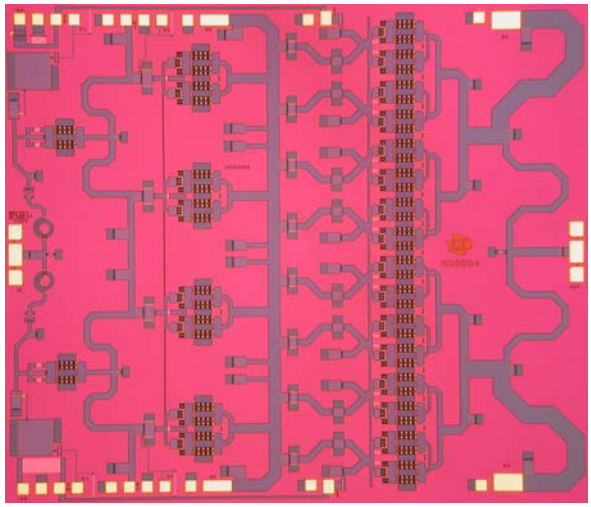

Fig. 4. Three-stage HPA (chip size: 5.0x4.3 mm^2).

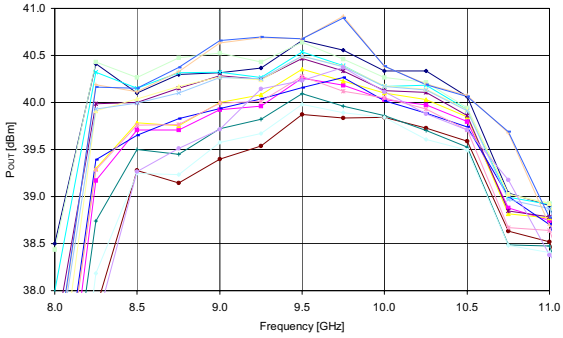

Fig. 5. Output power of three-stage amplifier measured at V_{DS}=8 V and P_S=19 dBm.

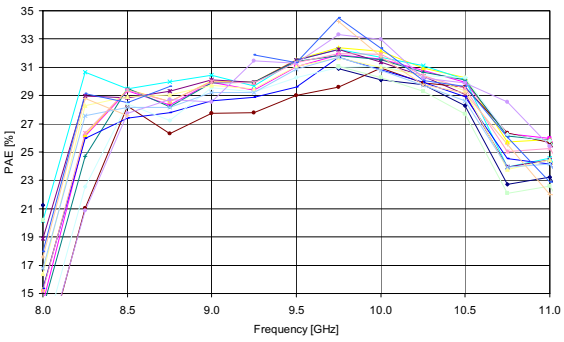

Fig. 6. Power Added Efficiency of three-stage amplifier measured at V_{DS}=8 V and P_S=19 dBm.

The measured performance as function of temperature shows a small-signal gain variation of -0.04 dB/°C, a PAE variation of -0.08 %/°C and an output power variation of -0.015 dB/°C.

The variation of the large-signal performance has also been measured as function of time. The obtained measurement results are depicted in figure 7. The power amplifier has been tested for a period of 144 hours under full RF operating conditions. The measurements have been performed under pulsed measurement conditions and temperature that have been mentioned before. The

depicted results show an encouraging low output power variation of approximately 0.1 dB. The measured drain current shows a corresponding variation of less than 3 % over the depicted period. The PAE varies over this period with approximately 0.5%.

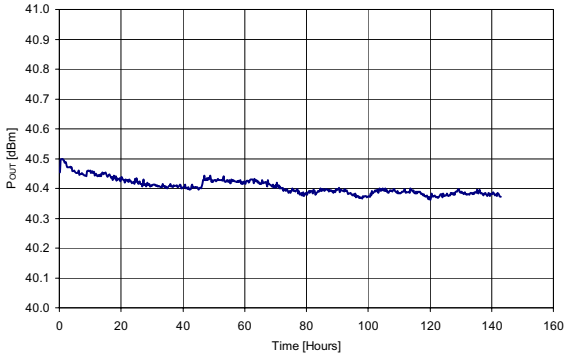

Fig. 7. Output power as function of time of a three-stage amplifier measured at f=9.75 GHz, V_{DS}=8 V and P_S=19 dBm.

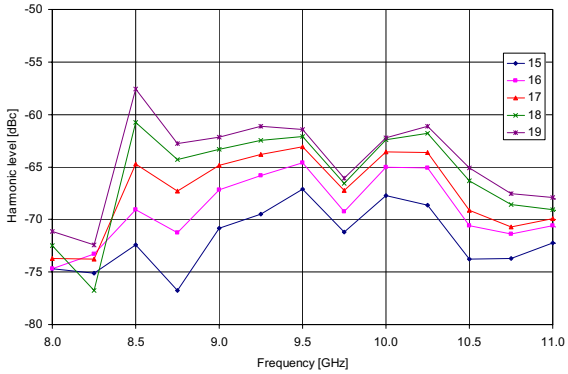

Fig. 8. Measured second harmonic output power level of the three-stage amplifier. The measurements have been performed at V_{DS}=8 V and source powers ranging from 15-19 dBm.

In figure 8 the second harmonic power level is shown for various source power levels. From the depicted results can be seen that the second harmonic level is lower than -55 dBc over the entire frequency range.

Mimix Broadband [5] is currently performing the industrialisation of the discussed three-stage power amplifier.

V. Two-stage 10-Watt HPA performance

The two-stage HPA also has 16 transistors in the output stage and 8 transistors in the first stage, see figure 9. These stages have a total gate width of respectively 19.2 and 9.6 mm. The two-stage amplifier has been designed for a 1 dB lower output power to keep the drain current to a value below 4 A. The measured output power has been depicted in figure 10. The results show the expected average output power of 8 Watt. The depicted results are coming from two different wafers. These wafer are different from the ones on which the three-stage amplifiers were realized. The measured PAE is depicted in figure 11.

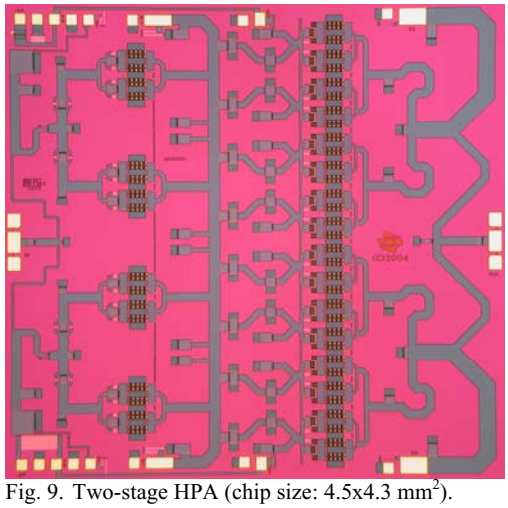

Fig. 9. Two-stage HPA (chip size: 4.5x4.3 mm^2).

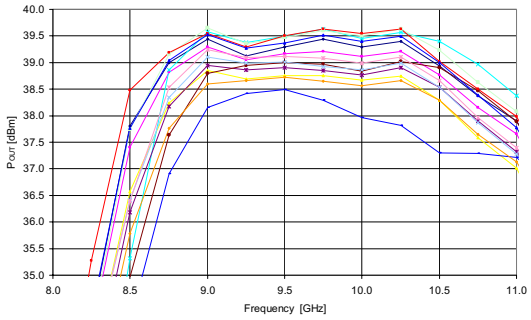

Fig. 10. Output power of two-stage amplifier measured at V_{DS}=8 V and P_S=23 dBm.

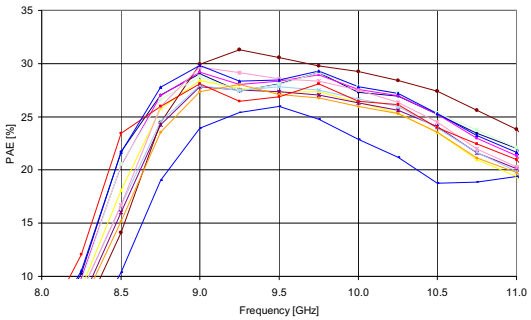

Fig. 11. Power Added Efficiency of two-stage amplifier measured at V_{DS}=8 V and P_S=23 dBm.

It is expected that the variation of the output power and PAE as function of temperature of the two-stage amplifier is similar to the measured numbers of the three-stage amplifier given in the previous section. The small-signal gain variation will be less (≈ -0.03 dB/ °C) because of the lower number of amplifier stages.

VI. Driver amplifier performance

For the driver amplifier design two transistors with a total gate width of 2.4 mm have been used in the output stage. In the first stage a 1.2 mm transistor is used, see figure 12. The measured output power and power added efficiency have been depicted in respectively figure 13 and 14. The results show an output power of more than 1 Watt over the 8.5-11.5 GHz frequency band. In addition,

an excellent power added efficiency between 35-45% has been measured.

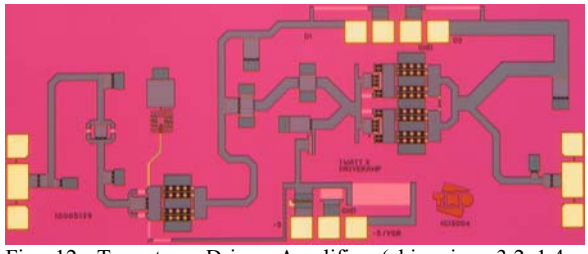

Fig. 12. Two-stage Driver Amplifier (chip size: 3.2x1.4 mm^2).

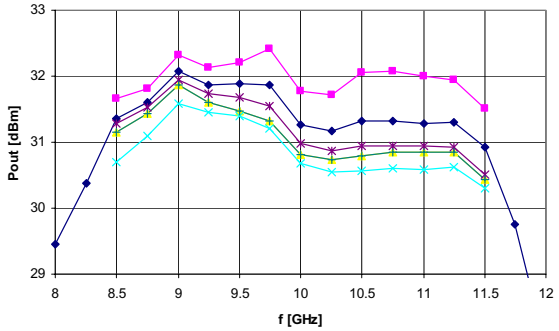

Fig. 13. Output power of the Driver Amplifier measured at V_{DS}=8 V and P_S=17 dBm.

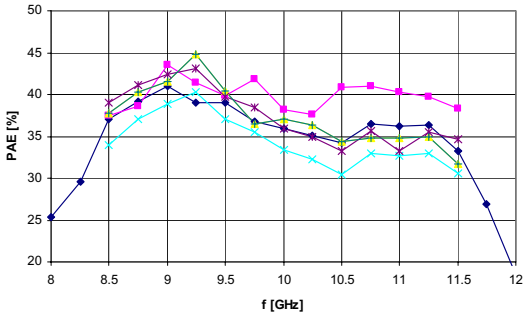

Fig. 14. Power added efficiency of the Driver Amplifier measured at V_{DS}=8 V and P_S=17 dBm.

VII. Conclusion

The design and measurement results of two high power amplifiers and one driver amplifier have been discussed. An excellent average output power of 10 Watt combined with a gain of 21dB and a PAE of 30% has been obtained for the three-stage amplifier. For the two-stage high-power amplifier an average output power of 8 Watt, a PAE of 27% and a gain of 16 dB have been obtained.

The driver amplifier shows an output power of more than 1 Watt, a PAE of more than 30% and gain of more than 15 dB over the 8.5-11.5 GHz frequency band.

In summary, it can be stated that a high performance power amplifier chip set has been realized in a high volume low cost process.

References

[1] F.E. van Vliet and A. de Boer, “Fully-Integrated Core chip for X-band Phased-Array T/R modules “, IEEE MTT-S Symposium Digest, pp. 1753-1765, 2004.

[2] Thermal Analysis System, HTTAS:09, January 2003.

[3] A.P. de Hek, Workshop on High-Power Amplifier fundamentals, GAAS 2004.

[4] A.P. de Hek, “Design, Realisation and Test of Gaas-based Monolithic Integrated X-band High-Power Amplifiers”, ISBN 90-386-1920-0, July 2002.

[5] www.mimixbroadband.com, data sheet XP1006.