Dispersion Free Doped and Undoped AlGaN/GaN HEMTs on Sapphire and SiC Substrates

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***Abstract* — We present dispersion free pulsed current voltage (I-V) and radio frequency (RF) power results of undoped and doped AlGaN/GaN HEMTs on sapphire and SiC substrates. The most significant processing step leading to these results is the application of a reactive ion etching (RIE) argon (Ar) plasma (10sccm, 40mTorr, 20W, t=30s, DC bias = -167V, 20°C) to the AlGaN surface before annealing of the ohmic contacts and surface passivation with plasma enhanced chemical vapor deposition (PECVD) silicon nitride (SiN_x). In addition, this process strongly improves the uniformity of RF device performance and is independent of the material source.**

I. Introduction

Over the past few years radio frequency (RF) power results for AlGaN/GaN HEMTs on both sapphire and SiC substrates improved significantly. State of the art RF power densities for conventional gate devices on these substrates are 6-7W/mm [1] and 10-12W/mm [2], respectively. Devices with gate extensions or field plates have shown a tremendous increase in power densities up to 12W/mm on sapphire substrates [3] and 30W/mm on SiC substrates [4].

In practice, the maximum RF output power of AlGaN/GaN HEMTs can be significantly less than what may be expected from the static current voltage (I-V) curves and the chosen operating point. This discrepancy, generally indicated as DC-to-RF dispersion or gate lag, is due to drain current collapse during RF power operation which itself is caused by trapping of two-dimensional electron gas (2DEG) electrons in the gate drain access region at the AlGaN surface [5]. The most commonly used method to eliminate gate lag is passivation of the AlGaN surface using silicon nitride (SiN_x) [6].

We have observed that passivation with only SiN_x indeed leads to increased current recovery and good uniformity of the DC characteristics. However, the uniformity of RF device performance, even on samples as small as $10\times10mm^2$, can be very poor and hence severely limit process yield. Although GaN is well known to withstand harsh environmental conditions we have found that gate lag is very sensitive to surface treatments and its reduction is strongly related to proper device processing.

Dispersion free pulsed I-V and RF power results of undoped and doped AlGaN/GaN HEMTs on sapphire and SiC substrates will be presented. In addition, the uniformity of RF device performance has strongly been improved and the results are independent of the material source. We will show that the key processing step has been the application of a reactive ion etching (RIE) argon (Ar) plasma (10sccm, 40mTorr, 20W, t=30s, DC bias = -167V, 20°C) to the AlGaN surface before rapid thermal annealing (RTA) of the ohmic contacts and SiN_x surface passivation.

II. Material and Device Layout

For this work we used comparable undoped AlGaN/GaN heterostructures on sapphire substrates from RF Nitro and QinetiQ. The doped HEMT structures on semi-insulating SiC substrates have been grown by the Fraunhofer Institute for Applied Solid-State Physics (IAF). All epitaxial material was grown by metal organic chemical vapor deposition (MOCVD). We have investigated devices with a total gate periphery (W_g) of $2\times40\mu m$ using either optically defined gates with a gate length (L_g) of $2\mu m$ or electron beam written gates with L_g = 400nm. The former are referred to as "fat" gate devices, the latter are referred to as "submicron" gate devices. Fat gate devices have a drain-source spacing (L_{ds}) of $10\mu m$ and the gate is placed in the middle of this region. The gate-source (L_{gs}) and gate-drain (L_{gd}) spacings in the submicron devices are $1\mu m$ and $2\mu m$, respectively. All gates are arranged in a U-shape configuration. Fig. 1 shows the layout of a fat gate device.

III. Process Technology

The application of surface treatments to the AlGaN barrier layer prior to SiN_x passivation is based on the hypothesis that contaminants, processing remnants or crystal irregularities residing at the AlGaN-SiN_x interface prevent effective and reproducible gate lag reduction, which leads to poor uniformity of RF device performance even on samples as small as $10\times10mm^2$. We assumed that cleaning and reorganization of the AlGaN surface

prior to SiN_x passivation would strongly improve reproducible gate lag minimization. We have investigated the influence

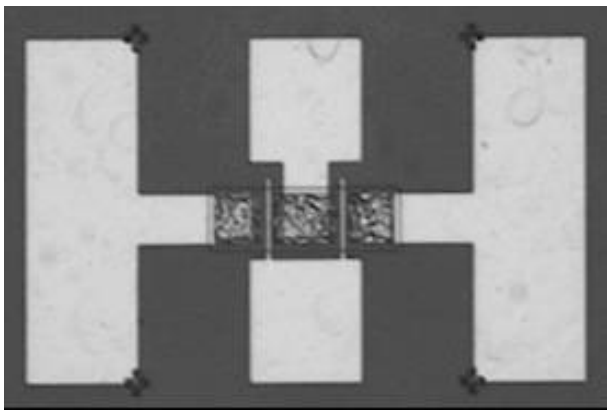


Fig. 1. Layout of a fat gate device. Total gate width (W_g) is 2×40µm, gate length (L_g) is 2µm and source-drain spacing (L_{ds}) is 10µm.

of buffered hydrofluoric acid (BHF) and RIE Ar plasma (10sccm, 40mTorr, 20W, t=30s, DC bias = -167V, 20°C) in combination with SiN_x passivation on the amount of gate lag and the uniformity of RF device performance. The BHF dip (t=60s) was performed at the start of the HEMT processing whereas the Ar plasma was applied just before the RTA step (800°C, 2 minutes) of our optimized Ti/Al/Ni/Au ohmic contacts [7]. The RTA step is carried out at 800°C to avoid degradation of the crystallinity of the AlGaN material [8]. Annealing for 2 minutes still yields good ohmic contacts (R_c = 0.3Ωmm) and enables reorganization of the AlGaN surface.

To make a good comparison between the four possible surface treatments and to exclude sample to sample spread we have combined them on the same sample with a typical size of 10×10mm^2. On all processed samples, we have fabricated four identical transistor modules consisting of 91 HEMTs each. Module 1 did not get any surface treatment prior to passivation with 100nm PECVD SiN_x (250°C, refractive index at 632nm of 1.994) and served as a reference. Module 2 was only dipped in BHF. Module 3 was only exposed to the Ar plasma and module 4 got both these treatments before SiN_x passivation.

IV. RESULTS

To examine the amount of gate lag in our devices, we have built a measurement setup to perform on-wafer pulsed I-V measurements. This setup consists of a HP214B voltage pulse generator, DC bias sources and a HP54120A digitizing oscilloscope. The starting point for the pulsed I-V measurement was to bias the device in the saturation region and just below pinch-off. The values used for the drain-source (V_{ds}) and gate-source (V_{gs}) voltages were 10V and -6V, respectively. Voltage pulses of 100ns in width (9ns rise time, 0.2% duty cycle) were used to drive V_{gs} from -6V (just below pinch-off) to 0V (open channel). The value of the drain current in response to the applied pulses to the gate ($I_{ds,p}$) was determined 15ns from the leading edge. Fig. 2 shows the pulse shape of the drain current in response to a gate pulse for passivated undoped fat gate devices on sapphire substrates that severely suffer from gate lag. Fig. 3 shows the drain current pulse response for a similar dispersion free device.

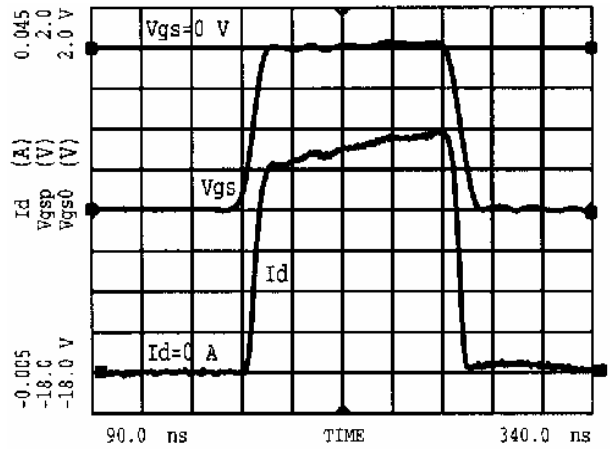


Fig. 2. Pulse shape of drain current in response to a gate pulse for passivated undoped fat gate devices on sapphire substrates showing strong gate lag.

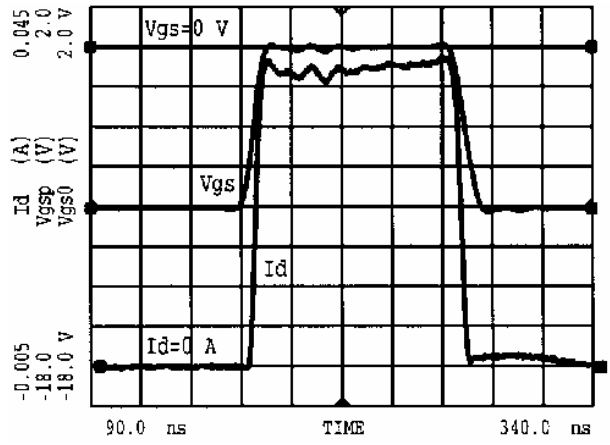
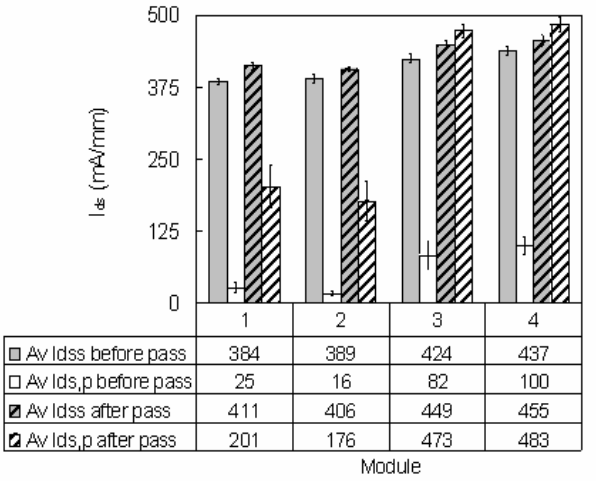


Fig. 3. Drain current pulse response for dispersion free passivated undoped fat gate devices on sapphire substrates.

We have defined the amount of gate lag as the ratio between $I_{ds,p}$ and the DC drain current at V_{gs} = 0V (I_{dss}). Fig. 4 shows typical gate lag behavior of the fat gate devices on RF Nitro and QinetiQ material from the four differently treated modules before and after passivation with 100nm SiN_x. The clear bars represent average values for I_{dss} (gray) and $I_{ds,p}$ (white) before SiN_x passivation. The corresponding dashed bars represent average values of these quantities after passivation. The error bars indicate the standard deviation of the measured values. In each module 15 transistors have been

measured. The relatively moderate values for I_{dss} are mainly caused by the dimensions of the fat gate devices, which give rise to considerable parasitic source and drain resistances.



	1	2	3	4
Av Idss before pass	384	389	424	437
Av Ids,p before pass	25	16	82	100
Av Idss after pass	411	406	449	455
Av Ids,p after pass	201	176	473	483

Fig. 4. Pulsed I-V results of undoped fat gate HEMTs on sapphire substrates fabricated using different surface treatments (module 1: reference; module 2: BHF; module 3: Ar; module 4: BHF & Ar). The clear bars represent average values for I_{dss} (gray) and $I_{ds,p}$ (white) before SiN_x passivation. The corresponding dashed bars represent average values of these quantities after passivation. The error bars indicate the standard deviation of the measured values.

Fig. 4 clearly indicates that the devices from all modules show a very large amount of gate lag before passivation. This is especially true for the modules that have not been treated with the Ar plasma (modules 1 and 2, respectively). After SiN_x passivation, the amount of gate lag in devices from modules 1 and 2 has been decreased significantly but it still is unacceptably large. This is in sharp contrast with devices from the modules that have been treated with the Ar plasma (modules 3 and 4, respectively) because in that case gate lag has completely vanished. It should be noted that the strong reduction of self-heating under pulsed measurement conditions causes $I_{ds,p}$ to be higher than the corresponding I_{dss}. When looking at the error bars it should also be noted that the Ar plasma has significantly improved the uniformity of the pulsed I-V results after passivation. The observed increase in the values for I_{dss} and $I_{ds,p}$ after passivation is in accordance with literature [6]. Although the combination of the BHF dip and the Ar plasma treatment (module 4) in combination with the SiN_x passivation gave the best result it has to be concluded that the Ar plasma is the key processing step leading to the strongly minimized gat lag and the significantly improved uniformity of the results.

Fig. 5 shows the static I-V curves of passivated undoped submicron gate devices on sapphire substrates that have been processed using the BHF and Ar plasma treatments. Based on these curves the expected maximum output power density in class A operation would be:

$$P_{out} = 1/4 \times (V_{ds} - V_k) \times I_{dss} = 1/4 \times (26-7) \times 0.7 = 3.3 W/mm \quad (1)$$

where V_k is the knee-voltage.

Fig. 6 shows active load-pull measurement results at 4GHz of these passivated submicron gate devices using V_{ds} = 26V and V_{gs} = -6V as bias conditions. These RF power results confirm the absence of gate lag as had been indicated by the pulsed I-V results because the maximum output power density of 3.3W/mm is in excellent agreement with the value based on the static I-V curves. It has to be noted that this value for the output power density is thermally limited. The maximum power dissipation for these devices was 350mW.

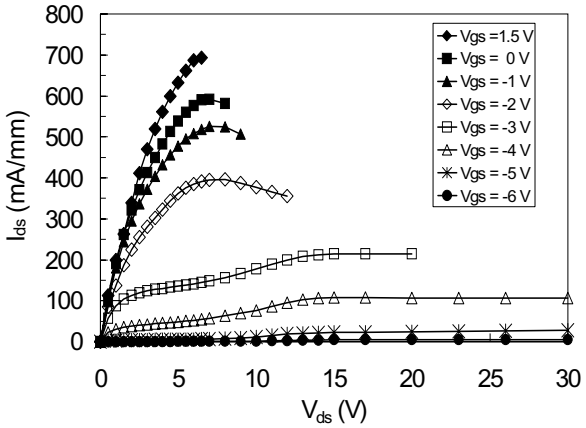


Fig. 5. Static I-V curves of passivated undoped AlGaN/GaN submicron gate devices on sapphire substrates that have been processed using the BHF and Ar plasma treatments.

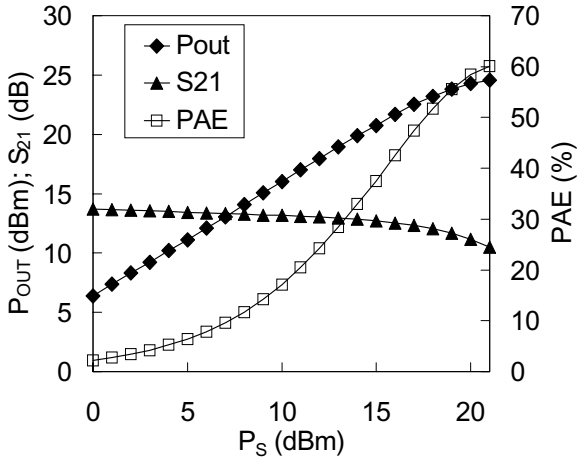
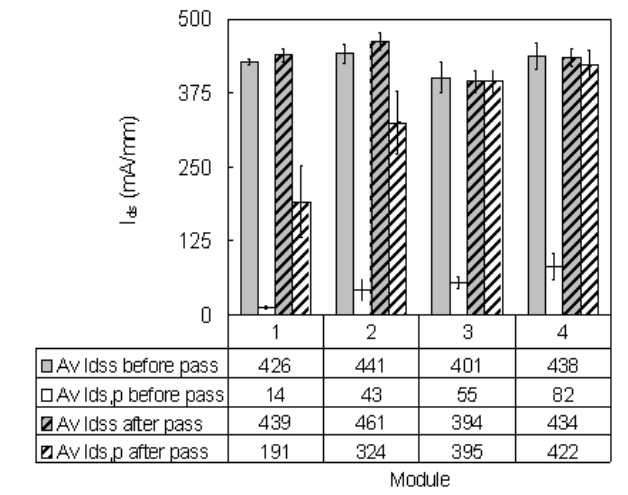


Fig. 6. Active load-pull data at f=4GHz of passivated undoped AlGaN/GaN submicron gate devices on sapphire substrates that have been processed using the BHF and Ar plasma treatments. Bias conditions: V_{ds} = 26V, V_{gs} = -6V. The maximum output power density corresponds to 3.3W/mm.

As a next step, we have directly transferred the transistor process, which has been developed on the undoped HEMT structures on sapphire, to doped AlGaN/GaN structures on SiC substrates from IAF. The previously described fat gate HEMT layout and processing approach have been used. Fig. 7 shows the pulsed I-V results for these doped structures before and after SiN_x passivation. Again, the clear bars represent

average values for I_{dss} (gray) and $I_{ds,p}$ (white) before SiN_x passivation. The corresponding dashed bars represent average values of these quantities after passivation and the error bars indicate the standard deviation of the measured values.



	1	2	3	4
Av Idss before pass	426	441	401	438
Av Ids,p before pass	14	43	55	82
Av Idss after pass	439	461	394	434
Av Ids,p after pass	191	324	395	422

Fig. 7. Pulsed I-V results of doped fat gate devices on SiC substrates fabricated using different surface treatments (module 1: reference; module 2: BHF; module 3: Ar; module 4: BHF & Ar). The clear bars represent average values for I_{dss} (gray) and $I_{ds,p}$ (white) before SiN_x passivation. The corresponding dashed bars represent average values of these quantities after passivation. The error bars indicate the standard deviation of the measured values.

Figure 7 clearly shows that the general dispersion behavior of the doped structures on SiC substrates is similar to that of the undoped structures on sapphire substrates. Although the process needs some fine-tuning to achieve the full potential of these structures, the modules that have been exposed to the Ar plasma (modules 3 and 4) again show excellent gate lag minimization.

VI. Conclusions

The presented pulsed I-V and RF power results of undoped and doped AlGaN/GaN HEMTs on sapphire and SiC substrates have shown strongly minimized gate lag and significantly improved uniformity of RF device performance. These results are of significant importance to the enhancement of process yield especially in the case of large periphery RF power devices. We have shown that the key processing step was the application of the RIE Ar plasma to the AlGaN surface before annealing of the ohmic contacts and SiN_x surface passivation. In addition, this process is independent of the material source.

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