50 Watt S-band Power Amplifier in 0.25 μm GaN Technology

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***Abstract*—A 50 W S-band High Power Amplifier in the UMS GH25-10 technology is presented. In order to increase the output power per area the size of the transistors is increased beyond the maximum size modelled by the foundry. For this reason the design procedure included the measurements of a transistor and the creation of a scalable Angelov-GaN model with the use of EM simulations. An output matching design approach is adopted which intrinsically optimizes the transistor harmonic load impedance. The results show that the amplifier delivers an output power of over 50 W within the frequency range from 3.05 to 3.5 GHz at a PAE of more than 62 %. The maximum measured output power is 63 W with a PAE of 65 %.**

I. Introduction

Modern radar systems are often implemented as Active Electronically Scanned Arrays (AESA) in which the viewing direction and beam shape are adjusted electronically. Beam steering is obtained by amplitude and phase control for a large number of small antennas, usually aligned in a flat plane. The main advantages are their greater flexibility (for example multiple viewing directions simultaneously and variable beam shapes) and higher reliability (no moving parts). The scope and the chance of detection of a radar system is to a significant extent determined by the total transmitted power. In a phased array radar system the total power is generated by a large number of "small" power amplifiers. The RF power per amplifier is limited by the used semiconductor technology and the total available supply power. The power density is a limiting factor because only a portion of the power is actually transmitted (amplifier efficiency). The remaining power is converted into heat, which makes a proper cooling system essential. An increase of the output power at a lower power dissipation gives immediate relief from the requirements at system level and will lead to higher performance, smaller, lighter and cheaper systems. Reduction of the cost of the power amplifier remains relevant because of the large number of amplifiers required by AESA systems.

Gallium nitride power amplifiers offer several advantages over other III-V type semiconductor amplifiers. The high breakdown voltage of GaN transistors offers the possibility to use higher drain supply voltages. This eases the DC power distribution on a system level by causing lower supply currents. Besides the higher impedance levels eases the power matching problems resulting in lower loss or higher bandwidth. Furthermore GaN devices or more robust to load mismatch which makes them more reliable. As the thermal conduction of GaN is superior the removal of generated heat is less problematic. Considerations for the use of GaN MMIC HPA at S-band frequencies relate to the dimensions and robustness, especially when the HPA is directly connected to an antenna [1].

II. Technology

The UMS GH25-10 technology, a 0.25 μm GaN HEMT MMIC technology [2] is used for this HPA. This technology is developed to address applications and market needs up to Ka band. The breakdown voltage of the transistors is in excess of 100 V. The process will be qualified on a 4 inch substrate diameter and contains MIM capacitors, Thin Film Resistors and through wafer vias. Integrated power amplifiers in this technology have been published at other frequency bands, an example is given in [3].

One of the key figures of power amplifiers is the RF output power per chip area. Trade-offs between output power, efficiency, reliability and chip dimensions are investigated for several amplifier topologies. It was concluded that in order to achieve a competitive output power density, the transistors in the output stage needed to be larger than maximum available size utilized by the foundry. This implies that the creation of custom transistor model was required.

III. Transistor modelling

The HPA contains contains two amplifying stages with four 10x360 μm transistors in the output stage and a single 10x250 μm transistor in the input stage. As these dimensions are outside the range covered by the foundry model library, a custom model was developed. During the time of modelling the largest available sample was an 8x100 μm transistor. This means that a model was required that is scalable to higher values of gate width and larger number of fingers.

The DC part of the non-linear model consists of the drain-source current source, the gate-source diode current source and the drain-gate breakdown current source. The drain-source current and the gate-source diode current are described with the Angelov-GaN equations [4]. The drain-gate breakdown current is based on DC off-state breakdown measurements. The DC IV curves are measured from a quiescent bias point of V_{dg}=30 V and V_{gg}=-2.5 V. as this gives the best representation of the operation of the FET in the HPA.

The samples available for measurements all have eight gate fingers and the unit gate width is in the range from 75 μm to 250 μm. This means that scaling of the (extrinsic) model

parameters over number of gate fingers and for large unit gate widths cannot be determined from measurements. For this reason an estimation of the scaling is based on EM simulations. These simulations are performed on extrinsic transistor parts with different values for gate width and number of fingers. Based on the obtained scaling rules the extrinsic component values for a measured device are determined.

The intrinsic small signal Y-parameters are derived based on the extrinsic model parameters obtained from the previously described scaling. After deembedding of the extrinsic transistor model components, the intrinsic transistor small signal parameter values are extracted according to the well known method described by Dambrine et.al. [5]. The bias dependency of the capacitance values are described with the Angelov-GaN equations. The output impedance of the transistor is further optimized with the help of the available dispersion model.

IV. Design

A schematic view of the entire HPA is shown in figure 1. The stability of the individual transistors is improved by placing parallel RC networks in series with the gates. The transistors of the output stage are not made unconditionally stable as this would result in a very low power gain and would have a big impact on the overall amplifier PAE. The gate bias voltage for each stage is generated by an active gate bias circuits that compensates for variations in threshold voltage [6]. This bias circuit contains a logic enable-input to be able to switch off the HPA with a LVCMOS signal [3]. The drain supply voltages are supplied from a single side. The shunt capacitors in the output matching network are implemented as a stacks of three capacitors to support the large voltage swing.

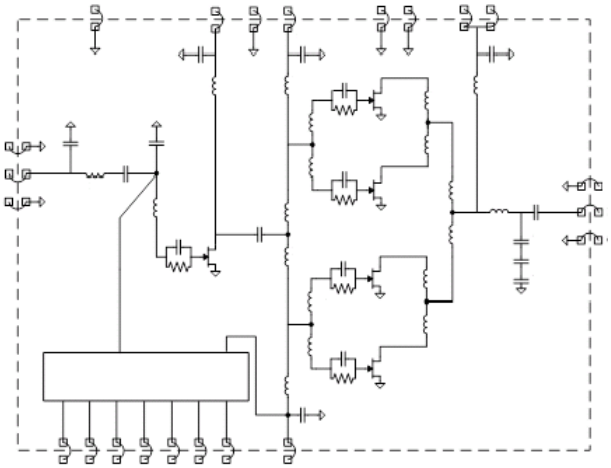

Fig. 1: Power amplifier schematic.

The optimum load impedance of the transistors is determined from load pull measurements on an 8x250 μm transistor at a single frequency of 2.5 GHz. The output power and PAE contours from a fundamental load pull are shown in figure 2. The measurement was performed at a source power that yields the highest PAE and with a second harmonic load of 50 Ω.

The output power and PAE contours for a variation of second harmonic load are given in figure 3. It is seen that both the output power and PAE are improved if a termination

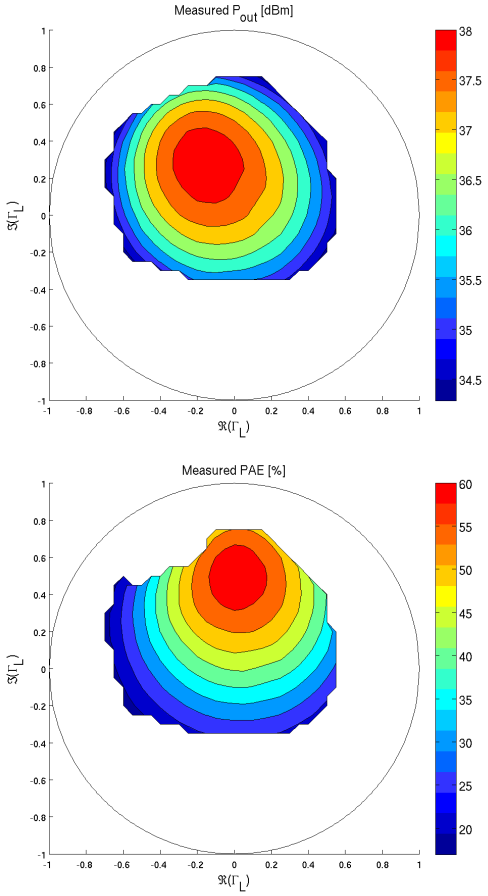

Fig. 2: Fundamental loadpull, Vd=30 V, Vgs=-2.5 V, f=2.5 GHz.

near an open circuit is applied. The output power and PAE improvement with respect to a 50 Ω termination are 0.3 dB and 5 % respectively.

For the HPA design a compromise load is selected between the maximum output power and maximum PAE load. This selected load is modelled with a parallel RC network of 92 Ω and -850 fF. For the design of the output matching networks this load model of the 8x250 μm transistor is scaled to the required dimensions. The obtained model is then translated to a series LR network, representing the same impedance at the mid-band frequency. This load model intrinsically contains the high impedance values at the harmonic frequencies as found optimal from the load pull measurements. Figure 4 represents this approach. Based on this LR load model an ideal matching network is synthesized and the in-band matching to the RC network is enhanced during the conversion step to microstrip components while the phase at the second and third harmonics frequency ranges are kept close to zero. The wideband loads that are presented to the output stage transistors are given in figure 5 together with the reference loads of the RC and RL network. The reference loads in fundamental frequency range and the transistor loads in the first, second and third harmonic frequency range are highlighted in the plot. It is seen that in-band the loads are close to required loads, while at the harmonic frequencies the loads are close to an open circuit.

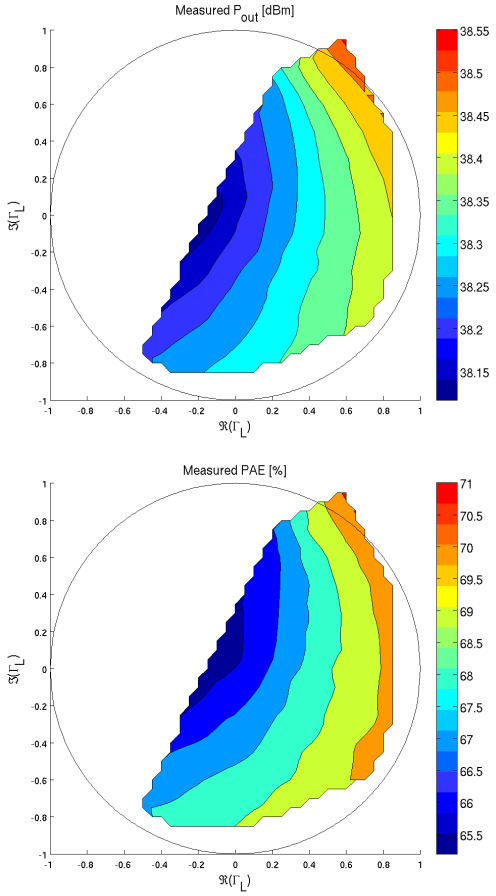

Fig. 3: Second harmonic loadpull, Vd=30 V, Vgs=-2.5 V, f=2.5 GHz, $\Gamma_{f0} = -0.1 + j0.46$.

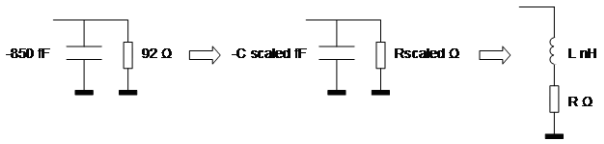

Fig. 4: Transformation of in band optimum loads to broadband model for matching network design.

V. Results

The layout of the HPA is shown in figure 6. The chip area is 12.6 mm^2.

Figure 7 shows the output power of the HPA measured on wafer, together with the initially simulated results. It is seen that the output power level is according to the simulated value with a peak level above 60 W but a frequency shift of approximately 150 MHz is present.

The PAE of the HPA is given in figure 8 together with the simulated values. Besides the frequency shift, also an increase of approximately 10 % is observed. This deviation is due to the transistor model accuracy as the PAE deviation is also observed in measurements on a single FET.

The input matching of the HPA is shown in figure 9. The level of matching better is better than -10 dB over the entire frequency range. Also here the frequency shift with respect to simulations is observed.

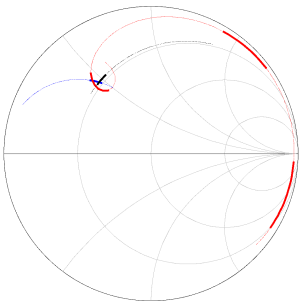

Fig. 5: Broadband loading of output stage transistors (red), reference RC (blue) and RL (black) model loads, f=2.5 to 11 GHz.

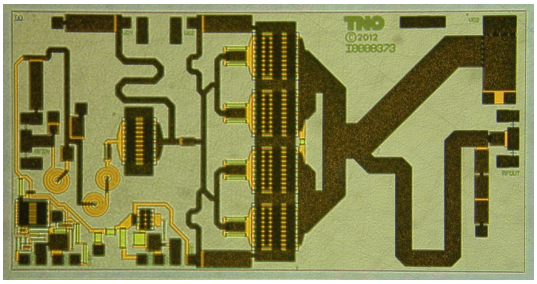

Fig. 6: Layout of S-band HPA, chip dimensions are 4.5x2.8 mm^2.

TABLE I: Overview HPA results.

Parameter		Simulation	Measurement
Operating frequency	(GHz)	2.9 to 3.4	3.05 to 3.5
Output power	(dBm)	$>$ 46	$>$ 46
PAE	(%)	$>$ 50	$>$ 60
Input matching	(dB)	$<$-12	$<$ -10

TABLE II: Comparison the previous work.

Reference	Frequency	P_{out}	PAE	A	$\frac{P_{out} \cdot PAE}{A}$
	(GHz)	(W)	(%)	(mm^2)	(W/mm^2)
[7]	2.9 - 3.5	85	59	5x4.4	2.28
[8]	3.3 - 3.9	18.2	55	-	-
[9]	2.8 - 3.4	32	47	4.3 x 5.6	0.62
[10]	3.2 - 4.3	50	43	4.1x3.1	1.69
[1]	2.7 - 3.3	30	30	5x3.3	0.55
This work	3.05 - 3.5	50	62	4.5 x2.8	2.46

A summary of the obtained results is given in table I.

In table II a compassion against other recently published S-band GaN HPAs is given. It is seen that the device delivers competitive performance. If a figure of merit is defined equal to the product of output power and PAE divided by the chip area, the current HPA delivers the best performance.

VI. Conclusion

A GaN S-band HPA is designed, manufactured and measured. The two stage amplifier delivers and output power of

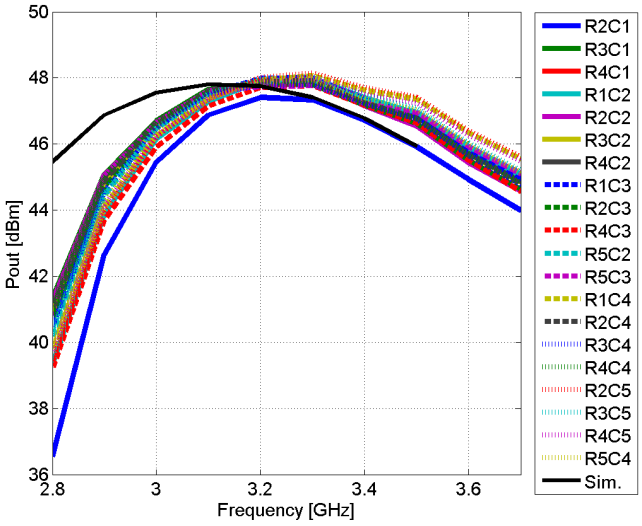

Fig. 7: Output power of all HPAs, measured from wafer at Vd=30 V, Vss=-8 V, T=25 °C, PW=10 μs, PRF=1 kHz.

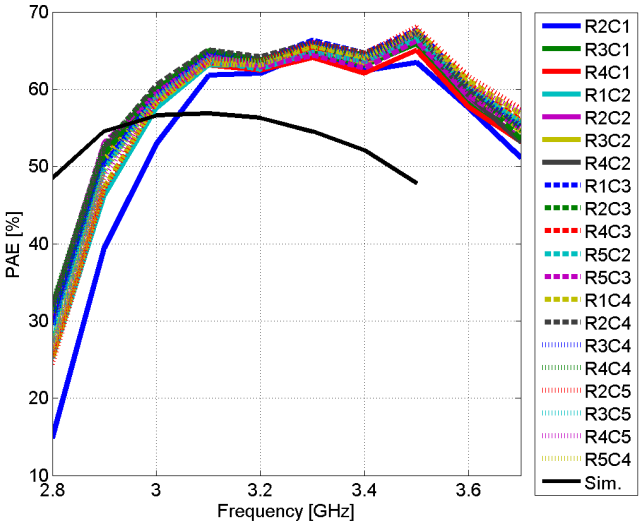

Fig. 8: Power added efficiency of all HPAs, measured from wafer at Pavs=28 dBm (measured) or 26 dBm (sim.), Vd=30 V, Vss=-8 V, T=25 °C, PW=10 μs, PRF=1 kHz.

in excess of 50 Watt over a frequency range from 3.05 to 3.5 GHz with a peak power of more than 60 W. The PAE of the amplifier is higher than 62 %. With a chip dimension of 12.6 mm^2 the output power normalized to chip dimension is 4 W/mm^2.

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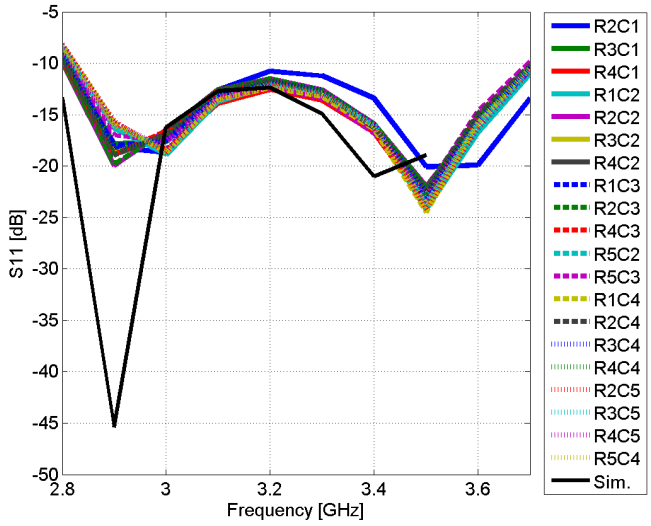

Fig. 9: Γ_{in} of all HPAs, measured from wafer at Pavs=28 dBm (measured) or 26 dBm (sim.), Vd=30 V, Vss=-8 V, T=25 °C, PW=10 μs, PRF=1 kHz.

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