Generic robust LVCMOS-compatible control logic for GaAs HEMT switches

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***Abstract* — Robust digital control logic for a X-band five-bit digital attenuator and six-bit phase shifter has been developed and tested. The circuit uses an innovative combination of feedback and feed forward. The devices have been developed in the 6-inch 0.5 µm power pHEMT process (PP50-10) of WIN Semiconductors. The use of this process results in cost effective devices with a high power capability.**

***Index Terms* — FET digital integrated circuits, FET switches, MMIC phase shifters, Attenuators.**

I. Introduction

Digitally controlled binary attenuators and phase shifters are widely used components [1, 2] in Transmit Receive modules for phased array antennas applications. In this paper digital control logic is presented that is used to control an attenuator and phase shifter. The circuits are designed in a low-cost GaAs power process. Both devices are suitable for X-band applications and show competitive performance. It will be shown that the digital interface electronics included on the devices has a stable performance over both temperature- and process variations.

II. PP50-10 power HEMT technology

The designs have been realized in the PP50-10 power pHEMT process of WIN Semiconductors. The transistors in this process have a gate length of 0.5 µm and the substrates thickness is 100 µm. The use of this process is attractive because of the 6" wafer size and good reproducibility resulting in a high-yield and a relatively low price per device. The (depletion mode) FETs are used as switches.

III. Digital control logic

Since the phase shifter and attenuator should be controlled with single ended voltages coming from LVCMOS digital circuits on-chip level shifters and inverters are required. This section describes the design of these level shifters and inverters. The goal of this design is to comply with the LVCMOS specifications, listed in table I. The specifications indicate that a voltage under 0.8 V should be accepted as a logic zero and that a voltage above 2 V should be accepted as a logic one. The maximum current drawn should stay below 24 mA, but this is only specified for voltages between the supply voltages of the digital circuit. It is known that drawing large currents from a low output can cause latch up. No latch up current limit is given. Since the level shifter draws only 0.5 mA per input no problems are expected as long as not too many inputs are connected to a single LVCMOS output.

TABLE I. SPECIFICATIONS OF LVCMOS.

Parameter	Value	Description
V_{OL}	0.4 V	Maximum low output voltage
V_{IL}	0.8 V	Maximum low input voltage
V_{OH}	2.4 V	Minimum high output voltage
V_{IH}	2.0 V	Minimum high input voltage
Imax	24 mA	Maximum current

Fig. 1 shows the simulation result of a simple level shifter inverter without any compensation for process variations. The performance of this circuit for a nominal process is good, but the variation renders the circuit unusable.

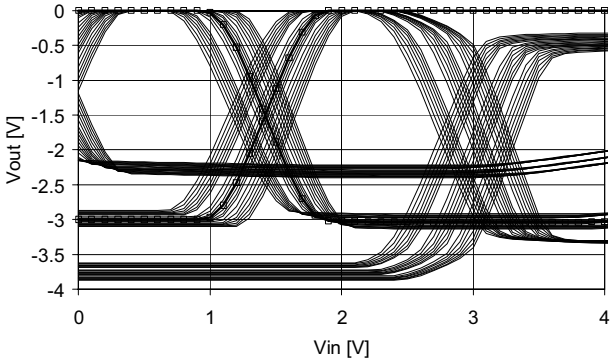

Fig. 1. DC simulation results of a simple level shifter inverter versus input voltage with variation of the resistors (±15%), threshold voltage (±0.3V) and temperature (-40°C to 80°C).

The digital control logic described compensates for process variations. Fig. 2 depicts a block schematic of the digital control logic. It shows a bias generator that generates bias voltages that compensate the process dependency of the level shifters and inverters. The level shifter shifts the LVCMOS signal down to a level that can be accepted by the inverter. The inverter has

complementary output signals with the correct levels for the switch FETs used in the attenuators and phase shifters.

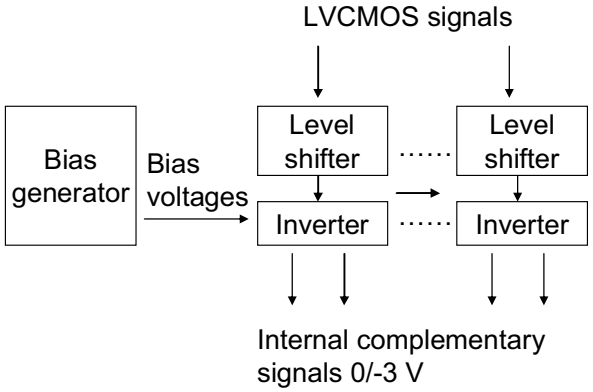

Fig. 2. Block schematic of the digital control logic.

The design is based on 3 assumptions:

1. Resistance variation does not affect the voltage divide ratio of a voltage divider.
2. The square resistance is the same within the whole level shifter inverter.
3. The threshold voltage variation is the same within the whole level shifter inverter.

Fig. 3 depicts a detailed schematic of the digital control logic. The bias generator makes the voltages v_1 and v_2 over the resistors in the current sources equal to the voltage supplied by the resistor divider on the left. In this way effects of temperature and threshold variation are eliminated. The current delivered by the current source is inversely proportional to the resistance. This eliminates the effect of the resistance variation on the output voltage.

Since the gain provided by the differential pair is not infinite some effects of the variation are still present. A thing that requires special care is the temperature behaviour of the diodes. The forward voltage varies with -2 mV/°C. In the bias generator 6 diodes are present giving 1.5 V difference in voltage drop over the temperature range of -40°C to 80°C. This has a large impact on the level shifter. To be able to meet the LVCMOS specifications 2 diodes have been connected in series with the resistor in the level shifter. They give 0.5 V voltage drop variation over the temperature range compensating the effect of the diodes in the bias generator.

The stability of the feedback circuit is checked using the loop gain and the output impedance of the current source. Fig. 4 shows that the low frequency gain is 5.7 and a phase margin of 85°. This check is also done with some extra parasitic capacitances at some places to check the sensitivity for parasitics on the stability.

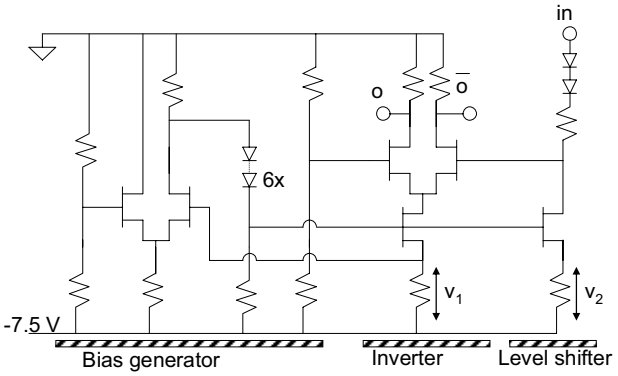

Fig. 3. Detailed schematic of the bias generator and the inverter level shifter.

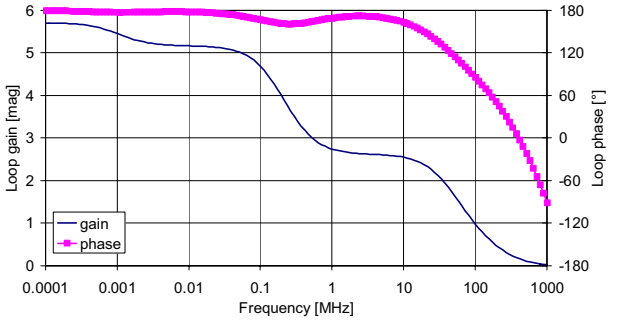

Fig. 4. Loop gain and phase of the feedback circuit in the bias generator.

IV. Scaling and Variation

Fig. 5 shows the simulation result of the digital control circuit with process variation. It can be seen that for all cases a voltage below 0.8 V is accepted as a logic 0 and that a voltage of more than 2 V is accepted as a logic 1. The simulation is performed for temperatures from -40 °C to 80 °C, a resistor variation of ±15 % and a threshold variation of ±0.3 V.

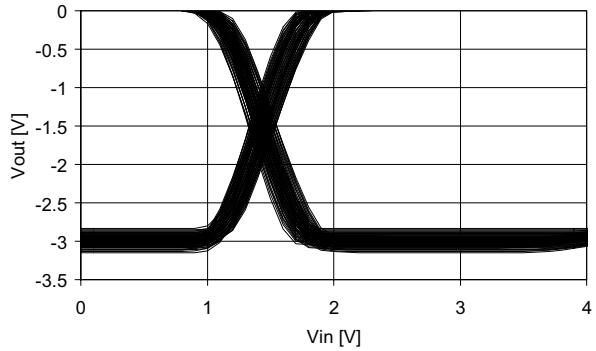

Fig. 5. DC simulation results of level shifter inverter versus input voltage with variation of the resistors (±15%), threshold voltage (±0.3V) and temperature (-40°C to 80°C).

Fig. 6 shows the simulation result of the digital control circuit with supply voltage variation from 6 to 9 V (±20%). Since the supply voltage is used as a reference the performance changes a lot. The output level changes is linear with the supply voltage. The switch point changes with 10%.

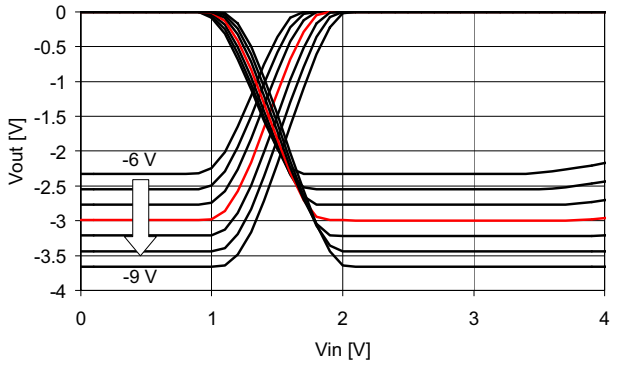

Fig. 6. DC simulation results of level shifter inverter versus supply voltage from -6 to -9 V.

Fig. 7 shows the measurement result of the digital control logic versus temperature. The measurement results come from a wafer which has the lowest threshold voltage within the PCM window. The threshold voltage shifted from -1.4 to -1.7 V. It can be seen that the digital control logic is still working correctly.

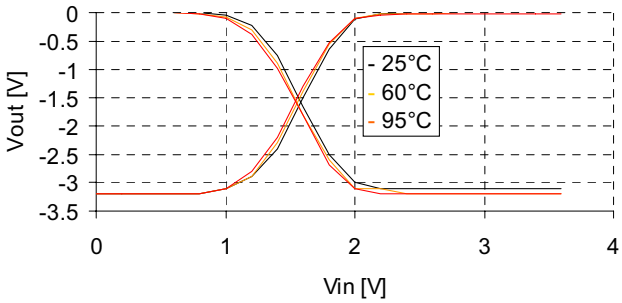

Fig. 7. DC measurement results of level shifter and inverter versus input voltage and temperature (25°C to 95°C).

The number of bits used is scalable by repeating the inverter and level shifter cells. The maximum number of bits is limited by the available perimeter of the chip. The size of the bias generator is 340x210 μm^2. The combined size of the inverter and level shifter is 200x210 μm^2. When the bond pads are included the height increases to 370 µm. The size of the inverter level shifter is thus slightly above the size of the bond pads and the area the circuit occupies is compensated by the reduction in bond-pads needed. Reducing the number of bond pads also reduces the cost by reducing the number of bond wires and leads needed.

Fig. 8 shows a photograph of the digital control logic with 5-bits as used in the attenuator.

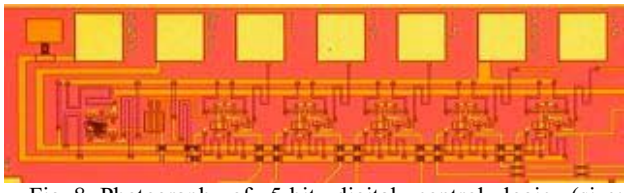

Fig. 8. Photograph of 5-bit digital control logic (size: 1.5 x 0.4 mm^2, including bond pads).

V. Application Example

An attenuator and phase shifter have been designed with the digital control logic. The attenuator and phase shifter use switch FETs with two or four gate-fingers operating at a gate to source voltage of 0 V ('on-state') and -3 V ('off-state'). Before the actual design the first step was the modelling of these switch FETs. A scalable model has been created based on the measurement results of switch FETs with seven different dimensions.

Both devices consist of separate sections (henceforth called bits) with binary weighted attenuation- or differential phase values. If possible the parasitic capacitances of the switch FETs are embedded in the filter- or attenuator sections of the individual bits. For both designs each individual bit is matched to 50 and the following order of the bits is optimized for large signal performance. The isolation between the different bits is enhanced by adding extra ground strips at tactical positions. The bond-pads are embedded in 50 π-networks to improve the overall matching of the devices.

The switch FETs are driven by differential signals from the on-chip digital electronics. Each bit is controlled by a single ended LVCMOS signal with a '0' for the reference state and a '1' for the enabled state. Since each bit is controlled via a separate control signal, the binary scale of the bit values is transparent to the control of the devices.

The layout of the attenuator is shown in Fig. 9.

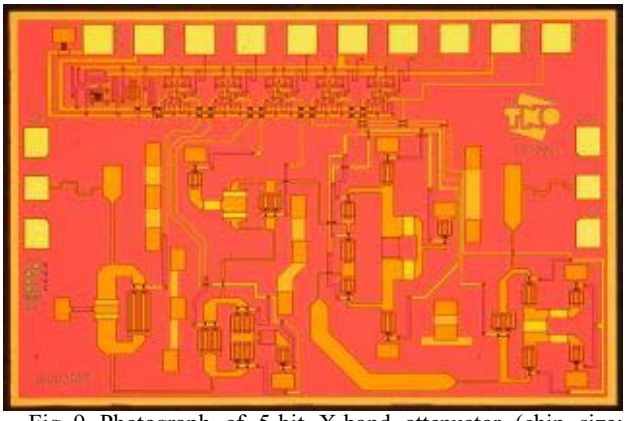

Fig. 9. Photograph of 5-bit X-band attenuator (chip size: 2.4 x 1.6 mm^2).

Fig. 10 shows the attenuation of a typical attenuator for all states. It can be seen that all states are addressed. The nominal step size is 0.9 dB. The total attenuation range is 28 dB.

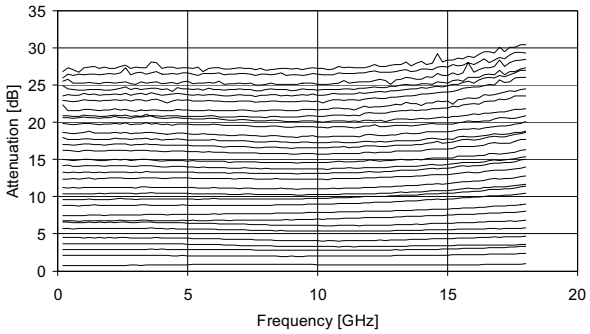

Fig. 10. Attenuation of a typical attenuator. Measured from 0.2 to 18 GHz.

In Fig. 11 the measured RMS attenuation error over all states is shown. It is seen that for frequencies up to 15 GHz, the error is smaller than 0.6 dB.

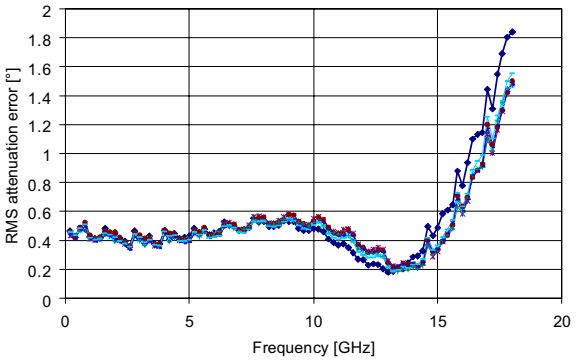

Fig. 11. RMS attenuation error of attenuator. Measured on eight samples.

The input- and output matching of the attenuator are at X-band frequencies better than -16 dB for all states. The reference loss is smaller than 6 dB for frequencies up to 14 GHz. The transfer remains linear until a source power of 23 dBm is reached.

The layout of the 6-bit phase shifter is shown in Fig. 12.

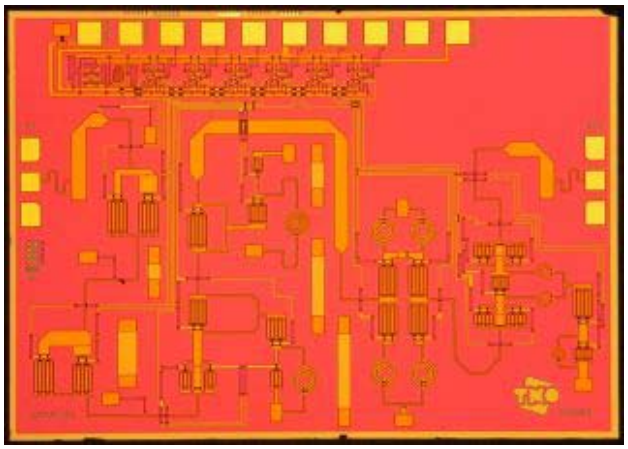

Fig. 12. Photograph of 6-bit X-band phase shifter (chip size: 3 x 2.1 mm^2).

Fig. 13 shows the phase shift of a typical phase shifter versus frequency. The phase-frequency plane is well covered.

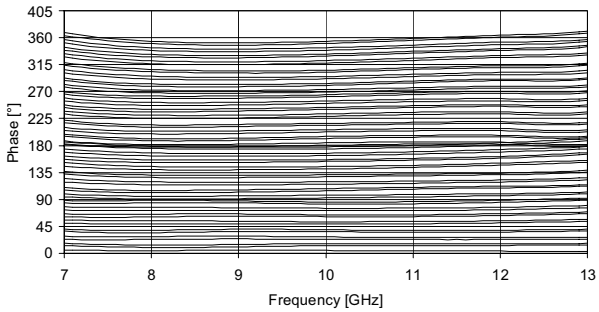

Fig. 13. RMS phase error of phase shifter. Measured on five samples.

Measurement results of five different samples of the phase shifter from a single wafer are given in fig. 14. The measured RMS phase error over all states is given.

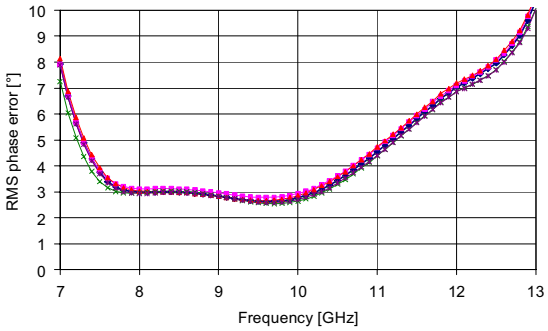

Fig. 14. RMS phase error of phase shifter. Measured on five samples.

The reference loss is smaller than 7 dB for frequencies between 7 GHz and 12.6 GHz. The matching at X-band frequencies is better than -10 dB for all states. The transfer remains near linear until a source power of 20 dBm is reached. The worst case 1dB compression power is larger than 22 dBm.

VI. Conclusion

Robust LVCMOS compatible control logic that is insensitive to process variations has been designed and measured. By employing a feedback circuit the effect of process variation is greatly reduced. The digital control logic is scalable and reusable. A first pass success attenuator and phase shifter have been designed using this digital control logic.

References

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[2] A. de Boer, J.A. Hoogland, E.M. Suijker, M. van Wanum, F.E. van Vliet, "Highly-Integrated X-band Multi-function MMIC with Integrated LNA and Driver Amplifier," GaAs 2002 Symposium Digest.