Design and Analysis of a 34 dBm Ka-Band GaN High Power Amplifier MMIC

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Abstract — **This paper presents the design and analysis issues related to the use of recent GaN technologies for realizing high power millimeter wave MMICs. Two GaN Ka-band amplifier MMICs have been designed, fabricated and characterized. The small-signal and power measurement results are presented for both amplifiers, with an excellent output power of 34.1 dBm at 27 GHz for the 2-stage power amplifier MMIC. Both MMICs have a very good yield and performance, even more so in regard of the current state-of-the-art. The observed deviations between the original simulation and measurements have been explained by extensive use of 3D EM simulations of the coplanar passive structures.**

Index Terms — **GaN, MMIC power amplifiers.**

I. INTRODUCTION

Millimeter-wave GaN amplifiers are technologically highly challenging. The combination of millimeter-wave frequencies, implying submicron gate lengths, with high power, implying high breakdown voltages, with a challenging thermal problem, even at good efficiencies, is not trivial at all. It is this problem that is the subject of this paper.

AlGaN/GaN HEMTs are genuine high-speed and high power devices, which combine to date the capabilities of wide bandgap semiconductors. They have demonstrated extremely promising performance at X-band with power densities exceeding GaAs PHEMT by nearly a factor of 10 [1]. They combine wide band gap semiconductor properties, i.e. high breakdown fields relative to other common III-V semiconductors, with transport properties similar to those of Si. This so far has made them extremely promising for the lower frequency range up to 20 GHz. Recent reports from NEC in Japan show an extremely promising performance of 250 nm and 150 nm gate length AlGaN/GaN devices on SiC for 30 GHz [2] and even 40 GHz power operation [3][4].

GaN is generally grown on a different substrate material, such as sapphire, silicon or silicon carbide. The substrate material then determines the thermal behavior, and in particular silicon carbide is a very good heat conductor. Further, the use of GaN pHEMT transistors allows the use of high bias voltages (breakdown voltages over 100 Volt are encountered). This reduces the requirements for DC-DC converters, and is hence good for the system efficiency and cost reduction. Also, the high bias voltage is of great help in the matching of the power amplifiers, that now inherently present a higher output impedance. Finally, the increased power density of GaN as compared to GaAs will lead to small MMICs, which is a good way to reduce the cost price, and allows for compatibility with millimeter-wave phased-array stacking requirements.

II. GaN TECHNOLOGY EMPLOYED

The power amplifier results presented in the next section are based on the FhG-IAF AlGaN/GaN HEMT technology. This technology is based on multiwafer MOCVD growth on 2 inch semi insulating (s.i.) SiC substrates based on an Aixtron 2000 multiwafer reactor. Next to epitaxy, a full 2 inch AlGaN/GaN technology on s.i. SiC and sapphire is available with gate length range currently down to 500 nm (optical stepper lithography) and down to 150 nm (e-beam). The T-gate technology is e-beam defined with a gate length of l_G= 150 nm. Device isolation is achieved with mesa isolation. Devices with a gate-width of W_g= 0.48 mm yield a maximum drain current of > 1.1 A/mm and a transconductance of > 275 mS/mm at V_{DS}= 7 V. The current gain cut-off frequency f_T of the 0.48 mm device is well beyond 50 GHz at V_{DS}= 7 V. The maximum frequency of oscillation at V_{DS}= 7 V amounts to f_{max}> 80 GHz. Currently the maximum operational voltage is V_{DS}= 35 V with a corresponding on-state breakdown voltage of BV_{DS}> 65 V. Loadpull measurements for a 0.4 mm device used for the modeling yield a saturated output power of > 3.5 W/mm at 30 GHz, a linear gain of > 5 dB at V_{DS}= 30 V tuned for maximum output power in CW operation at room temperature. A large number of GaN MMICs have been realized in this technology [5][6] and the passive components are specially optimized to suit the harsh power requirements of GaN MMICs.

III. GaN MODELLING AND MMIC DESIGN

Specific GaN large-signal modeling has recently received much attention, such as in [7]. The high power densities and the dispersive effects of the GaN transistors require the full use of the modeling capabilities developed for GaAs PHEMT including self-heating and low frequency dispersion and further development of the extraction and verification procedures. Pulsed DC and time domain RF measurements are used for model verification at various frequencies, as a simple small-signal based approach can be fundamentally misleading.

For the design of the passive structures, a full coplanar ADS design-kit is available on SiC substrate containing

NiCr resistors, lines, junctions, and high-voltage MIM capacitances, all suitable for Ka-band operation. Because of the high voltage and current requirements for the passives, thick metal plating is used.

From a design point of view, GaN MMIC design is not so different from GaAs based design. The increased output impedance level is repeatedly stated as advantageous in the literature. We have found, however, that at 30 GHz the transformation of the intrinsic impedance through the millimeter-wave layout with its parasitics is dominating, and largely removes this feature. Further, interstage matching of the very different input and output impedance levels requires similar attention as for GaAs PHEMT amplifiers, as the ratio is still large. Because of the limited range of available CPW line impedances that can be used, the design of the matching networks is more difficult than when using microstrip lines. This results in relatively large losses of the matching networks (e.g. 1.5 dB for the HPA output matching and 3.0 dB for the HPA interstage matching), which is considerably higher than for standard GaAs microstrip MMIC designs.

Due to the innovative nature of the design, considerable margins were taken for the design. The selected topology for the driver is a 3-stage design with 1x4x60 – 1x4x60 – 1x8x60 FETs and an estimated gain of 18 dB and output power of 31 dBm. The topology of the power amplifier is a 2-stage design with 2x8x60 – 4x8x60 FETs with an estimated gain of 10 dB and output power of 37 dBm. The selected operating point is V_{DS}= 30 V and V_{GS}= -3.0 V, which corresponds with a class-AB setting. The optimum load for the 8x60 µm output FET has been based on loadpull simulations and is around 6.65 + j 20.3 Ω at the drain reference plane at 30 GHz. This might seem a rather low impedance for a GaN device, but as stated earlier this is caused by impedance transformation of the extrinsic drain parasitics. The internal output resistance corresponding with this load is around 110 Ω.
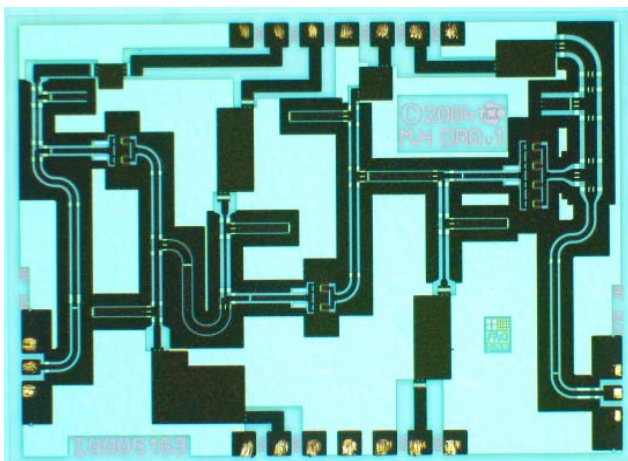

Fig. 1. Photograph of the 3-stage driver amplifier MMIC with a size of 2.75 x 2.00 mm².

Each active device has been made unconditionally stable by adding a parallel RC network in series with the gate. This is a conservative design approach that causes extra interstage matching loss, but aids in obtaining a stable amplifier and a first iteration design success. The resulting first iteration MMIC designs are shown in Fig. 1 and Fig. 2.
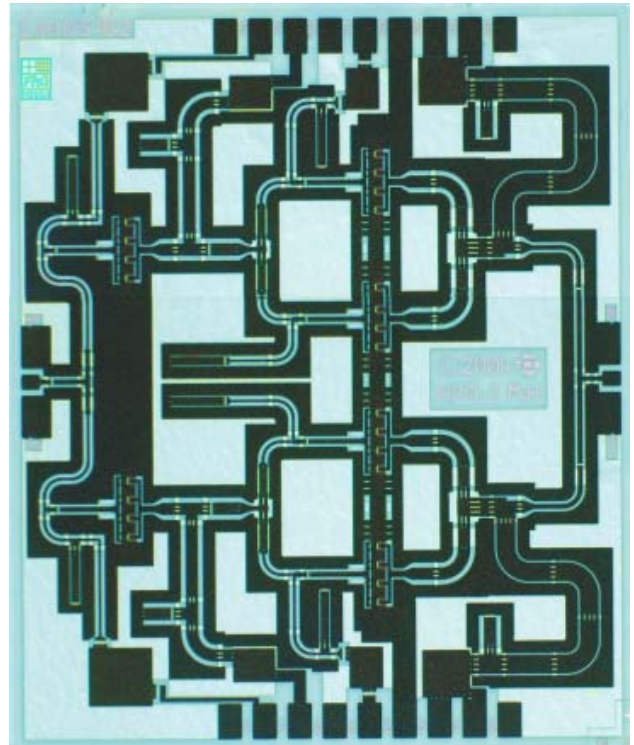

Fig. 2. Photograph of the power amplifier MMIC with a size of 2.75 x 3.25 mm².

IV. MEASUREMENT RESULTS

The initial measurements on these two MMICs have already been shown in [8]. By now a much better understanding of the observed behavior has been obtained by the extensive use of 3D EM simulations of the passive structures and re-simulating the design using measured S-parameter FET data.

These measurements have shown a reduction in output power (-3 dB) and gain (-3 dB to -5 dB) and a downward shift (3 GHz) in frequency. Part of this deviation can be explained by the technology performance. For this purpose a test structure has been used of the 8x60 µm FET including RC stability network, as it is being used in the power amplifier. The comparison between the simulated and measured maximum gain was determined from S-parameter measurements of this test structure. Although the measured gain was lower than expected, more than 6 dB per transistor was available. The measured output power density of the 8x60 µm FET was around 3 W/mm at 27 GHz, while the design has been based on an output power density of 4 W/mm.

To check the accuracy of the original passives library, measurements on test structures have been performed and compared with the original models and new 3D EM (HFSS) simulations. One such test structure is a series capacitor connected to a short, in a T-structure. The HFSS model of this structure is shown in Fig. 3. In the design this element is used to provide a short circuit in the bias lines around the operating frequency of 30 GHz.
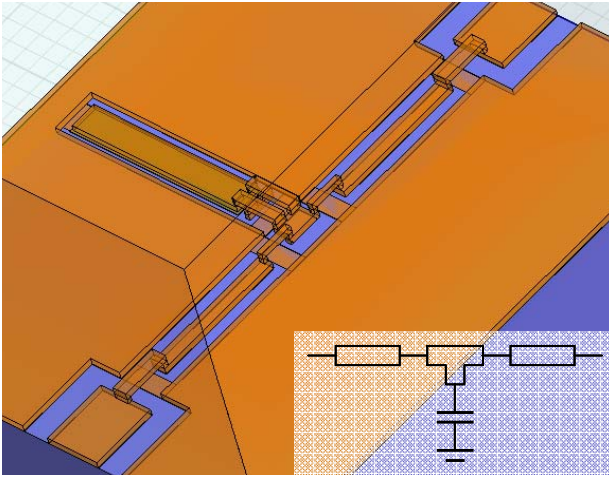
Fig. 3.   3D HFSS model of the decoupling test structure.

The advantage of this test structure is that the resonance frequency is not influenced by the accuracy of the calibration. The simulated and measured results, for 17 measured test structures, are shown in Fig. 4. As can be seen there is a downward frequency shift between the original simulation and the measurements. The HFSS simulation result of this structure compares very well with the measurements. The major cause of the frequency shift is the fact that the capacitor model is not accurate for large aspect ratios, as used in this structure.
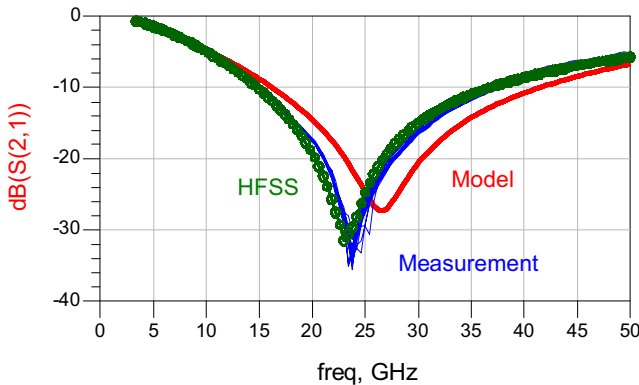

Fig. 4.   Measured (thin blue lines) and simulated gain of the decoupling structure using the original model (thick red line) and the HFSS model (green circles).

Also EM simulations with a 2.5D EM simulator, Momentum, have been tested, but these have found to be less accurate because of the very thick CPW lines and narrow gaps. From this test structure analysis it has been concluded that all passive networks in the MMIC design needed to be simulated with HFSS to check their performance and the effect on the overall MMIC performance.

The slightly reduced performance of the active devices and de-tuning of the matching networks has had its effect on the power and gain performance of the driver amplifier and power amplifier MMIC. To verify the measured performance, the designs have been re-simulated using measured small signal S-parameter data for the active devices and using the results from the HFSS simulations of the matching networks. The result

of this analysis for the small signal gain of the driver is shown in Fig. 5 and for the power amplifier in Fig. 6.
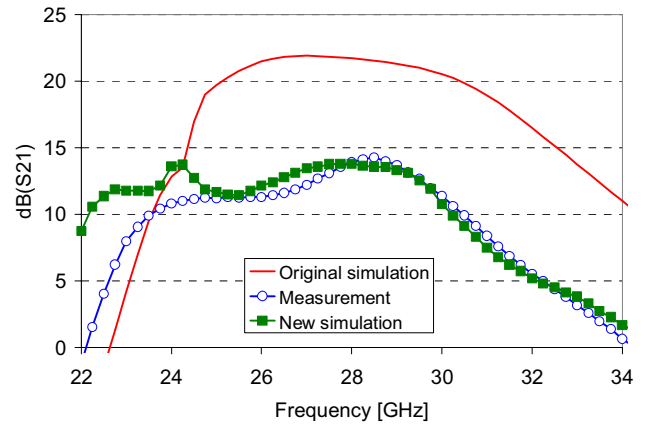

Fig. 5.   Measurement (blue circles), original simulation (red line) and new simulation (green squares) of the small signal gain of the driver amplifier MMIC biased at V_{DS}= 30 V and V_{GS}= -5.25 V.
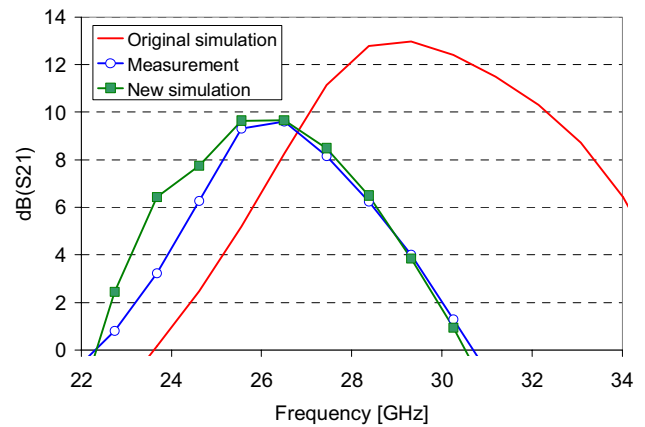

Fig. 6.   Measurement (blue circles), original simulation (red line) and new simulation (green squares) of the small signal gain of the power amplifier MMIC biased at V_{DS}= 30 V and V_{GS}= -5 V.

For both designs the new simulations correspond very well with the measurements, and can explain the reduction in gain and shift in frequency. This analysis will enable the successful redesign of these two MMICs to operate at the correct frequency. Finally the measured large signal performance has been verified with new simulations. The measured output power, gain and efficiency of the power amplifier MMIC, together with the new simulation, are plotted in Fig. 7.

The maximum measured output power at 27 GHz is 34.1 dBm with a power gain of 5.5 dB, which is a very good result for a 2-stage MMIC at this frequency. Using the HFSS models for the passives and newly extracted large signal FET models, the observed large signal behavior is correctly predicted by the new simulations.
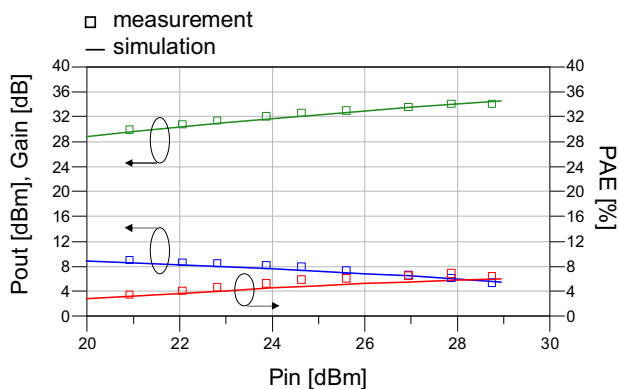
Fig. 7. Measured (squares) and simulated (solid line) CW output power, gain and efficiency at 50 Ω load versus input power at V_{DS}= 30 V, V_{GS}=-5 V and 27 GHz.

Furthermore, initial linearity measurements have been performed on the power amplifier at V_{DS}= 20 V, giving a third order output intercept point of 38.7 dBm. However, the requirements on the measurement setup for driving the power amplifier are very high and additional experiments are still needed to finalize the linearity characterization at high linear input power levels.

V. CONCLUSIONS AND OUTLOOK

Using the FhG-IAF AlGaN/GaN on SiC technology, two coplanar Ka-band amplifier MMICs have been designed, fabricated and analyzed. The results show very promising performance. The 2-stage power amplifier MMIC shows an output power of 34.1 dBm at 27 GHz. The measured small signal and large signal performance have been verified by re-simulating the designs using HFSS results for the passives and measured FET data. This successful analysis enables to redesign these MMICs to operate at the correct frequency.

With increasing design experience in such processes, improved modeling accuracy and process reproducibility even higher performance figures are near. The introduction of microstrip technology for GaN designs will further increase the power amplifier MMIC performance, by providing decreased matching losses and increased design freedom. In conclusion, it has been shown that GaN technology, especially for power amplifier designs, can offer lower cost and higher performance systems for applications over a wide frequency range.

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