S-BAND SIGE PHASE AND AMPLITUDE CONTROL MMIC

F.E. van Vliet, A. de Boer and G.C. Visser

TNO Defence, Security and Safety, P.O. Box 96864, 2509 JG, The Hague, The Netherlands
Phone: 31.70.374.07.40, Fax: 31.70.374.06.54, Email: frank.vanvliet@tno.nl

Abstract – **This paper presents very recent achievements in the Silicon implementation of phase and amplitude control for active electronically steered arrays. The IC combines 6-bit amplitude control with more than 20 dB amplitude range, including control logic and series-to-parallel converters. The IC is a step forward in lowering active array cost and presents a small IC area with a high phase accuracy and dynamic range.**

I. INTRODUCTION

Active electronically steered arrays (AESA's) have strong requirements on their front-end electronics, both in the radar and in the telecommunication domain. Due to the nature of AESA's, beam steering is generally accomplished by changing phase and amplitude of individual transceive modules. At microwave frequencies this is traditionally implemented by III-V electronics, generally GaAs.
There is an ever increasing demand for a reduction in cost, power consumption and size. For a considerable time, the reduction in size has mainly been achieved by integrating as much as possible the required functionality in one or two monolithic microwave integrated circuits (MMIC's). For the current state-of-art at microwave frequencies, the full transmit/receive (T/R) module is implemented by a single MMIC for power levels up to approximately 23 dBm, and by two MMIC's for higher power levels.
In the world of consumer electronics, the majority of the functionalities is currently implemented in Silicon RF CMOS or BiCMOS technologies. The main driver for this is the very attractive cost of these technologies, especially when produced in large quantities. Current phased-arrays generally do not use silicon for the microwave electronics.
The results presented in this article clearly show that in the near future this is likely to change for frequencies in S-Band and above.
Obviously, the functionality of the front-end will change dramatically, once silicon finds its way into the front-end. Although a strong increase in functionality may be expected from this migration, we will concentrate in this paper on the actual demonstration of silicon promises to AESA front-ends.

II. DEFINITION

Based on existing solutions for phase- and amplitude control for AESA's operating in S- and C-Band, a set of specifications has been derived. The specifications are summarised in Table 1.

Table 1: Target specifications for an S-band phase and amplitude control MMIC.

Parameter	**Target**
Frequency of operation [GHz]	2.6 – 3.8
Phase range [°]	360
Phase resolution	6 bits
Phase error [°]	< 3.6 r.m.s.
Amplitude error [dB]	< 0.4 r.m.s.
Amplitude range [dB]	> 15
Insertion Gain [dB]	> 0
S11 [dB]	< -10
Pout [dBm]	> 10
Chip size [mm^2]	< 9
Supply voltage [V]	3.3
Control	Serial, LVCMOS

III. TECHNOLOGY

Several constraints had to be taken into account for the technology. On the one hand, a modern technology is preferred, as this is likely to offer the best high-frequency capabilities, and the best perspective for the years to come. On the other hand, modern technologies tend to be the more expensive ones, and require very large volumes for a justication of mask and other costs.
Trade-offs had to be made between RF CMOS and BiCMOS technologies. As the majority of the functionality is analogue, no real argument can be made for the necessary digital integration. The increased dynamic range from the BiCMOS processes turned out to be necessary.

We have chosen to use a Silicon Germanium (SiGe) BiCMOS process from Austriamicrosystems. In particular, the 0.35µm SiGe-BiCMOS based on the proven 0.35µ m mixed-signal CMOS process licensed from TSMC has been used.
This advanced RF process offers high-speed HBT transistors with excellent analog performance, high fmax and low noise as well as complementary MOS transistors with 3.3V and 5V gate voltages. The AMS design kit has been used for the development of the MMIC.

IV. DESIGN

A block diagram of the design realized is shown in figure 1. As can be seen, a phase shifter based on a vector modulator with digital control was chosen. As opposed to conventional III-V vector modulators, the control circuitry could be implemented on the same die.
The vector modulator consists of an IQ generator and differential amplifiers and mixers. An output amplifier is added to allow for output levels as high as 10dBm. The IQ generator and differential amplifiers have been tested individually before, and showed adequate performance.

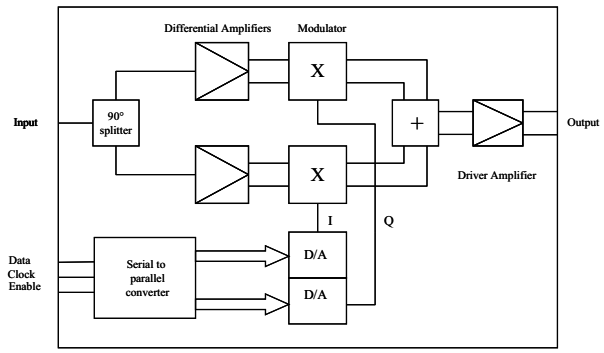

Figure 1: Block diagram of the SiGe amplitude and phase control MMIC.

The RF path is divided into two equal outputs with 90 degrees phase difference. The In-phase channel is designated as the I channel. The Quadrature-phase channel is designated as the Q channel. Each signal passes through a mixer which sets the attenuation level of both the I and Q path and 0 or 180 degree state. The output of the I and Q path are combined into the required vector.
The mixer employed is of the Gilbert type. This type of mixer requires that the input signal of the mixer is differential. As a result, the buffer amplifiers needed to be implemented differentially.

Gilbert mixers also have a balanced output, which put demands on the output buffer. As there is no on-chip balun, this needs to be implemented off-chip when single-ended signals are required.

The control inputs of the Gilbert cell are connected to the DAC via a pre distortion circuit. For layout reasons the serial to parallel circuits is split up in two segments, bit 0 to 7 and bit 8 to 15.

The resulting layout is shown in figure 2. From left to right, the quadrature splitter, differential amplifiers, Gilbert cell mixer and the two stage driver amplifier can easily be identified. At the upper and lower edge of the chips, the pad ring , serial to parallel converter, D/A converters, reference voltage circuits and control amplifiers are placed.
The size of the MMIC is 2.75x2.5 mm2, which is found much smaller than other approaches to the problem.

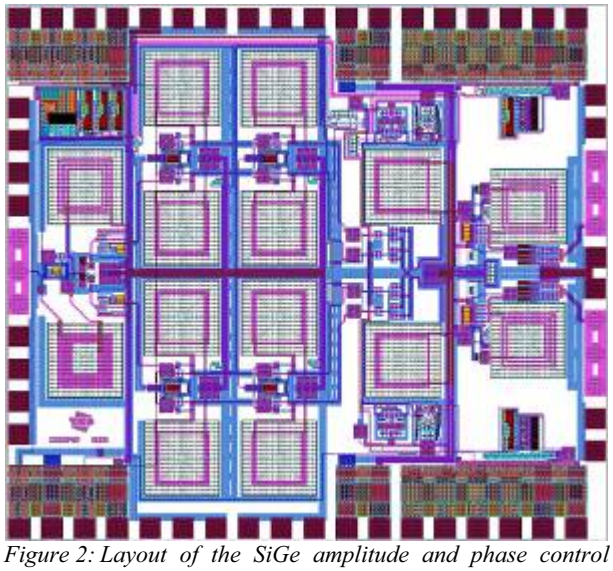

Figure 2: Layout of the SiGe amplitude and phase control MMIC.

IV. SIMULATION RESULTS

The simulated uncorrected RMS phase error (for 6 bit resolution) and RMS amplitude error over gain range for three frequencies are summarised in Table 1 to 3. The absolute amplitude variation over phase states at 3.2 GHz at 0 dB gain setting is shown in Figure 4. The absolute phase error over phase states at 3.2 GHz at 0 dB gain setting is shown in Figure 5. The simulated gain is more than 20 dB and the output power is around 10 dBm.

Table 2 RMS Phase and amplitude error at 3.2 GHz

Gain setting	Phase RMS error	Amplitude RMS error
0	0.702	0.14
-10	1.26	0.154
-15	1.771	0.153
-20	2.725	0.153

Table 3 RMS Phase and amplitude error at 2.6 GHz

Gain setting	Phase RMS error	Amplitude RMS error
0	4.648	0.512
-10	4.782	0.537
-15	5.391	0.53
-20	7.078	0.542

Table 4 RMS phase and amplitude error at 3.8 GHz

Gain setting	Phase RMS error	Amplitude RMS error
0	3.672	0.374
-10	3.591	0.381
-15	3.812	0.382
-20	4.362	0.389

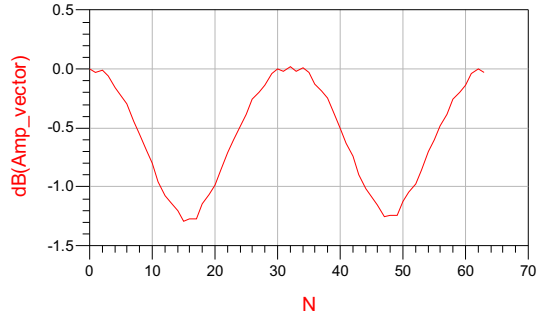

Figure 3: Simulated amplitude variation over phase states at 3.2 GHz and 0 dB gain setting

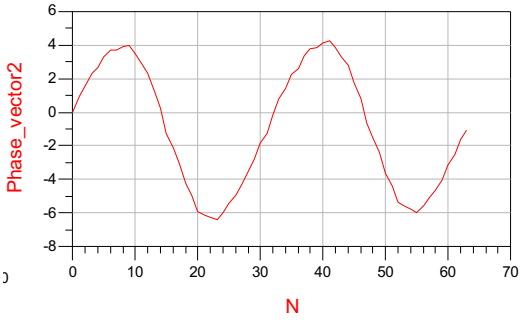

Figure 4: Simulated phase error over phase states at 3.2 GHz and 0 dB gain setting

V. CONCLUSIONS

This paper has presented very recent achievements in the Silicon implementation of phase and amplitude control for AESA's. The performance combines 6-bit amplitude control with more than 20 dB amplitude range. The IC is a step forward in lowering active array cost and presents a small IC area with a high phase accuracy and dynamic range. The functionality is realised in combination with a serial-to-parallel converter. Further work on the addition of calibration and control is expected and adds greatly to the low-cost nature of the solution described.

VI. ACKNOWLEDGEMENT

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