Multi Function and High Power Amplifier Chipset for X-Band Phased Array Frontends

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***Abstract* — This paper presents the design and measurement results of two MMICs for X-band phased array applications: a Multi Function Chip (MFC) and High Power Amplifier (HPA). The fully integrated MFC combines the phase and attenuation setting, Transmit/Receive (T/R) switching, Low Noise Amplifier and Driver Amplifier. Furthermore active biasing and a Low-Voltage CMOS compatible digital interface are included. The HPA design is matched to the MFC to create a two-chip T/R module solution and shows an excellent performance of 39.7 dBm output power with 46 % PAE at 9.0 GHz.**

***Index Terms* — MMIC, Phased array, radar, transmit/receive module, high power amplifier.**

I. Introduction

Modern phased array radar systems use up to thousands of antenna elements, often with one T/R module per element [1]. The cost of these T/R modules are for a large part determined by the cost of the Microwave Monolithic Integrated Circuits (MMICs) that are being used in the module and also by the total number of MMICs in one module [2][3]. The number of MMICs needed for one T/R module can be drastically reduced by combining as many functions as possible on a single MMIC, the so called Multi Function Chip. A possible integration of functions is shown in Fig. 1.

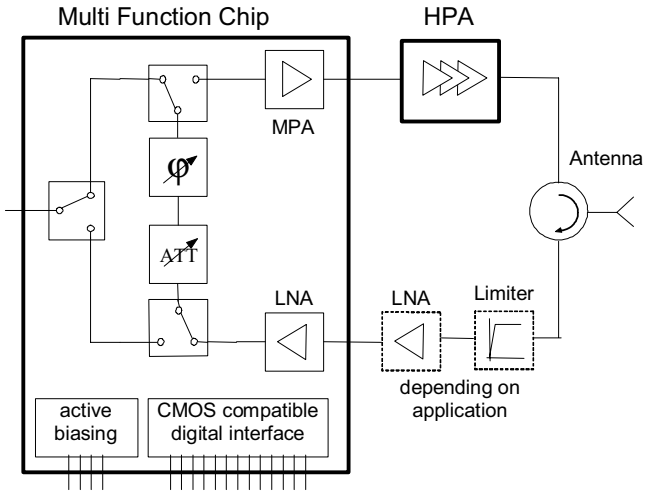

Fig. 1. Block diagram of a phased array T/R module frontend.

In this paper a Multi Function Chip and HPA MMIC are presented that together form a two-chip T/R module frontend. Depending on the specific application, only an external limiter and LNA might be necessary. The MFC is designed in the 0.25 μm PHEMT (PH25) process of UMS and integrates as much functions as possible into a single MMIC. The HPA is a 3-stage design in the 0.25 μm power-PHEMT (PPH25X) process of UMS. First the design and measurement results of the MFC are presented, followed by the HPA design and results.

II. Multi Function Chip

The topology of the MFC is based on a partial common leg architecture, as shown in Fig. 1. This design consists of the following functionalities and features:

- three T/R switches,
- a 2-stage LNA at the receive input,
- a 6-bit phase shifter in the common leg,
- a 5-bit attenuator in the common leg,
- several interstage amplifiers,
- a 2-stage driver amplifier at the transmit output,
- a combined level shifter/inverter for 0 V – 3.3 V LVCMOS compatible digital control,
- two gate bias circuits and
- simple biasing using +4 V and -4 V connections.

The design of this MMIC is based on previous versions of the MFC [4][5]. A detailed description and schematics of the building blocks can be found in these references. The major improvements with respect to the previous version are the reduction of the total MMIC size from 24.8 mm^2 to 20.0 mm^2, the use of a 0 V – 3.3 V LVCMOS compatible digital interface (instead of a -5 V – 0 V interface), improved active biasing to compensate for temperature variations, improved Tx-Rx isolation and performance improvements by using measurement data from the previous iteration. Experience from the previous version has shown that it is very important to reduce the MMIC size to obtain an acceptable yield. This has resulted in an excellent functional yield of this new design, measured on one wafer, of better than 80 %. The drawback of reducing the MMIC size is the risk of increased coupling between the folded branches of the common leg, especially for branches with large amplitude differences that occur in the attenuator. Much attention has been paid to reduce the coupling as much as possible by placing multiple grounded shield lines between the branches. The effectiveness of these shield lines has also been verified by EM simulations. The chip photograph of the MFC is shown in Fig. 2, clearly showing the shield lines between the different branches

of the common leg and the switches. In the layout the switches are placed on the left side, the LNA on the bottom-right and the driver amplifier on the top-right. The digital interface circuitry is concentrated on the right side, between the Tx and Rx port.

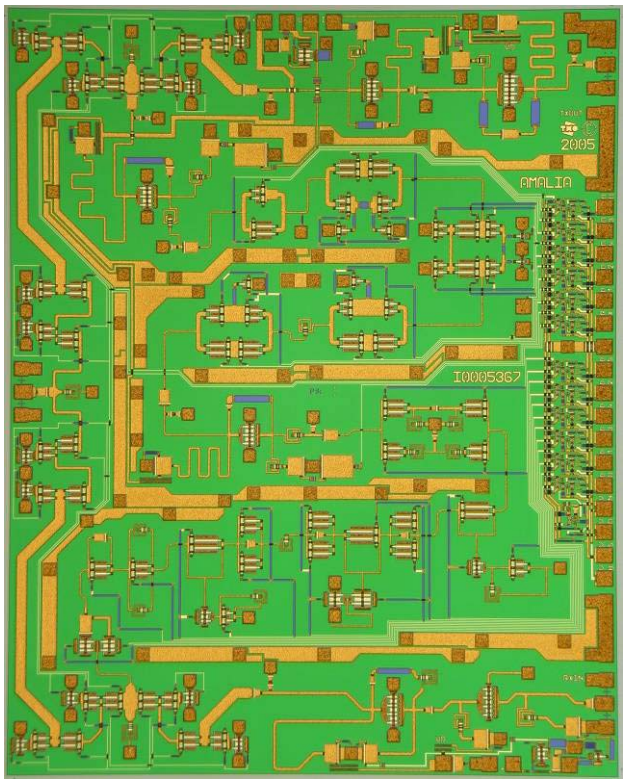

Fig. 2. Photograph of the Multi Function Chip (4.0 x 5.0 mm).

The MFC has been automatically characterized by on-wafer measurements using a wafer stepper probe station. In total 149 MFCs have been measured and 123 have been found functionally correct. The measured small signal gain, input and output matching are shown in Fig. 3. The gain is more than 27 dB from 8 to 11.5 GHz.

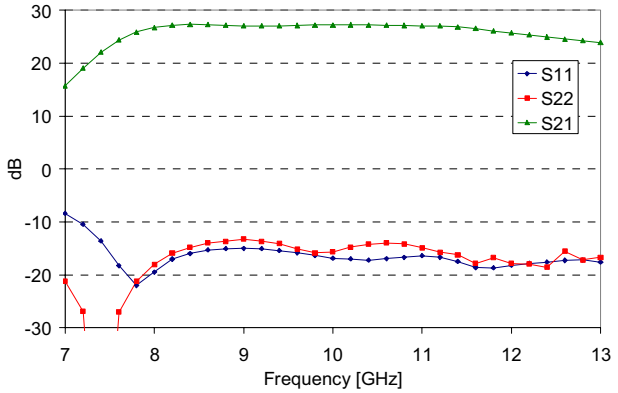

Fig. 3. Measured S-parameters of a typical MFC MMIC in receive mode at maximum gain setting.

Fig. 4 and 5 shows the measured Noise Figure and input P_{-1dB} of the entire receive chain at maximum gain setting for a representative number of samples. The Noise Figure is between 2.0 and 2.5 dB from 8 to 13 GHz and the input 1 dB gain compression point is around -13 dBm.

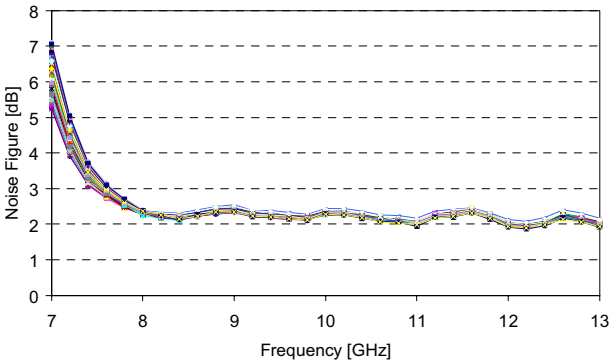

Fig. 4. Measured Noise Figure of 25 MFC samples in receive mode with maximum gain setting.

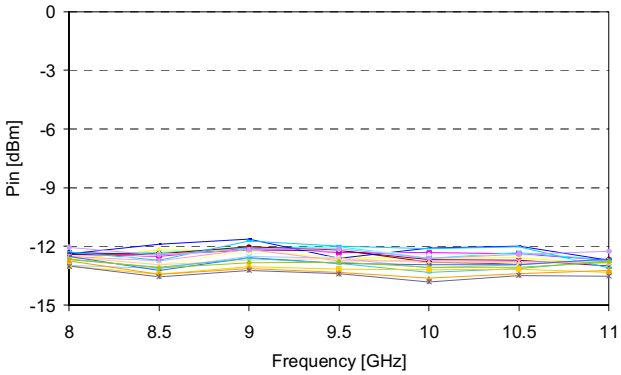

Fig. 5. Measured input P_{-1dB} compression for 20 MFC samples in receive mode with maximum gain setting.

Figures 6 to 9 show the attenuator and phase settings versus frequency as well as the RMS phase error over all attenuator and phase settings.

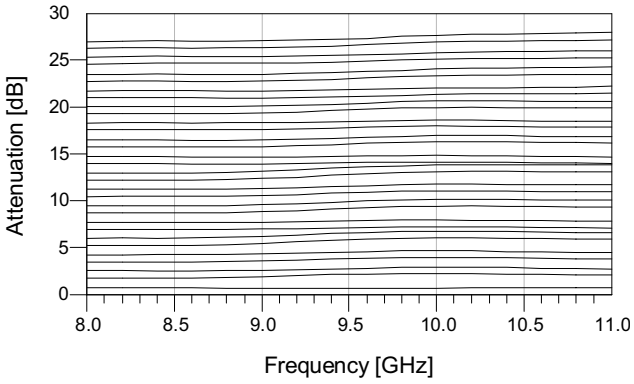

Fig. 6. Measured attenuation-frequency plane, referenced to the maximum insertion gain setting.

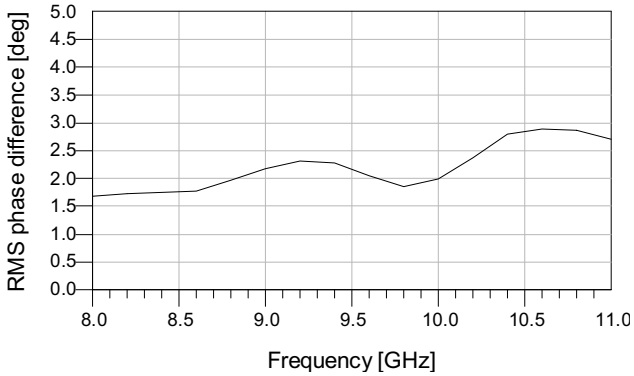

Fig. 7. RMS phase error over all attenuator states.

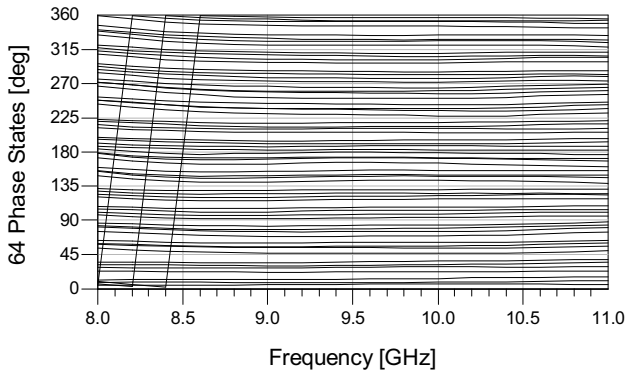

Fig. 8. Measured phase-frequency plane, referenced to an arbitrary phase state.

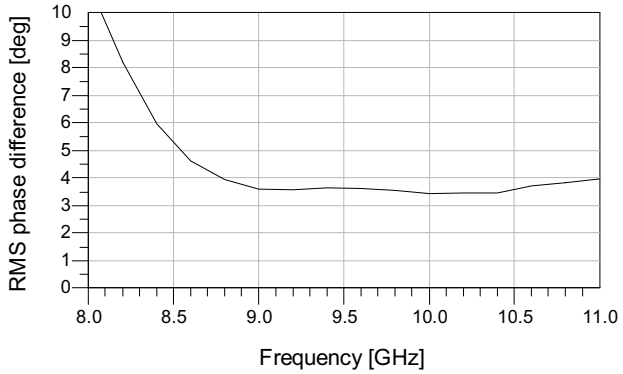

Fig. 9. RMS phase error over all phase states.

Fig. 10 shows the isolation measurement at the receive port, while the MFC is operating in transmit mode. The obtained isolation of better than 30 dB is very good, considering the fact that the total on chip gain is more than 40 dB. The isolation is very important since any transmit signal that couples externally from the Tx output to the Rx input (e.g. via the circulator or electromagnetic coupling over the DC bondwires) can cause instability. As mentioned earlier, much attention has been paid in the design to increase the isolation and with respect to the previous design iteration, the isolation has improved from around 15 dB to 30 dB.

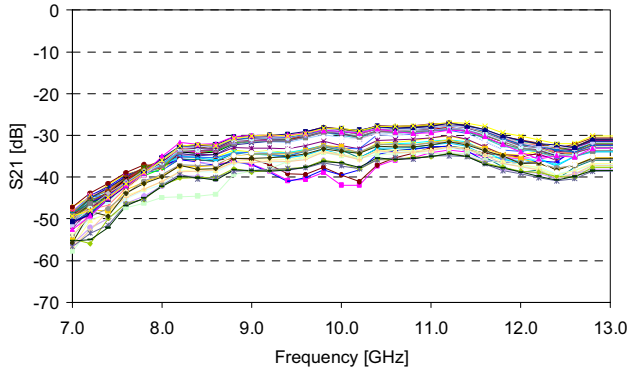

Fig. 10. Measured isolation at the receive input while the MFC is operating in transmit mode.

Finally Fig. 11 shows the measured P_{-1dB} ouput power of the transmit chain with maximum gain setting. The output power at 1 dB gain compression is more than 19 dBm up to 10.5 GHz. The measured saturated output power is more than 21 dBm over this frequency range.

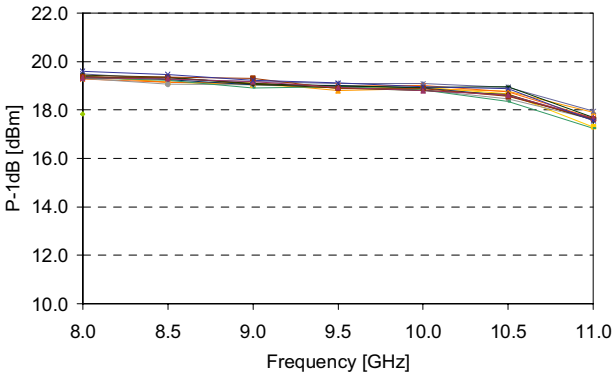

Fig. 11. Measured P_{-1dB} output power of 15 MFC samples in transmit mode with maximum gain setting.

III. High Power Amplifier

The X-Band HPA has been designed to be used together with the MFC. The HPA is a 3-stage design and includes an active gate bias circuit to compensate for technology spreading and temperature. The design goal is 10 Watt output power at X-band with at least 24 dB gain under pulsed conditions. The design has been based on the approach described in [6]. The photograph of this MMIC is shown in Fig. 12.

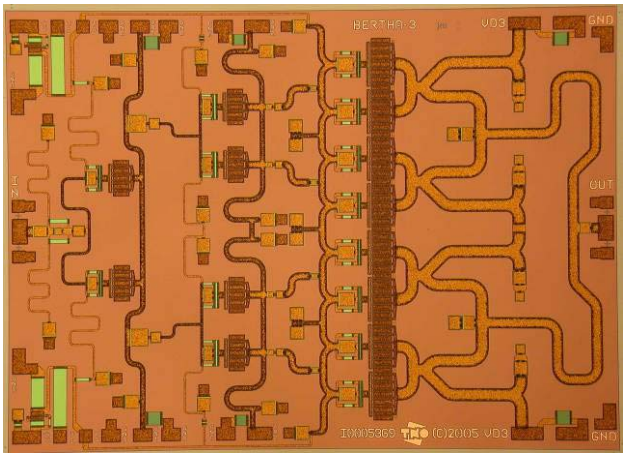

Fig. 12 Photograph of the 3-stage HPA (4.90 x 3.55 mm).

The measured S-parameters of a typical sample are plotted in Fig. 13, showing a small signal gain of more than 25 dB from 8.5 to 10.5 GHz. The on-wafer measurements of 334 samples on 2 wafers have shown an excellent DC and small signal yield of more than 87 %.

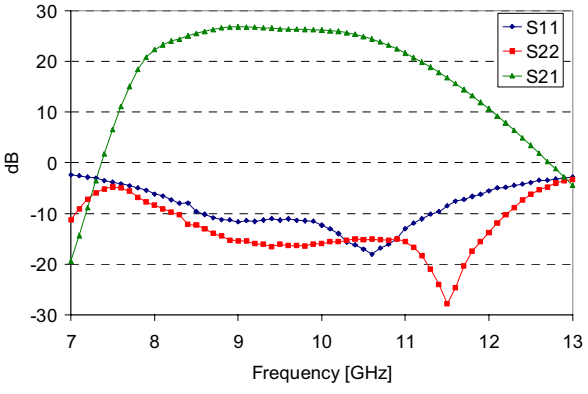

Fig. 13. Measured on-wafer S-parameters of the HPA MMIC.

Fig. 14 shows the spread of the measured S21 of 120 samples from one wafer. Because of the active gate bias circuit 89 % of the functional samples are within a +/- 0.5 dB spread window.

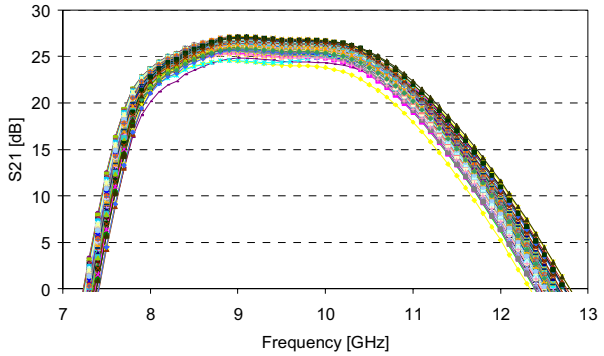

Fig. 14. Measured on-wafer S21-parameter of 120 HPAs.

Pulsed large signal measurements have been performed on a typical HPA MMIC mounted on a metal carrier. Barcaps have been included on the carrier to provide high frequency decoupling of the bias, which is supplied by a DC multi contact probe wedge on the barcaps. The measurements have shown one instable area around 10.5 GHz and input powers above 10 dBm, which might be caused by the not so good low frequency bias decoupling. Therefore the measurements are only shown up to 10 GHz and even the measurements at 10 GHz might be influenced by this instability. The following three figures show the measured power gain, output power and Power Added Efficiency (PAE). The measured power gain under pulsed conditions is between 29 and 30 dB. The maximum measured output power is 39.7 dBm at 9.0 GHz with 46 % PAE, which are excellent results.

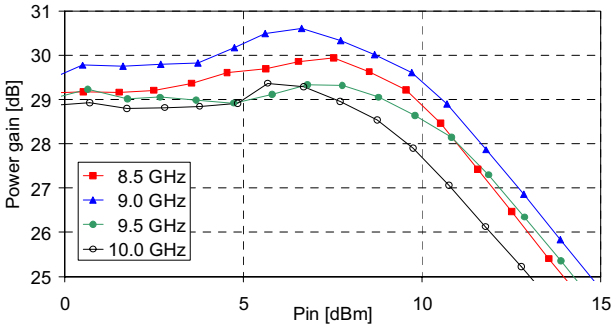

Fig. 15. Measured large signal power gain from 8.5 to 10 GHz.

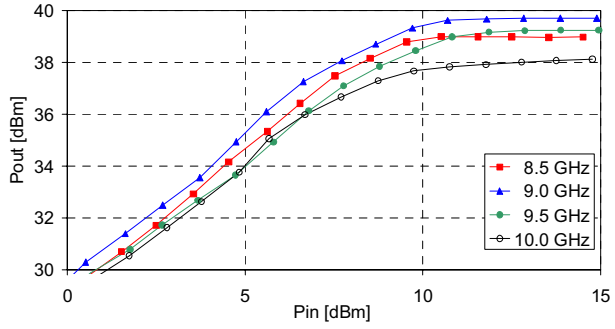

Fig. 16. Measured large signal output power from 8.5 to 10 GHz.

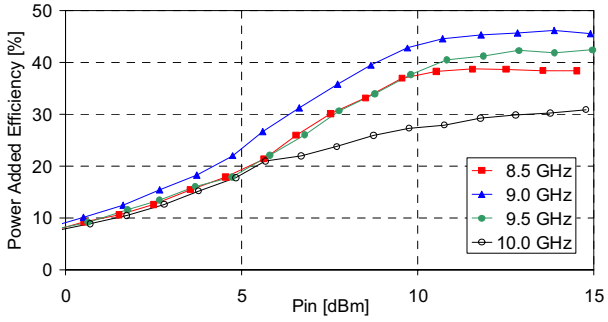

Fig. 16. Measured PAE from 8.5 to 10 GHz.

Currently work is in progress to design a new test fixture with better low frequency bias decoupling in order to solve the remaining large signal instability.

VI. Conclusion

The design of a Multi Function Chip and High Power Amplifier chipset for X-band phased array T/R modules has been successfully accomplished. The MFC is based on an earlier design iteration and has been improved on a.o. reduced MMIC size, LVCMOS digital control, improved isolation and active biasing for temperature and process variation. The design shows excellent performance with more than 21 dBm saturated output power and 2.5 dB Noise Figure. The HPA measurements show a very good DC and small signal yield and excellent large signal results of 39.7 dBm output power with 46 % PAE at 9.0 GHz.

Acknowledgement

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