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Crossbar arrays of nonvolatile, rewritable polymer ferroelectric diode memories on plastic substrates

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In this paper, we demonstrate a scalable and low-cost memory technology using a phase separated blend of a ferroelectric polymer and a semiconducting polymer as data storage medium on thin, flexible polyester foils of only 25 µm thickness. By sandwiching this polymer blend film between rows and columns of metal electrode lines where each intersection makes up one memory cell, we obtained 1 kbit cross bar arrays with bit densities of up to 10 kbit/cm^2. © 2014 The Japan Society of Applied Physics

Organic electronics technology has developed rapidly. Fueled by the vision of the "Internet of Things", many research activities in organic electronics focus on contactless identification transponders or smart labels.[1,2) The development of reprogrammable nonvolatile memory (similar to the well-known flash memory) is essential for storing information in such applications. In almost all foreseeable applications, multiple memory devices are needed to store a multiple number of bits. The cross-bar-type memory array device, where the resistance switching material is interposed between intercrossing word and bit lines, is the most promising structure in this regard. This configuration allows for a high integration density owing to a minimal footprint of $4F^2$, with F being the minimum feature size. The extreme parallel geometry of the crossbar array, however, requires the implementation of a certain selection device to prevent read disturbance problems. Implementing a Schottky-type diode with each resistance switching element can be a solution to this problem—as was demonstrated in single cells.[3–7) Cho et al. demonstrated the construction of a 4 × 4 crossbar memory device with hybrid-type devices consisting of an inorganic Schottky diode and organic unipolar memory components.[8) However, it is highly beneficial that the resistance switching device would inherently possess rectifying characteristics, as, for example, possible with diodes containing a blend of an organic semiconductor and a ferroelectric polymer.[9) A 3 × 3 crossbar array on glass illustrated that it is possible to integrate these ferroelectric diodes in crossbar arrays, without the need for transistors or other additional electronic components.[10) However, the bit density was low, less than 3 bit/cm^2. In a theoretical study, Kemerink et al. calculated that the maximum bit density for this memory technology could be as high as 1 Gbit/cm^2.[11) This has prompted us to investigate experimentally the scaling behavior of the semiconducting/ferroelectric blend memory diodes, both in terms of device area as well as array size.

Discrete memory diodes and arrays of different sizes are processed on 25-µm-thick plastic substrates (DuPont Teijin Films Teonex® PEN Film) that are temporarily glued to a 150 mm silicon wafer support. The anode layers were deposited by e-beam evaporation of gold and patterned using standard photolithographic techniques. Next, a 200-nm-thick continuous film of a 1 : 9 w/w blend of poly(9,9-di-*n*-octylfluorene-*alt*-benzothiadiazole), F8BT, and a ferroelectric copolymer of vinylidene difluoride and trifluoroethylene, P(VDF–TrFE), with 77 mol% VDF, is formed by spin coating the polymers in an initially homogeneous evaporative solution, followed by a thermal anneal at 135 °C for 1 h to facilitate the ferroelectric ß-phase growth. The polymers demix spinodically, which, owing to the low semiconductor-to-ferroelectric volume ratio, leads to a dispersed phase consisting of pillarlike semiconductor domains embedded in a ferroelectric matrix.[12) Finally, the column electrodes are evaporated through a shadow mask. We used BaAl and Au as the top electrode. The chemical structures of the materials used are shown in Fig. 1(a). F8BT forms a (hole) injection barrier of ~0.8 eV with gold. The work function of BaAl matches the LUMO energy of F8BT, yielding an ohmic contact for electron injection.

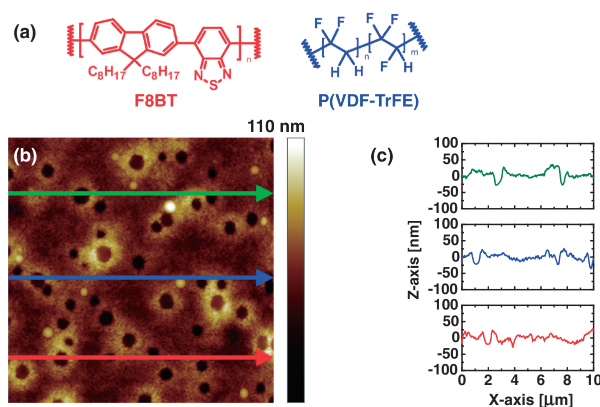

Fig. 1. (a) Chemical structures of F8BT (red) and P(VDF-TrFE) (blue). (b) AFM topography image (total vertical scale 110 nm, 10 × 10 µm^2) of a P(VDF-TrFE):F8BT (9 : 1 w/w) blend on Au electrode. (c) Line scans measured at position indicated in image (b).

Figures 1(b) and 1(c) show an atomic force microscopy (AFM) topography image and three line scans of the F8BT/P(VDF-TrFE) blend layer, respectively. The phase-separated morphology is characterized by nanometer-sized circular domains of F8BT surrounded by a P(VDF-TrFE) matrix. The diameters of the F8BT domains are typically about 300–700 nm. Asadi et al.[13) and Khan et al.[14) reported similar phase-separated morphologies using either a different polymer or molecular semiconductor. By carefully optimizing the solvent and processing conditions, we obtained smooth films with a low R_{rms} surface roughness of 10 nm, as measured by AFM. This leads to a high device yield close to unity. Using a

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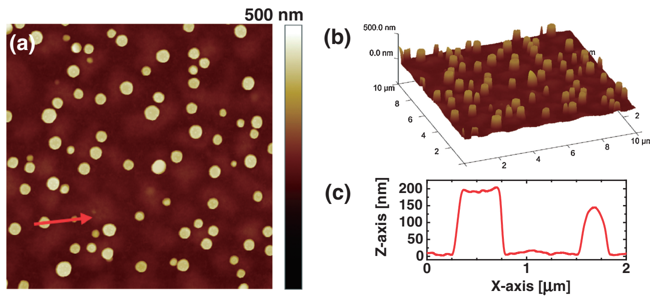

Fig. 2. (a) Topography and (b) corresponding 3D AFM image obtained after selectively dissolving P(VDF-TrFE) phase from the polymer blend (total vertical scale 500 nm, $10 \times 10\,\mu m^2$) (c) Line scans over two different types of F8BT domain.

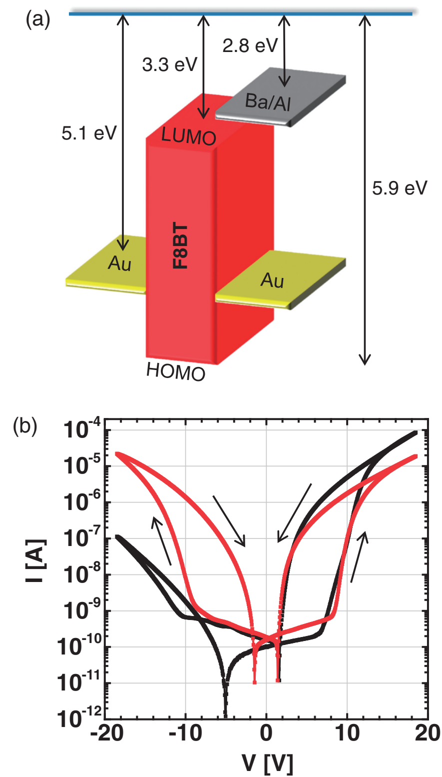

Fig. 3. (a) Band diagram of Au/F8BT/Ba (Au) diode. (b) Current vs voltage hysteretic sweep of memory switches. Au was used as bottom contact metal; the top electrode was either Au (red line) or BaAl (black line). Arrows indicate the voltage-scanning direction.

selective solvent that dissolves the ferroelectric polymer but not the semiconductor, we obtained more information on the three-dimensional (3D) structure of the blend. Figure 2(a) shows AFM topography measurements obtained after P(VDF-TrFE) is selectively removed. The remaining structures are therefore attributed to F8BT on top of the bottom electrode. Most of the semiconducting domains fully percolate the layer, as the height of the domains closely equals the thickness of the initial blend film. A minor fraction of domains are less high in these AFM images. This leads us to believe that these particular domains do not fully percolate to the top electrode and will not contribute to the charge transport in the final device. We also find evidence of a semicontinuous thin wetting layer of F8BT. A comprehensive study of the 3D morphology of phase-separated memory blend films will be published elsewhere.[15)]

A schematic of the band diagram and current vs voltage hysteretic sweeps of discrete memory switches are shown in Figs. 3(a) and 3(b), respectively. The ferroelectric layer, because of its remnant polarization, can adopt either of two stable remnant polarization states. The stray field of the polarized ferroelectric modulates the injection barrier at the metal-semiconductor contact, leading to bistable current switching.[11,16)] Because the ferroelectric polarization remains when the power is turned off, the information is nonvolatile. In our devices, ferroelectric polarization reversal already occurs at a low voltage of ~10 V. This value is close to the coercive voltages determined in the capacitors with corresponding P(VDF-TrFE) layer thickness. When the electric field exceeds the coercive field of P(VDF-TrFE), the hole injection barrier of Au is modulated, and the forward current is markedly increased. Applying a sufficiently large negative voltage reduces the hole injection barrier of the top electrode in the case of using Au. As a result, a close-to-symmetric current–voltage characteristic is measured for the Au-active layer-Au device. The large hole injection barrier of F8BT/BaAl, however, cannot be overcome, which effectively results in a low current at negative voltages compared with the Au top electrode. The ON current of the BaAl diode is 74 ± 9 nA at a gate bias of 7 V (measured over 42 devices). The average OFF-current is 42 ± 21 pA. The current modulation, therefore, exceeds 10^3. With Au as the top electrode, the ON current of 24 ± 7 nA and OFF-current of 55 ± 24 pA yield an average ON/OFF ratio of 450. Note that the OFF current is likely dominated by nonintrinsic effects as slow depolarization and ionic movement, as witnessed by the nonzero current at zero bias. All diodes can be repeatedly programmed and erased for at least 100 times without a significant change in current. After 100 program-erase cycles, the ON current decreases by a factor of ~4. The OFF current remains constant.

F8BT is an ambipolar semiconductor, and it has been intensively utilized for organic light-emitting diode (OLED) applications. We observed its typical green electroluminescence in the BaAl diode at positive biases (albeit faintly because we used opaque/refractive electrodes in this study). This suggests ambipolar injection. Such electroluminescence was not observed in the diodes with Au bottom and top electrodes, suggesting that electron injection is negligible in these diodes and they can be regarded as hole-only devices. The larger forward current in the BaAl diode is therefore explained by the injection and transport of electrons, and enhanced (space-charge-limited) hole current.

Transient switching was studied by measuring the device current at 7 V after programming pulses of various widths, magnitudes, and polarities [Fig. 4(a)]. When we define the switching time as the pulse width at which the ON-to-OFF transition and OFF-to-ON transition intersect, the switching time decreases roughly exponentially from ca. 10 ms for pulses of ±10 V ($1 \times E_c$) to ca. 10 µs for pulses of ±20 V ($2 \times E_c$). It is found to be independent of the top electrode material [Fig. 4(b)]. These switching times are considerably longer than the ferroelectric polarization switching times of the corresponding capacitors,[17)] but are substantially shorter than the previously reported values for polymer ferroelectric transistors.[18)]

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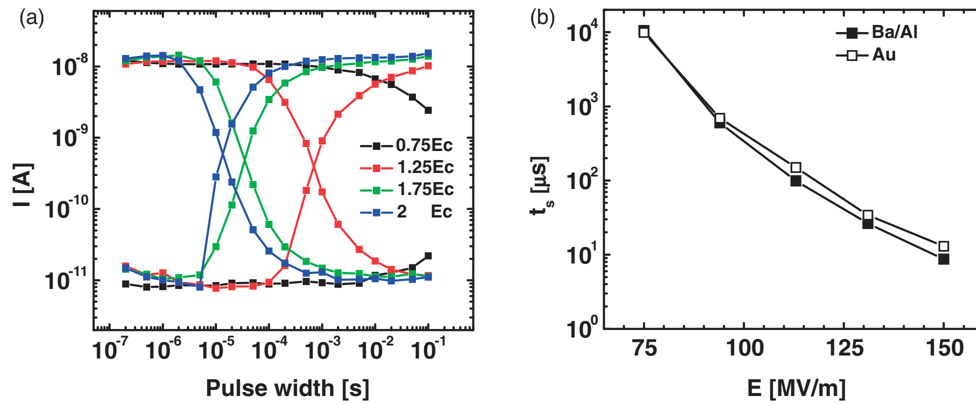

Fig. 4. (a) Switching time measurements of Au-active layer-Au diode. Diode currents were measured at 7 V after programming pulses of different pulse widths and heights. (b) Switching speed of Au-active layer-Au and Au-active layer–Ba/Al diodes plotted as a function of E.

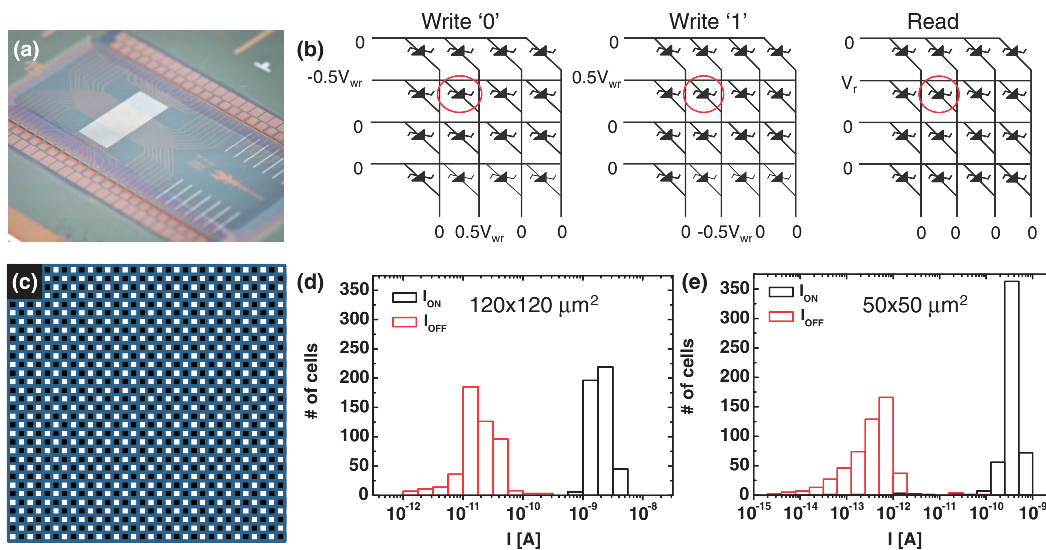

Fig. 5. (a) Photograph of 1 kbit crossbar array with 120 × 120 μm^2 memory elements on plastic. (b) Addressing scheme used to write and read the memory arrays. (c) Neighboring cells were programmed alternatingly to the "0" and "1" states in the so-called checkerboard pattern. (d, e) Measured output current of 1 kbit arrays with different sizes of active memory element, F, in $4F^2$ array.

Low-temperature large-area processing of thin blend layers of F8BT/P(VDF-TrFE) has been upscaled to 150 mm flexible foil-based substrates. The discrete device yield was close to unity, allowing us to fabricate the largest reprogrammable organic nonvolatile memory arrays on flexible substrates reported to date. Figure 5(a) shows a photograph of the 1 kbit flexible memory diode array consisting of 32 × 32 memory cells with an active area of 3 × 3 mm^2.

In these crossbar arrays, the F8BT/P(VDF-TrFE) blend is sandwiched between rows and columns of metal electrode lines where each intersection makes up one memory cell. The active area was determined by the width of both electrodes, either 120 or 50 μm. The spacing between electrodes was also either 120 or 50 μm, leading to a $4F^2$ crossbar array. To program a memory cell in a crossbar array, its row and column are set to $-V_{wr}/2$ and $+V_{wr}/2$, respectively. All other rows and columns are kept to GND (ground) [Fig. 5(a)]. This ensures that no other junction is charged with V_{wr}. Even though most unaddressed cross points experience no voltage, all unaddressed cross points along the addressed row and column experience a disturbing voltage of $\pm V_{wr}/2$. Therefore, it is important that the ferroelectric material can retain its polarization state when disturbed by such a voltage. In this respect, it is important to note that the time required to switch our memories is a highly nonlinear function of the applied voltage (Fig. 4). This property is advantageous because it allows the memory state in a crossbar array to be rapidly set (less than 10 μs) at reasonable switching voltage amplitudes of ±20 V, while it remains unperturbed at the half-disturb voltage of 10 V. The arrays were thus programmed in a checkerboard pattern and subsequently read out. Reading is performed by the application of the read voltage V_{read} of 7 V in one row, whereas all other rows are floating and columns are grounded. At a V_{read} of 7 V, the ratio of ON current to OFF current reaches the maximum of 10^3. Alternative reading schemes in which the nonselected rows and columns are set to a nonzero voltage result in even lower disturbing voltages. These alternative reading schemes have, however, the disadvantage that additional voltage levels are required.

Figures 5(d) and 5(e) show the device currents of all devices in the arrays with the BaAl cathode and 120 × 120 and 50 × 50 μm^2 device areas. Scaling down the device area

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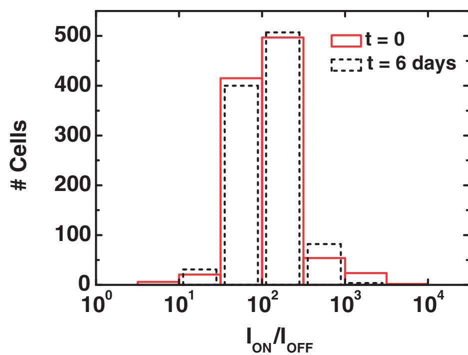

Fig. 6. Histograms of ON/OFF ratio of 1024 memory cells (area, $120 \times 120\,\mu m^2$) directly after programming and after 6 days.

by a factor of ∼6, from 120×120 to $50 \times 50\,\mu m^2$, results in a decrease in the average ON current of the same magnitude. Hence, no scaling effects are found for a bit density up to 10^4 bit/cm^2. The ON and OFF currents are distinctly separated by more than two orders of magnitude; consequently, the programmed checkerboard pattern can easily be recognized. There is no systematic drift of the parameters along rows or columns. Similar results were obtained for the 1 kbit array with the Au cathode. Figure 6 shows a histogram of the ON/OFF current ratio directly after programming and after 6 days. Good data retention is observed. This indicates that the nonuniformity is largely due to variations in cell parameters. Other possible factors such as repetitive application of $V_{wr}/2$ during programming, repetitive application of V_{read} during readout, and data retention loss due to depolarization with time do not significantly affect the polarization state of nonselected diodes.

For the further evolution of these memory arrays, the inherent physical and possible technical limitations to scaling are most important. In our current approach, one ultimate limitation is the lateral leakage between neighboring word and bit lines. Asadi et al. showed that the lateral current dropped to essentially zero when the electrode spacings were larger than the domain size of the polymer semiconductor.[13] An essentially zero current was observed for spacings of 2 µm or more. This suggests that the interelectrode distance can be reduced to a few micrometers before the lateral leakage current will become important. Another limitation is obviously set by the size of the active area, and therefore, the width of the word and bit lines. A smaller device area denotes lower readout currents that, in general, require more sophisticated peripheral sense electronics, but also, a smaller device area will result in a larger device-to-device variability owing to the stochastic variation in the number of semiconducting domains. The minimal area is set by the demand that the variation in current owing to the varying number of domains in single bits is much smaller than the ON/OFF ratio. From AFM measurements, as shown in Fig. 1(b), we estimate that $4F^2$ arrays can be scaled down further to $F = 5\,\mu m$.[19] Further downscaling would require better control over the spatial position and diameter of the semiconducting domains.

In summary, we have demonstrated a scalable and low-cost memory technology using a phase-separated blend of a ferroelectric polymer and a semiconducting polymer as data storage medium on thin, flexible polyester foils of only 25 µm thickness. By sandwiching this polymer blend film between rows and columns of metal electrode lines where each intersection makes up one memory cell, we obtained 1 kbit crossbar arrays with bit densities of up to 10 kbit/cm^2. It is interesting to note that the choice of electrode metals determines the reverse current in these devices. Hence, simply changing one of the electrodes transforms the system from an active memory element to a passive selection device or vice versa. This implies that in addition to non-volatile memory, these ferroelectric devices can also be used as reconfigurable switches in field-programmable gate-array (FPGA)-type logic, diode resistor logic, routers, or multiplexers.

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19) From the AFM measurement on a $10 \times 10\,\mu m^2$ area [Fig. 1(b)] we can get an impression on the short range variability. In total 47 F8BT domains cover 15% of the total surface area. The largest number of active domains, 14, is found in the lower right ($5 \times 5\,\mu m^2$) quadrant. The lowest number of 10 is found in the upper right ($5 \times 5\,\mu m^2$) quadrant. This variability is still low compared to average on–off current ratio and its spread (we measured in discrete, large area devices 1800 ± 400). We therefore believe that the technology can be scaled to $4F^2$ arrays with $F = 5\,\mu m$.

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