A multi-channel S-band FMCW radar front-end

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***Abstract*— This paper describes the design and performance of a low-cost synthesized FMCW radar module, operating in S band. The bi-layer PCB contains a frequency-agile low phase-noise synthesizer and three identical coherent receive-channels. The transmit channel has an automatic power control system that reduces the output power when a large reflection causes the receiver input level to exceed the linear input range. Standard surface-mount components from commercial WLAN applications have been used to create a versatile programmable radar module.**

The DDS-based PLL synthesizer achieves a SSB phase-noise level of -101 dBc/Hz @ 10 kHz offset from a 2.4 GHz carrier. A basic serial PC interface enables control of the FMCW radar parameters that can be stored in the on-board non-volatile memory. The complete front-end operates from a single 3.6 - 5.5 Volts supply, drawing 220 mA and measures only 55 x 100 mm.

I. Introduction

FMCW radar systems are often the preferred choice for low-cost, simple radar systems, for applications as diverse as height sensing and presence detection.

This paper describes the implementation of one, typical, front-end which was originally designed for short-range 3-D "through-the-wall" radar imaging applications, although it has found much wider applications.

The original application required a USB-powered (mobile) multi-channel front-end, which could later be interfaced with a portable signal processing device. Different antennas and measurement set-ups were envisaged.

The design needed a careful balancing between performance and production cost. The wide application area forced relatively stringent performance requirements and at the same time forced absolute cost limits.

II. Design Features

To accommodate for the wide application range, several features were added to make the front-end fail-safe and flexible:

- One example of this flexibility is the fact that the maximum output power can be selected by changing the value of the on-board attenuators, to adapt the transmit power for the antenna used, keeping the EIRP below the maximum value according to the IEEE802.11b standard.
- A second example of this flexibility is the implemented ability to program the FMCW radar parameters through a simple RS232 connection and store them in the internal non-volatile memory.

Direct switching between two different pre-defined sweep-profiles is provided by an on-board DIP-switch.

III. Detailed Design

A block schematic of the complete module is shown in Figure 1.

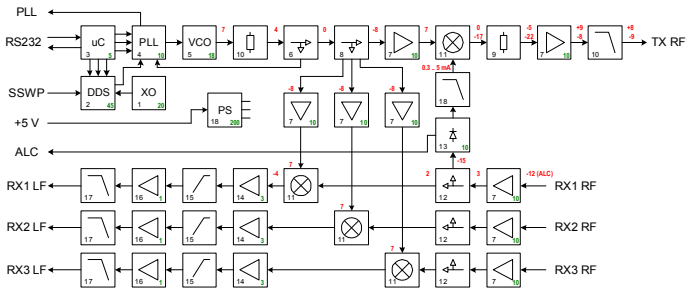

Fig. 1 Block diagram of the implemented front-end

As can be seen in the block diagram, a single DDS-PLL synthesizer combination was chosen to generate the microwave signal. Signal levels are indicated in the block diagram in red. Due to the integration of receiver and transmitter on a single board, re-use of the transmitted signal for down-conversion in the receiver could be implemented in a straightforward manner.

Multiple identical receivers were implemented in such a way that additional receivers could be added without major redesigns.

A. Frequency Synthesizer design

A 400 MHz commercial Direct Digital Synthesizer (DDS) IC is used, running at an on-board generated 125 MHz clock-frequency for a reduced the supply current. The DDS can now be programmed to generate sinusoidal output signals up to 50 MHz with a very low spurious content of typically less than -70 dBc.

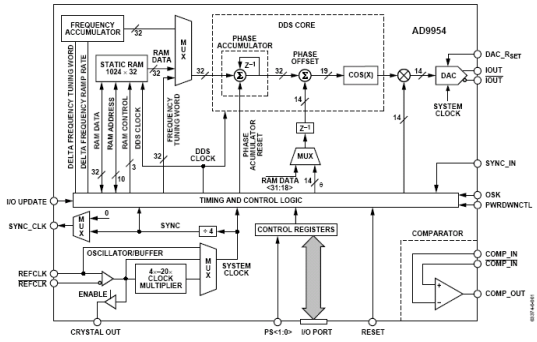

Fig. 2 Block-diagram of the DDS used (from AD9954 datasheet)

An external low-pass filter is required to remove the image frequency from the 14-bit resolution DAC output.

The particular DDS used also has the ability to generate a programmable automatic linear sweep. The sweep sequence is started immediately after the detection of a trigger signal on the trigger input of the device.

The DDS output signal is fed to the reference frequency input of a standard integrated Phase Locked Loop (PLL) IC. A low-voltage commercial 2400 MHz VCO is used which is then phase-locked to the DDS output signal, using a fixed divider ratio. In this way, the DDS output is effectively multiplied in frequency from 50 MHz to 2400 MHz.

PSPICE was used to simulate the critical parts of the circuit, in particular for the synthesizer system. A behavioural simulation model was made (shown in figure 3) for the PLL system to evaluate the transient behaviour of the loop as well as the phase-noise level of the output signal.

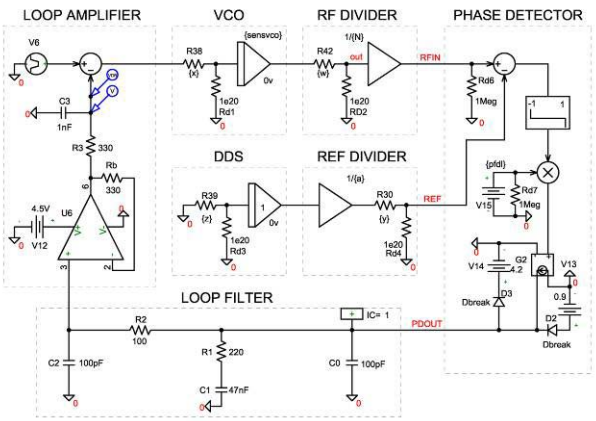

Fig. 3 PSPICE behavioural model for the PLL system

The circuit was optimised for sufficient transient response and lowest possible phase-noise level. The final loop bandwidth was set a 250 kHz, enabling sufficient tracking capability of the PLL at DDS sweep durations down to 50 µs. The simulated phase-noise level is shown in figure 4 and includes the noise-contributions from the 125 MHz Crystal Oscillator, the VCO, the DDS, the digital phase-detector of the PLL and the loop-amplifier and loop-filter electronics.

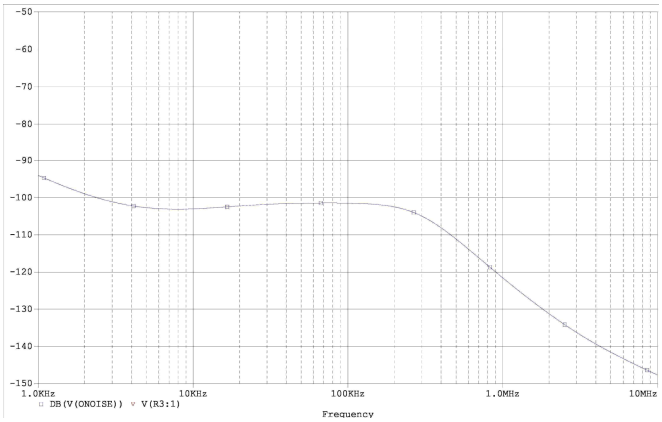

Fig. 4 Simulated SSB phase-noise of the 2400 MHz DDS-PLL

Since both the DDS and the PLL circuits need to be programmed and have a serial interface, a simple microcontroller is selected to perform this essential task at the start-up of the power-supply. Multiple other functions have been added, such as:

- An RS232 interface to remotely change the PLL and DDS parameters and store them in the non-volatile memory
- A buffered PLL Lock Detect Error output
- Sensing of the on-board DIP-switch to directly select between 2 different sweep-profiles without using the RS232 interface
- On-board generation of a programmable DDS sweep trigger signal (alternative to connecting an external trigger input signal)

B. RF & DC distribution

To be able to distribute both RF and DC from the synthesizer and the power supply circuit to the different channels of the module using a single metal layer, the DC signal from the power supply is superimposed on the RF output signal of the synthesizer. The RF signal is then split into 4 RF output signals using small surface-mount Wilkinson power splitters, capable of carrying the required DC current.

C. Receiver channel design

Each of the three receiver channels is basically identical and has a Local Oscillator (LO) & DC input, an RF Receive (RX) input and a Low Frequency (LF) output containing the down-converted beat-note signal of the radar. A coupled RF output port is designed, making it possible to measure the received signal power at the input of the mixer, which will be used to prevent the receiver channel from being overloaded by the signal from a very strong reflection. The schematic is shown is figure 5.

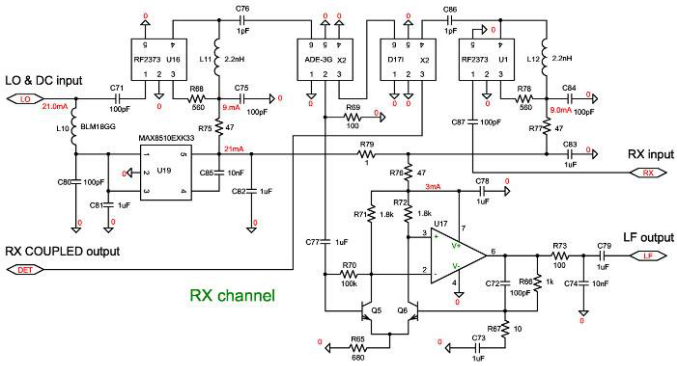

Fig. 5 Single receive channel schematic

The amplification of RX and LO signals is performed by low-power low-cost RF ICs from RF Micro Devices. The impedance matching is done using lumped inductors and capacitors (0603-size).

The current consumption of the complete receive channel is approximately 21 mA, at a supply voltage of 3.6 Volts. The overall conversion gain (RF in to LF out) is approximately

50 dB and the double side-band (DSB) noise-figure is around 7 dB.

D. Transmit channel design

Part of the transmit channel is identical to the receive channels; both the LO buffer-amplifier, the mixer and the power supply circuits are the same. In the transmit channel, the mixer is going to be used as an amplitude modulator for the transmit signal, forming part of the Automatic Level Control (ALC) system which will be discussed in the next paragraph. For this system, the necessary RF detector circuit (AD8314) is included in the transmit channel. An additional "ALC active" on-board indicator LED and a digital output signal are provided to warn that the input signal of the RX channel has exceeded its linear input range. The exact power level for the loop to be triggered is settable by a DC voltage (selected by choosing a resistor-value).

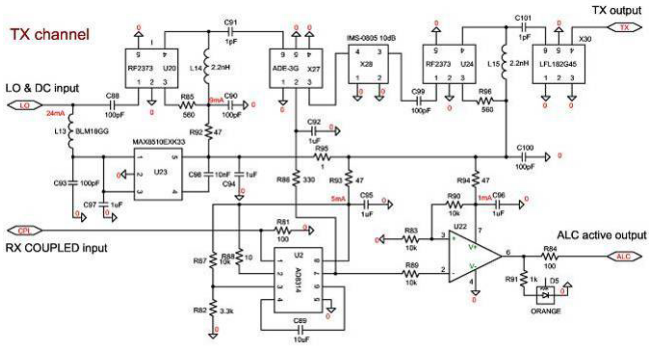

Fig. 6 Transmitter channel schematic

The basic transmit chain consists of a buffer amplifier, an amplitude modulator, a fixed attenuator to set the nominal output power level, an output amplifier and a low-pass filter to be able to both comply with CE regulations concerning maximum EIRP levels and spurious output. The settable output power is used to adapt the generated power to the gain of the specific antenna used, keeping the EIRP close to the maximum allowed value for maximum system dynamic range.

The total current consumption of the transmit channel is 24 mA from +3.6 Volts, and the output power can be set from -2 to +8 dBm. The amplitude modulator is able to further reduce the output power by 15 to 20 dB.

E. Automatic Level Control system

The Automatic Level Control (ALC) system has been implemented to avoid RF overload of the receiver input caused by reflections from large objects close to the antenna. When the input signal of the receiver exceeds its linear range, the gain will be decreased causing an increase in the effective noise figure and the radar will become less sensitive. In order to avoid this situation, part the RF input signal of the receiver is fed to a rms detector IC, and compared with the maximum linear input level for the receiver. When the input level exceeds this value, the transmitter power is automatically lowered (which offcourse directly influences the received signal level) until the receiver signal level is back to the linear input range.

In order to model the behaviour of the ALC and prevent unstable operation, a behavioural model has been designed and implemented in PSPICE, as shown in figure 7.

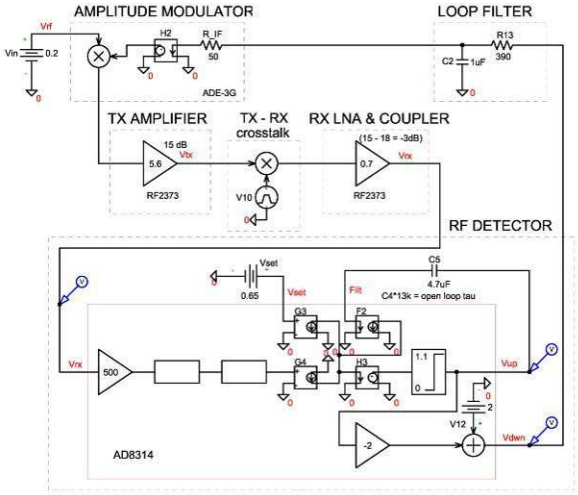

Fig. 7 Behavioural model of the ALC system

In the model, DC voltages are used to describe the envelope of the RF signal, making the simulation both fast and simple to implement. The loop gain is dependent on the signal level itself since the amplitude modulator (consisting of a balanced mixer) works completely linear while the RF detector IC (AD8314) only has a logarithmic output (V/dB). However, stable operation has been demonstrated with the set-up as shown, yielding a very simple system with a low number of components.

IV. REALISATION

The complete circuit was implemented on a bi-layer printed circuit board (PCB) using 8 mil thickness RO4003 substrate material, to make the module both low-cost and easily accessible. The synthesizer part is fully separate from the transmit and multi-channel receiver part. The only interconnection is a single micro-strip line, carrying both the RF signal from the synthesizer as well as the DC bias voltage for the TX and RX channels. This set-up makes modification of the front-end to a larger number of channels quite easy.

A photograph of the module is shown in figure 8; the individual blocks can easily be recognised; frequency synthesizer, receive and transmit channels and the LO & DC distribution.

Although the circuit uses relatively large components (all passives are 0603-size or larger), each complete receiver channel and the transmit channel only measure 15 x 30 mm (excluding connectors). The placement of metal shielding parts is facilitated by several grounded metal strips surrounding the circuits. The actual required shielding will be dependent on the mechanics and the specifications of the system in which the module is used.

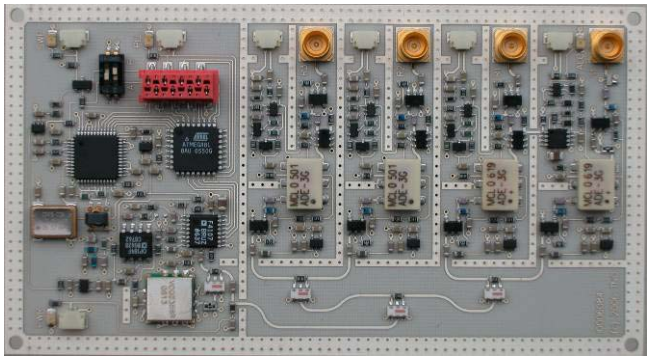

Fig. 8 Photograph of the assembled front-end

SMP surface-mount RF connectors are used because of their small size and high reliability. Furthermore, a very good and reproducible impedance-matched transition from micro-strip to coax is guaranteed by the design.

V. Measurements

The full module was characterised in-house; the module was functioning in one pass. Its main specifications are summarised in the table below.

TABLE I
S-band module performance summary

Parameter	Specification
Frequency range (programmable)	2290 – 2500 MHz
Sweep time (programmable)	50 to 100000 µs
Transmit power (setting range)	-2 .. +8 dBm
Harmonics (DC - 26.5 GHz)	< -47 dBc
Spurious output signals	< -70 dBc
Transmit power reduction range by ALC	> 17 dB
Receiver typical DSB noise figure	7 dB
Maximum receiver RF input level (P1dB)	-12 dBm
Maximum receiver RF output level (P1dB)	+10 dBm
Receiver output LF bandwidth (-3 dB)	200 kHz
Power Supply voltage	3.6 - 5.5 Volts
Power Supply current	220 mA

The SSB phase-noise of the transmit signal was measured and found to be close to the simulated value. The result is shown in figure 9.

The measured conversion (voltage) gain from RF input to LF output, and the Double Side-Band (DSB) Noise Figure is shown in figure 10. Note that the plot uses a logarithmic scale for the x-axis. The roll-off in conversion gain for lower frequencies is deliberately done, to avoid clipping of the output signal for close-by reflections (low frequency signals).

The RX channel-to-channel amplitude and phase matching makes accurate direction finding applications possible, as well as small phased array applications using digital beam forming techniques.

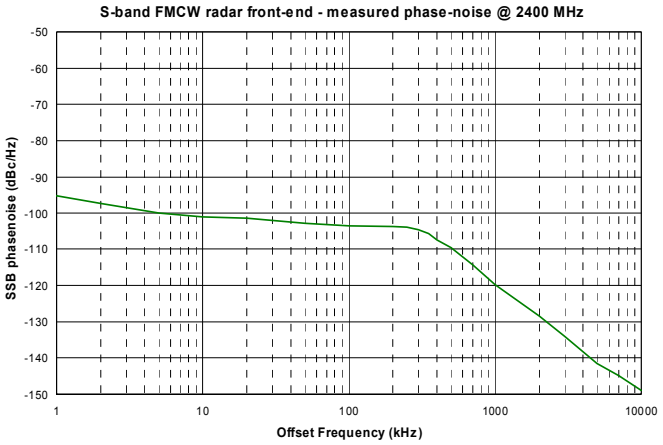

Fig. 9 Measured SSB phase-noise of the transmit signal

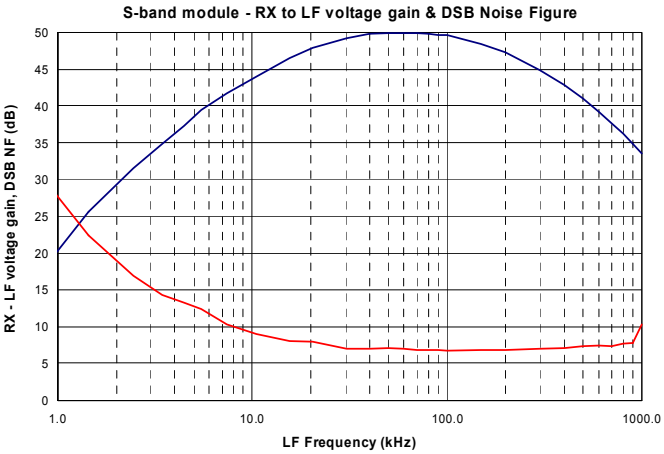

Fig. 10 Measured conversion gain and DSB noise-figure

Typical sweep-settings for the module are a linear up-sweep from 2400 to 2483.5 MHz in 900 µs, yielding a maximum range (@ 200 kHz LF) of 320 meters. Several other settings are possible, creating a large number of possible applications, ranging from short to medium range systems.

VI. Conclusions

A versatile S-band FMCW radar module has been designed and realized on a single board. Low-cost technology and components deliver high performance, due to careful design, dimensioning and layout. With the ability to be "USB-powered" the front-end is especially useable in portable multi-channel radar-systems.

Acknowledgment

The authors wish to thank the mechanical prototype department for the fast and accurate assembly of the front-end.

References

[1] *AD9954 Direct Digital Synthesizer*, datasheet, Analog Devices, 2003.