Technological and Physical Compatibilities in Hybrid Integration of Laser and Monolithic Integration of Waveguide, Photodetector and CMOS Circuits on Silicon

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Abstract

In this paper, technological and physical compatibilities in hybrid integration of AlInGaP laser and monolithic integration of ZnO monomode waveguide, *pin*-photodetector, CMOS circuits for laser power control and signal amplification on silicon substrate are studied. Prospective problems and their possible solutions are discussed. Also experimental results are presented.

1. Introduction

Opto-electronic systems, based on complete integration of optical and electronic components on one single silicon chip, show many advantages due to compactness, rigidness, small size, the prospect of cheap batchwise mass production, low loss, high speed and avoidance of the need of alignment of optical parts and independent packaging. In this paper, we report results of the study of technological and physical compatibility for an optoelectronic integrated circuit (OEIC) in which however the light source is incorporated hybridically. This OEIC has to be considered as a general platform for integrated optical processing or sensing circuits.

The principal structure of the OEIC is shown schematically in Fig.1. Light, emitted from a laserdiode, is coupled into an integrated optical waveguiding system. A small part of the light is coupled into a photodiode by use of an optical interconnect function to control the laser output power. In addition it serves as a measure for the magnitude of the input signal of the optical circuit. The remaining light will continue to propagate in the waveguide and will be modulated in the optical circuits by the measurement. The optical output signal is totally coupled into a second photodiode. After amplification, the electrical signal is fed to the output. The ratio between output and sensor input signal is the outcome of the measurement, the exact relation depending on the specific optical circuitry that has been applied.

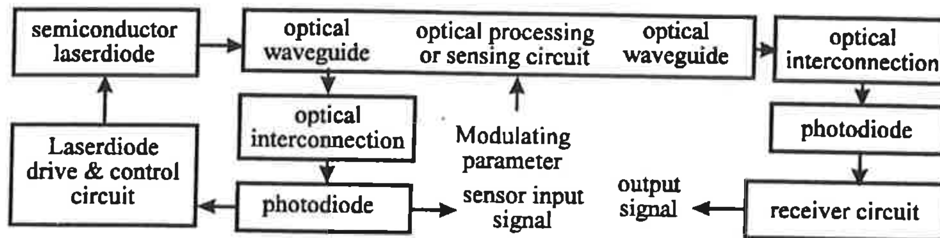

Fig.1. Principal structure of the OEIC.

It has been decided to concentrate initially on systems with bandwidth < 10 KHz, high dynamic range and resolution. In a later stage, higher bandwidths (up to 100 MHz) will be put into focus. The applied wavelength will be 675 nm.

2. Technological Compatibility

The technologies used in this system include BiCMOS technology for the electronic circuits and the photodiode, optical interconnection technology, waveguide fabrication technology and laser mounting technology. Therefore, the technological compatibility should be studied and the prospective problems should be solved.

For the reasons of materials incompatibility at high temperature processing it is required that first all the electronic components including the photodiode are made, followed by the low temperature processes used for optical interconnections, the waveguide fabrication and the laser mounting. Thus compatibility problems were reduced to two main questions: (1) can degradation of microelectronics by subsequent optical technologies be avoided ? (2) how to realise a microelectronics system, that is a good platform for the integrated optical parts ?

The main results of our investigations are detailed in the next sections.

2.1 Influence of Waveguide Fabrication on Microelectronics

The low-loss, uniform planar waveguide, as shown in Fig.2, is made by reactive RF sputter deposition of ZnO [1] on the SiO_2 buffer layer. After deposition, the ZnO film is annealed at 400 ^{o}C for four hours to reduce the optical attenuation. Higher annealing temperatures should be avoided because they will cause contact failure in microelectronics. The channel of the ridge waveguide is etched by Argon sputter-etching.

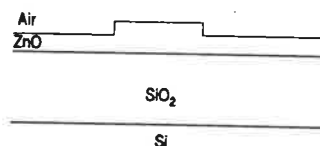

Fig.2 ZnO waveguide structure

A test chip containing diodes, capacitors and CMOS transistors was used to study the influence of the waveguide fabrication process on the microelectronics. Changes in leakage current, capacitance-voltage (CV) characteristics and threshold voltage were used to characterize the subsequent fabrication steps. The changes we observed were only minor and do not seriously alter the operation of the electronics. Zn diffuses quickly at 400 ^{o}C and it

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gives rise to mid-gap levels. So one would have expected a change in generation life time, and thus of leakage current and CV characteristics. The reason why this phenomenon is not observed may be explained by the fact that Zinc is strongly bounded to Oxygen in ZnO and that the solid solubility is low at 400 °C. Also there presents a diffusion barrier of SiO_2.

2.2 Influence of Laser Mounting on Microelectronics

The laser is an AlInGaP ridge waveguide laser emitting at 675 nm. It is mounted epi-down in an anisotropically etched well by means of a thermocompression method as shown in Fig.3 [2]. Multiple metal layers are evaporated on the substrate, after which the gold coated laser is pressed on the heated substrate.

The influence of the laser mounting on the microelectronics is now under investigation. Similar test structures as mentioned in section 2.1 are used to investigate the process. The first experimental results show a negative shift of MOS threshold voltages. A probable explanation is contamination, especially from Na^+ ions, This may be caused by aceton cleaning or handling of the chips or the photoresist developer which we found contains Na^+. More detailed experiments are still going on.

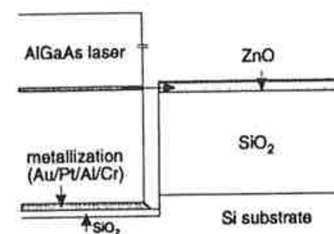

Fig.3 Laser mounted in Si substrate

2.3 Realisation of Grating Structures

In this OEIC system, a grating system is used to couple the light out of the waveguide and into the photodetector as show in Fig.4. This grating is realised by the etching of the waveguide. For higher wavelength a second grating has to be added [3] that will be realized at the surface of the silicon wafer. To realise that surface grating structure, we introduced an additional LOCOS field oxidation during the fabrication of the microelectronics, that is compatible with the standard LOCOS in the BICMOS technology. Of course, the process conditions for the first LOCOS need a minor adjustment.

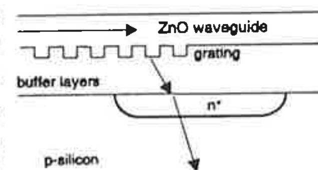

Fig.4 Grating system

2.4 Optical Buffer Layer Structure

The waveguiding layer has to be separated from the Si by an optical buffer layer in order to avoid Si-caused attenuation of the light propagating through the waveguide. The buffer layer thickness is required to be larger than 1 µm. In addition, it is required to be as uniform and smooth as possible. Since the PLOX (plasma-oxide) layer in BiCMOS technology is not appreciated by the optical system due to its higher refractive index, we introduced an additional lithographic process step to delete the PLOX layer at the waveguiding circuitry area.

Now for the buffer layer, there are two options: (1) 0.5 µm BPSG (SiO_2 doped with boron and phosphorus) + 1.0 µm CVD oxide. (2) 0.5 µm BPSG +1.0 µm sputtered oxide. After

ZnO deposition, it was found that only the second option results in an acceptable optical attenuation. Therefore, the sputtered oxide is a better basis for the ZnO growth.

3. Physical Compatibility

The integrated system is illustrated in Fig.5.

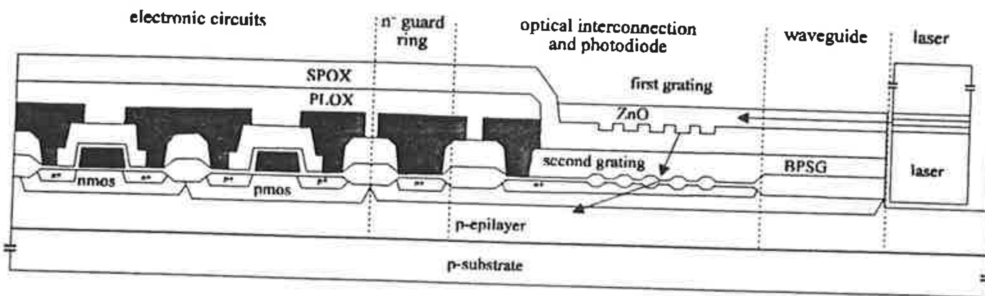

Fig.5 Cross Section of the structures.

In this system, the starting material is a p-epitaxial Si layer on a p^+ substrate. The integrated circuits are made by standard BiCMOS technology. The advantages of BiCMOS technology include very low static power dissipation, excellent noise immunity, and low sensitivity to ionising particles, which is very important in optoelectronic applications.

Integration of optical and electronic components asks for a discussion of spurious interactions between them.

4.1 Isolation Between Laser and Substrate

The polarity of the laserdiode in the epi-down configuration is not compatible with the silicon substrate; therefore an electrical isolation between the laser and the Si substrate is needed; there are three choices (1) laser mounted in a well inside the Si substrate, after sputtering of an additional SiO_2 layer. (2) laser mounted in a well inside the SiO_2 layer, automatically isolated by the remaining SiO_2. (3) laser mounted in a well inside the SiO_2 layer, isolated by an additional sputtered SiO_2 layer. After investigation, we concluded that the first option is the most practical because the others require thick oxide buffer layers (>2 um) which may crack.

The electrical connection between the laser and the driver circuit can be realised by means of bonding wires.

4.2 "Cross Talk" Behaviour

The "Cross Talk" behaviour includes both the electronic and optical effects.

The electronic cross talk occurs mainly between the photodiode and the electronic circuitry. This effect is mainly caused by photon induced carrier diffusion in the substrate. To minimise or eliminate this interaction, a spatial separation and the introduction of a diffused guard ring is foreseen, as shown in Fig.5.

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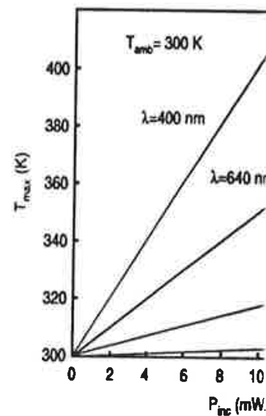

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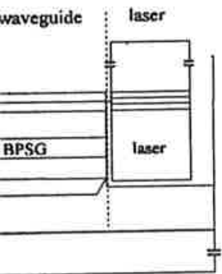

The opto-electronic cross talk is caused by light, propagating in the ZnO layer, outside the waveguide channels. This scattered light originates from imperfect laser-waveguide coupling. If absorbed in the Si, it will influence the performance of the electronic devices. To eliminate influence on the electronic devices, we introduce a light-blocking layer to cover the microelectronics.

4.3 Thermal Behaviour Consideration

The thermal influence could be of great importance in the final OEIC. It is found that the laserdiode (120 mW dissipation) and the driver electronics are the main heat sources. There are two kinds of thermal problems which should be considered. One is the effect of self-heating of components. The other is the influence between different components. In first instance a 2-D numerical simulation was developed to study the temperature distribution in the system [4].

First, we studied the temperature rise due to the photon absorption in the photodiode. The calculation was performed for several wavelengths and power densities. It showed that the maximum local temperature T_{max} is reached at the surface of the photodiode. Furthermore T_{max} increases with the incident power density and decreases with the wavelength. The self-heating can be neglected if the incident power is less than 1 mW/μm^2 for λ=675 nm as shown in Fig.6.

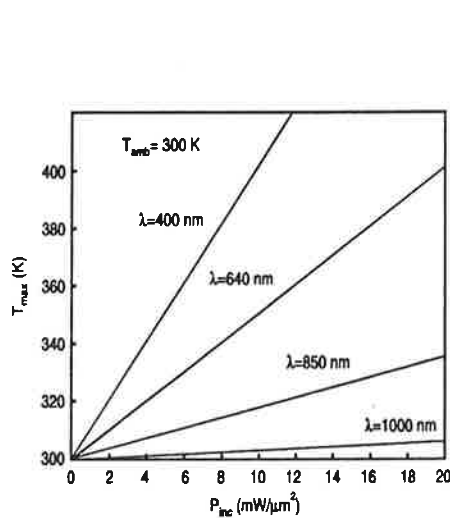

Fig.6. Maximum temperature in Si as a function of incident power for various wavelengths.

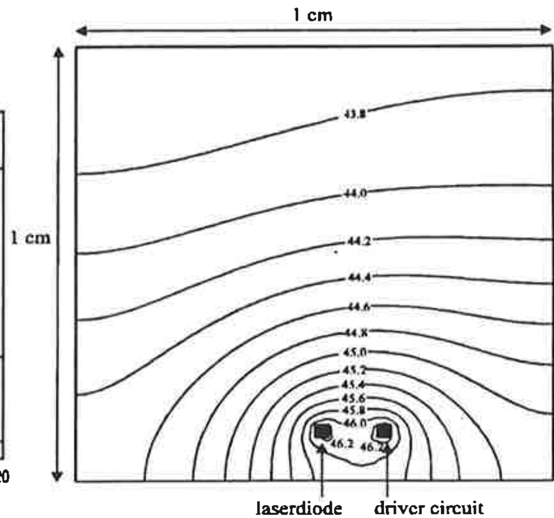

Fig.7. Temperature distribution in the OEIC at its working state.

Fig.7 shows the simulation results of the temperature distribution across the entire chip (thickness 450 μm), assuming that it is surrounded by air. The heat transfer mechanism in air is convection. Both the power dissipations of the laserdiode and the driver circuit are assumed to be 90 mW. It was found that the variation of the temperature over the whole chip is small, this is due to the high thermal conductivity of Si. Note that the temperatures are between 40 -

50 °C above ambient. In practice, due to the use of a heat sink, the increase of temperature on the chip can be reduced significantly and will be less than 10 °C.

5. Conclusions

The technological and physical compatibilities of hybrid integration of laserdiode and monolithic integration of waveguide, photodetector and electronic circuits have been studied. Results show that all the prospective problems can be solved and negative influences can be eliminated or minimised by applying proper methods and techniques.

6. Acknowledgements

The authors would like to thank Tom Aarnink for his processing of the test-chips, Karel Lippe for his help with the measurements, Klaas Hoen and Hans Wallinga for their valuable discussions.

This work was supported by the Dutch Ministry of Economic Affairs via the Innovative Research Program-Electro-Optics under the Project No. EO-TEL92.301.

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Sensor Technology 1994

Proceedings of the Dutch conference
on Sensor Technology 1994

University of Twente
Enschede, The Netherlands

February 17 – 18, 1994

Edited by P.V. Lambeck

This conference has been held under the auspices of the Platform 'Sensor Technology' and the *Dwarsverband*-committee 'Sensor Technology' as part of the STW/NWO Priority-Programme 'Sensor Technology'.