THE PHARUS PROJECT;
REAL TIME DIGITAL PROCESSING OF AIRBORNE POLARIMETRIC RADAR SIGNALS.

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1. ABSTRACT

The Dutch PHARUS project aims for the development of a polarimetric C-band aircraft SAR, to be finalized in 1994.

The PHARUS system consists of three subsystems: the radar, the subsystem for the onboard data processing and recording and the ground-based subsystem for SAR processing.

PHARUS is a very flexible system with numerous operating modes, intended for remote sensing research. Modes vary from a straight forward single mode (e.g. HH polarisation) to a full polarimetric mode with alternating chirp patterns.

This paper describes selected items of the onboard data processing and recording subsystem, as it is under construction now.

Data processing starts with high speed digitization of the offset modulated radar signals. The digitized offset modulated signals are demodulated and re-sampled (in range) to complex base band signals. A low pass filtering and decimation in flight direction is performed. Finally, pulse compression is performed based on FFT and IFFT.

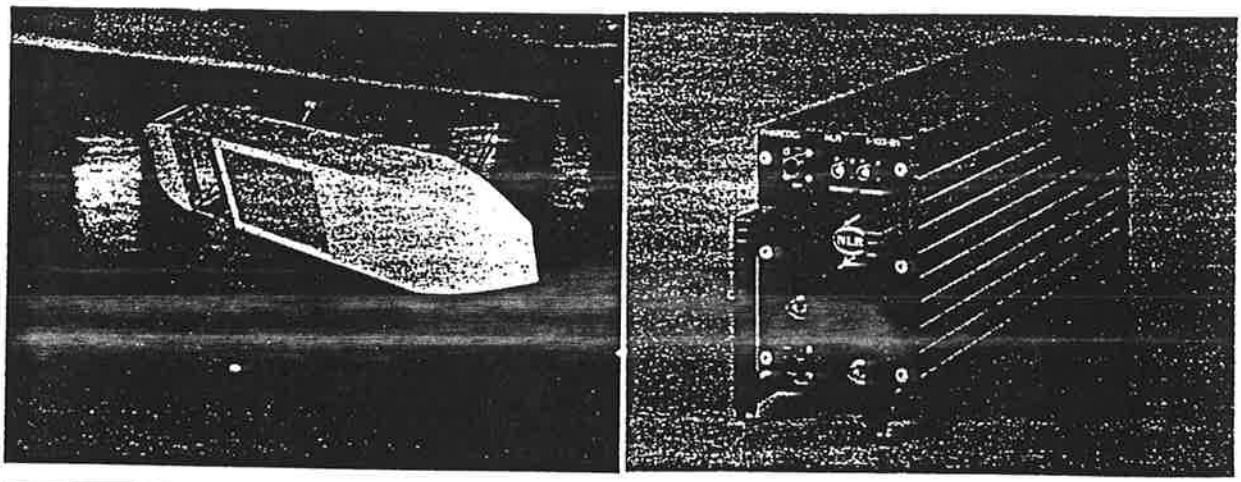
2. INTRODUCTION

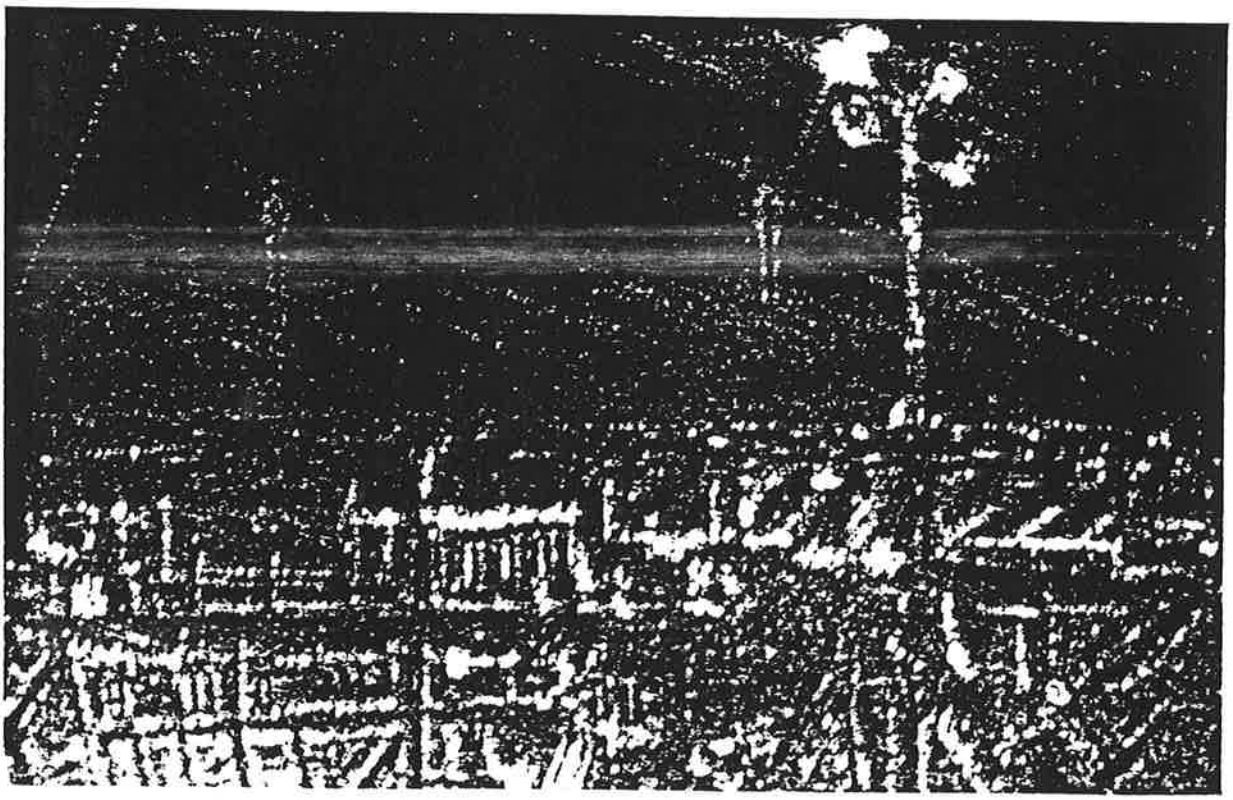
PHARUS is an acronym of PHased Array Universal SAR.
The PHARUS project in the Netherlands aims for the development and construction of a polarimetric C-band aircraft Synthetic Aperture Radar, to be used for Remote Sensing Research.

The PHARUS project is being carried out in cooperation between the Physics and Electronics Laboratory of TNO (FEL-TNO) in The Hague, the National Aerospace Laboratory NLR in Amsterdam and the Laboratory for Telecommunication and Remote Sensing Technology of the Delft University of Technology. Financial support is provided by the Ministry of Defence and the Netherlands Remote Sensing Board (BCRS). On behalf of these partners the program management is carried out by the Netherlands Agency for Aerospace Programs (NIVR).
The project is divided in two main phases: a definition phase and a realization phase. The definition phase started in 1988; the realization phase started in 1990; the system is planned to be ready for flight testing during the 1994 growing-season.

During the definition phase, one of the studies resulted in a flying test-bed which was used to investigate techniques and to spot possible problems. This test-bed PHARS (Phased Array Research System) consists of three subsystems: the subsystem for the radar,
the subsystem for onboard data processing and recording and
the ground-based subsystem for SAR processing.

The left photograph shows the instrumentation pod under one of NLR's laboratory aircraft; the radar is mounted in the centre section. The right photograph shows the box with the PHARS digitizing electronics.



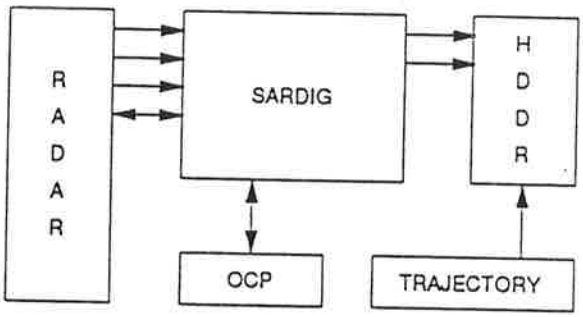


This radar image above gives a detail of an image acquired with PHARS during the second test flight in November 1991 is shown. This three-look image, with a 3x3 m resolution, presents a part of the sea side area of Scheveningen.

The final system, PHARUS, will have simular components, although the single HH polarised channel of PHARS will be extended into a full polarimetric capability for PHARUS. PHARUS will be a very flexible system with numerous operating modes.
The radar section of PHARUS was designed by FEL-TNO.
This paper explains a part of NLR's contribution to the project: the digitization of the radar signals and the onboard data processing prior to the digital recording.

3. SARDIG

SARDIG is the name of the electronics for the digitization and processing of the radar signals (SAR-Digitization).
The position of SARDIG in the PHARUS system is shown in figure 4. The number of connections between the different components is kept to a minimum.



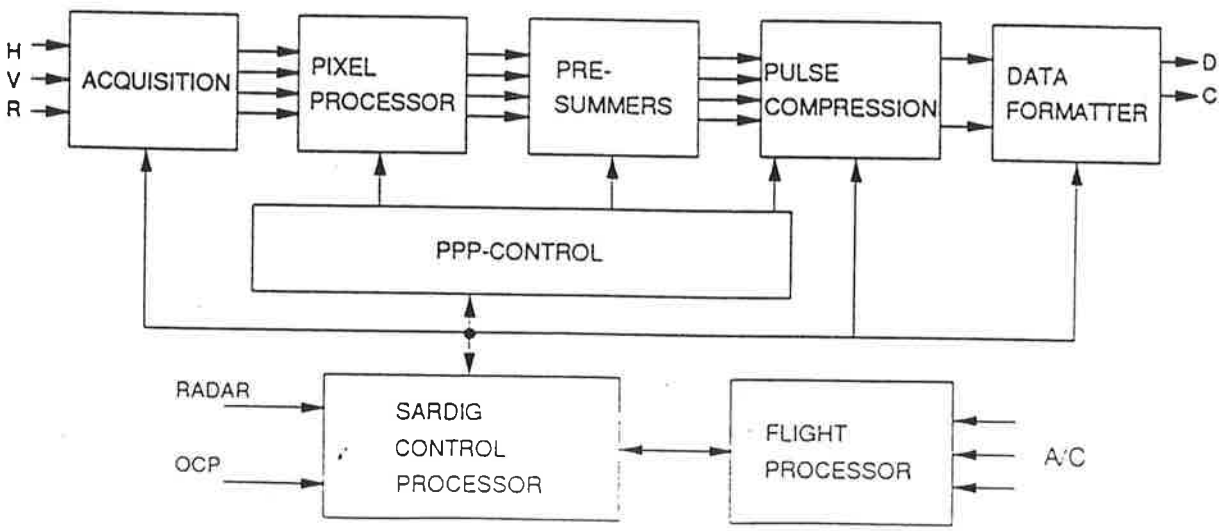
Interfacing with the radar section includes five signals:
- an analog signal (H-receiver),
- an analog signal (V-receiver),
- a digital synchronization signal
- two signals of a bi-directional data link,

Interfacing with the High Density Digital Recording (HDDR) system is by a 16 Mbit/sec serial data link, employing a continuous clock and a formatted data stream.

The PHARUS system is controlled by the Operators Control Panel (OCP), which is a small Personal Computer connected to SARDIG via a standard RS422 data link.

3.1 Organization of SARDIG

The organization of SARDIG will be explained using this block diagram.



The operation of SARDIG is controlled by the SARDIG CONTROL PROCESSOR SCP, which communicates with both the RADAR and the OCP.

The radar signals are accepted by the ACQUISITION block. In this block the two analog signals are digitized using the radar timing signal for reference. The samples in the Radar Range Window are stored in a Range Buffer.

The PIXEL PROCESSOR is controlled by the SCP. The samples are read from the Range Buffer. The processing in the pixel processor consists of code conversion from the ADC codes, conversion from real (offset modulated) samples to complex baseband samples and, if requested, low pass filtering with decimation in range.

In the PRE-SUMMERS the complex samples are filtered and decimated line by line: the corresponding pixels of a number of lines are passed through a programmable FIR filter. Four filters are working in parallel to achieve relative long filters at low decimation rates. The actual FIR characteristic is programmed on the spot by the operator via OCP and SCP.

PPP CONTROL (pixel processor/pre-summer/pulse compression) is the intermediate between SCP and the ACQUISITION, the PIXEL PROCESSOR, the PRE-SUMMERS and the PULSE COMPRESSION. It translates operation modes into control bits and generates the control signals for the three blocks.

The PULSE COMPRESSION block uses a special FFT-chip to compress the chirped pulse with compression factors up to 900. The compression mode is controlled by the SCP.

The DAF block is the Data Formatter which combines the processed Radar data with other data from the PHARUS system and with data on the aircraft trajectory into a programmable format which is suited to be recorded by a bit serial recording system.

The FLIGHT PROCESSOR accepts digital signals both in ARINC 429 and RS422 format from various aircraft systems including a Time Code Generator, a Global Positioning System, and an Inertial Navigation System.
Selected parameters are passed to the SCP and to the DAF block for inclusion in the recorded data. The Flight Processor shares a board with the SCP; data is exchanged by means of a dual ported RAM.

4. DETAILED DESCRIPTIONS

In this chapter a number of features of the SARDIG data handling are described in detail:

- Analog signal format,
- Timing reference extraction,
- Analog to Digital Conversion,
- Digital Coherent Demodulation,
- Range Decimation,
- Azimuth Decimation = Pre-summing,
- Pulse Compression,
- Data reduction by coding.

4.1 Analog signal format.
The coherent information of the analog radar data is transported from the radar to the digitizing electronics by an offset modulated signal.
The two analog radar signals of PHARUS are modulated on a carrier frequency of 25 MHz, having a bandwidth of 40 MHz, so the signal spectrum ranges from 5 - 45 MHz. The sampling frequency of the ADC is 100 MHz, exactly 4 times the carrier frequency.

4.2 Timing reference extraction.
The Timing Reference signal from the radar is a square wave signal which carries three kinds of information.

The reference for the analog signal carrier frequency is a square wave of 25 MHz. This digital signal is isochronous with the unmodulated carrier of the two analog signals.
With a Phase Lock Loop this 25 MHz is transformed into the 100 MHz sampling frequency for the ADC, in such a way that the samples are taken at the phases 0, $\pi/2$, π and $3\pi/2$ of the unmodulated carrier signal.

The reference for the Pulse Repetition Frequency of the radar is generated by omitting one pulse of the 25 MHz reference signal for each transmitted radar pulse. In the PLL this omitted pulse is detected and an internal T=0 marker is generated, which triggers the delay counter for the Range Window. Special action is taken in the PLL to correct the phase error detector for the missing pulse.

The third information is a code which indicates the meaning of the signals sent by the radar. The code can indicate the type of transmission (H or V), the changing of e.g. a gain setting or the progression of a calibration procedure. The code is inserted in the Timing reference signal by conditionally suppressing the three pulses in the 25 MHz signal following the T=0 marker pulse.

4.3 Analog to Digital Conversion.
The Analog to Digital Converter is an 8-bit flash converter. Additional taps on the reference resistor chain are used to generate a segmented characteristic. Small signals are converted with a resolution which is three times the resolution for the signals with a greater amplitude.

4.4 Digital Coherent Demodulation.
Direct digitization followed by Digital Coherent Demodulation is explained and the hardware implementation is indicated below.

4.4.1 Coherent signals digitized.
Analog coherent demodulation of a modulated signal $S(t) = A(t).\cos[wt+\Phi(t)]$ followed by digitizing with two parallel ADC's generates a series of complex digital samples (sampling interval τ_a):

$$I_a(k) := A(k\tau_a).\cos[\ \Phi(\tau_a)\ ], \quad Q_a(k) := A(k\tau_a).\sin[\ \Phi(\tau_a)\ ]$$

Direct digitizing of the same modulated signal with one ADC generates a series of real digital samples (sampling interval τ_d):

$$S_d(k) := A(k\tau_d)\ \cos[\ wk\tau_d+\Phi(k\tau_d)\ ]$$

Digital coherent demodulation is performed by multiplying this series with two digitized reference series $2\cos[wk\tau_d]$ and $-2\sin[wk\tau_d]$ which generates two series of digital samples:

$$I_d(k) := A(k\tau_d).\cos[\ \Phi(k\tau_d)\ ] + A(k\tau_d).\cos[\ 2wk\tau_d+\Phi(k\tau_d)\ ]$$
$$Q_d(k) := A(k\tau_d).\sin[\ \Phi(k\tau_d)\ ] - A(k\tau_d).\sin[\ 2wk\tau_d+\Phi(k\tau_d)\ ]$$

If there is no special relationship between w and τ_d the implementation of the demodulation requires a lot of hardware.

4.4.2 The PHARUS sampling frequency.
In the PHARUS project the sampling interval is defined as $\tau_d = \frac{1}{4}(2\pi/w)$ which results in a sampling grid with a phase step of $\pi/2$.

This sampling grid system simplifies the formulas. The demodulating series are reduced to series of four repeating figures: +2,0,-2,0 and 0,+2,0,-2. The effect on the resulting formulas is:

for k=even: $I_d(k) := 2 * A(k\tau_d).\cos[\Phi(k\tau_d)]$, $Q_d(k) := 0$
for k= odd: $Q_d(k) := 2 * A(k\tau_d).\sin[\Phi(k\tau_d)]$, $I_d(k) := 0$

Decimating by deleting the 0 terms and renumbering leads to:

$I_d(m) := A(2m\tau_d).\cos[\Phi(2m\tau_d)]$
$Q_d(m) := A(2m\tau_d+\tau_d).\sin[\Phi(2m\tau_d+\tau_d)]$

For $\tau_a = 2\tau_d$ the series $I_d(m)$ equals the series $I_a(k)$ and series $Q_d(m)$ looks like series $Q_a(k)$ except for the constant delay τ_d.
Normally this delay is corrected for by a re-sampling (interpolation) of the $Q_d(m)$ series by means of a digital filter (Hilbert filter).

In the PHARUS project is chosen to apply a re-sampling of both series $I_d(m)$ and $Q_d(m)$ to a common grid in such a way that $I_d(m)$ is shifted over $+\frac{1}{2}\tau_d$ and $Q_d(m)$ is shifted over $-\frac{1}{2}\tau_d$. The resulting grid of the complex samples $I_d(n)$ and $Q_d(n)$ corresponds with samples taken at $t = \pi/4 + n.\pi$:

$I_d(n) := A(n.2\tau_d+\tau_d/2).\cos[\Phi(n.2\tau_d+\tau_d/2)]$
$Q_d(n) := A(n.2\tau_d+\tau_d/2).\sin[\Phi(n.2\tau_d+\tau_d/2)]$

The shifting is done by applying two low pass digital FIR filters with a sufficient bandwidth and a linear phase characteristic. The coefficients of the two filters have the same values, only the order is reversed. The advantage is that the amplitude characteristics of both filters are essentially the same while the phase characteristics differ only in sign.

4.4.3 Electronic implementation.
The digital coherent demodulation is performed by the Pixel processor. The reading of the samples of the real signal from the Range Buffer is organized in parallel groups of four called quartets. Each quartet consists of the samples taken at phases 0, $\pi/2$, π, $3\pi/2$.
This means that the multiplication by +2 or -2 and decimation of the factors 0 can be reduced to a simple scaling and sign reversal. One element of a each quartet is always treated with the same scale and sign. The implementation is integrated in Look Up Tables which are also used to straighten the segmented ADC characteristic (see 4.4.1).

The LUT outputs are organized in two series ($I_d(m)$ and $Q_d(m)$) to be re-sampled. In order to achieve a sufficient throughput these series are processed in parallel by in total four FIR filters. Each FIR filter is build using two special FIR circuits (ZORAN ZR33891) working in parallel. A throughput data rate of 25E6 quartets/sec (100E6 samples/sec) can be achieved.

4.5 Range Decimation.
Range Decimation can be selected to increase the swath width at the cost of a reduced range resolution. In this case the radar will reduce the bandwidth of the analog signals but the carrier frequency is not changed. The required sampling rate for the demodulation generates an oversampling for the demodulated complex signals. Reduction is integrated with the demodulation. The bandwidth of the re-sampling filters is reduced and the output is decimated.

4.6 Azimuth Decimation - Pre-summing.
Azimuth decimation is applied to integrate power and to adapt the number of recorded lines per sec to the requirements. Azimuth decimation is weighted pre-summing (FIR filtering) of corresponding complex pixels over a number of consecutive lines.
In order to achieve a good quality of pre-summing (sufficient FIR taps) four pre-summers are active. The pre-summers are controlled to produce their outputs at regular spaced intervals, so for a line decimation of e.g. 1:10 the number of taps available for the FIRs is 4*10=40.

Each pre-summer consists in fact of four identical pre-summer sub-units; each sub-unit handling one I or Q component of one of two complex pixels. Each sub-unit consists of a multiplier adder circuit (LOGIC PRODUCTS LMS12), an 18 bit 8k-word circulation buffer and an output scaler.
The pre-summers are very flexible; by external control the first and last input lines are signalled, filter lengths of 4 - 256 can be realized. Filter coefficients are calculated prior to the measurement by the operators control panel and are sent via the SCP to the PPP-Control. PPP-Control loads all pre-summer at a line basis with the applicable coefficients and with the scaling factor of the output.

Maximum throughput data rate is 25E6 complex pixel-pairs/sec (2*2*9 bits), results are outputted as two parallel 10 bit resolution complex pixels (2*2*10 bits).

4.7 Pulse Compression.
Pulse compression is based on a chip made by Plessey (PDSP16510). This Stand Alone FFT Processor can read, transform and output 1024 complex points in 150 μsec.

As both the reference series and the signal series can be more then 1024 points, a sectioned approach, designed by FEL-TNO, is used in PHARUS to generate the required flexibility and the required compression speed.
Both the signal and the reference are divided into partitions. For each combination of one signal partition and one reference partition the correlation is calculated by a succession of a Fourier transform, a multiplication of the two complex frequency spectra and an inverse Fourier transform.
The main hardware of such a Correlation Processor (CP) consists of two FFT processor chips, a multiplier and some memories.

All sub-results are combined into the final result, taking in account the appropriate time delays.

Depending on the required speed each correlation proces (FFT, MULTIPLY, IFFT) can be performed by one CP or by several CP's in parallel.
PHARUS will apply four CPs in a combination of parallel and series calculations. A maximum throughput rate of e.g. 350 lines per second can be achieved with lines of 8192 complex pixels and a reference pattern of 1024 complex pixels.

4.8 Data reduction by coding.
Owing to the pulse compression the dynamic range of the data of point targets is increased with about 30 dB. In a straightforward I-Q presentation 2*15 bits are required. By this type of coding signals with large amplitudes generate a phase resolution which is much better then required. For PHARUS a phase resolution of the recorded data of 0.09 radians (5°) is sufficient.
Because of restraints of the recording system, only words of 8 to 15 bits long can be accepted; these words will be extended with a parity bit. Total capability of the system is 16 Mbits/sec including housekeeping data etc. (In the future, regretfully not the near future, a modern 100 Mbits/sec recording system will become available).

For PHARUS a binary type of floating point coding of individual complex pixels was chosen: each complex pixel is compressed into a single 14 bit word by a common binary exponent of 4 bits and two mantissas (I and Q) of 5 bits two's complement. The value of the exponent is dictated by the highest absolute value of I and Q.
With this coding the phase resolution for signals with an amplitude of more then 8 varies from 0.03 to 0.12 radians (2° to 7°) and the amplitude resolution varies from 4 % to 12 % (0.3 to 1 dB)
The dynamic range is 15 * 2^15 = 0,5. 10^6 (110 dB), which is sufficient.

5. EPILOGUE

The digitizing of an offset frequency modulated signal with one high speed ADC was succesfully tested with the test system PHARS.

The azimuth pre-summing was demonstrated with PHARS, applying a fixed 32 taps FIR filter.

Pulse compression based on Fast Sectioned Correlation by Fourier Transform is being tested by FEL-TNO in another project.

The onboard digital demodulation and range decimation is new in the PHARUS system.

The schematics and the lay outs of boards for the described functions are finalized at the time of presentation of this paper (mid 1992). The PHARUS system is intended to fly in 1994.

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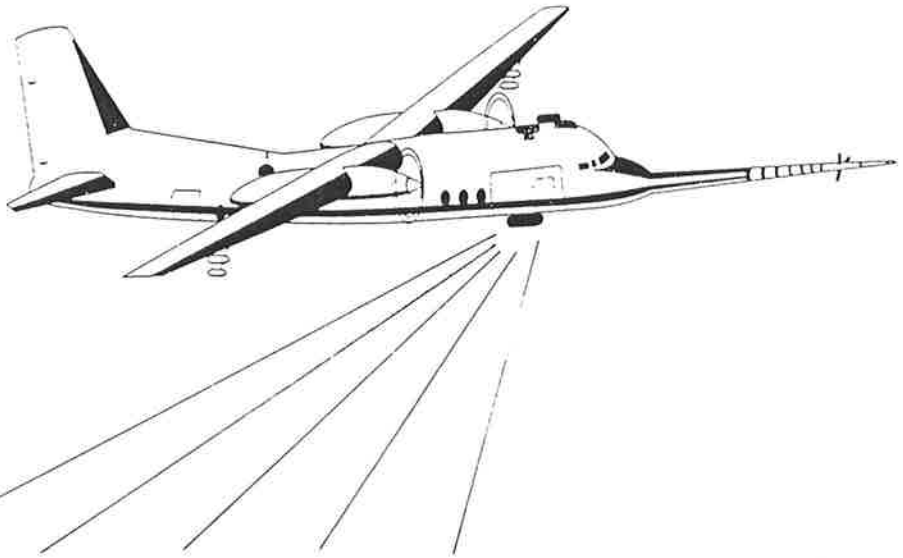
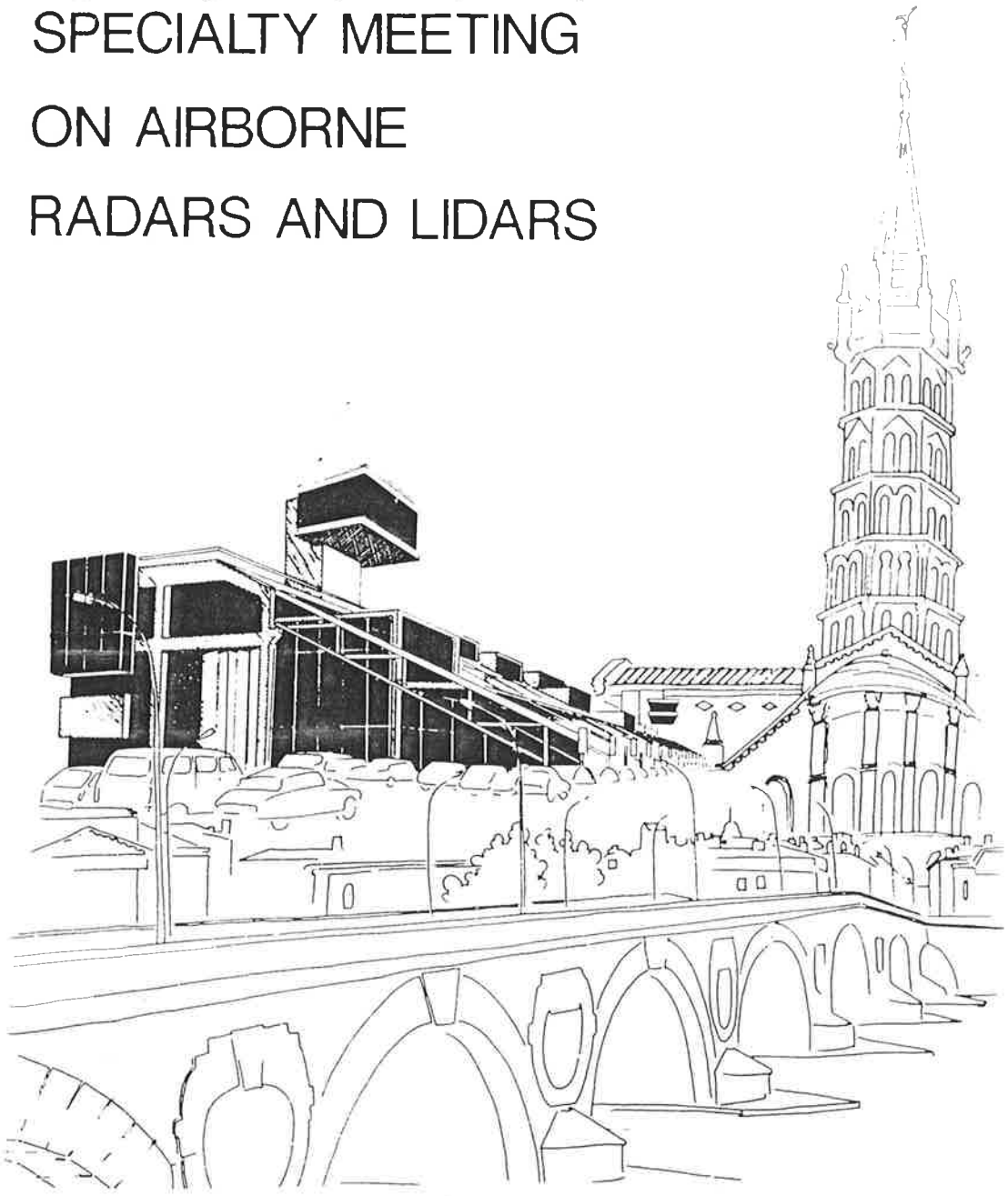


SPECIALTY MEETING ON AIRBORNE RADARS AND LIDARS



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