L-band AlGaN/GaN Power Amplifier with Protection Against Load Mismatch

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***Abstract*— Solid-state power amplifiers need protection at the output to handle high reflections due to mismatch. Normally this is implemented by using a ferrite-based isolator. These are however large and bulky components. This paper presents a Gallium-Nitride power amplifier module with automatic protection against large reflections based on fold-back protection, by sensing the reflected power. Measurements have been performed on a 100 W L-band power amplifier module at full reflection (short at the output) without damage to the amplifier. The reaction time of the protection mechanism is less than 0.5 µs.**

Keywords—High power amplifiers, Gallium nitride, MMICs

I. Introduction

The introduction of Gallium-Nitride (GaN) technology has enabled the realization of small solid-state power amplifiers with very high output power. For practical applications such power amplifiers need some kind of protection against mismatch at the output. In case of full reflection at the output (short or open load) all output power will reflect back to the device causing very high voltage peaks and/or large power dissipation and resulting junction temperature increase. Also during normal operation the load conditions can vary by for example beam steering in a phased array radar. The performance of the amplifier should ideally not be influenced by these changing load conditions.

A standard way of protecting the output of a power amplifier is by using a ferrite-based isolator, see for example [1]. Such a device will dissipate all reflected power in a dummy load and the amplifier will always see the nominal (50 Ω) impedance at the output terminal. An isolator is, however, a large and heavy component and difficult to integrate, especially at lower frequencies, and is limiting the miniaturization and weight reduction of solid-state power amplifiers. This is especially important for space and airborne applications. Another protection mechanism is to use a clamping circuit that senses the voltage peaks at the output of the amplifier [2], but this does not protect against increased dissipation due to reflected power. To protect against the temperature increase due to excessive power dissipation it is also possible to directly sense the temperature near the power transistors [3], but this does not protect against voltage stress. Finally, adaptive output-matching networks could be used to correct for a load mismatch [4], but this only works for a limited range of mismatch and often introduces extra loss in the output-matching network, causing a reduction in efficiency.

This paper presents an automatic protection mechanism that makes use of a reflected power detector and feedback mechanism to reduce the gain of the power amplifier in case of large reflections, also known as fold-back protection. This concept has been demonstrated on an L-band power amplifier using GaN technology from FBH [5]. A similar demonstrator using GaN technology from UMS [6] is currently under test. Section II describes the protection architecture. In section III the design of the power amplifier module is given and in section IV the measurement results are reported.

II. Protection Architecture

A solid-state power amplifier consists of one or more amplifier stages and input, inter-stage and output-matching networks. The output-matching network converts the external nominal load (normally 50 Ω) to the optimum load for the output-stage transistors. This optimum load can be the maximum power load, maximum efficiency load or a compromise between these two. When an arbitrary external load is connected (instead of 50 Ω) the output-matching network transforms this load to a load within a smaller region at the transistor drain reference plane. This is schematically illustrated in fig. 1.

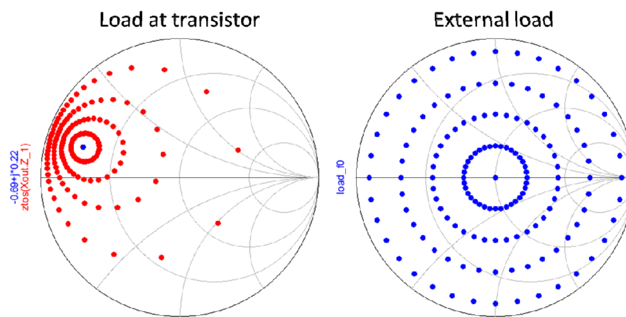

Fig. 1. Example of external load (right) to transistor load (left) conversion.

The non-optimum loads presented to the drain of the transistors will cause the optimum load line to change. This can either cause high voltage peaks or very high dissipation, depending of the phase of the reflection coefficient, and could cause breakdown of the transistor. Fig. 2 shows an example of

a single GaN power-bar with the nominal load line (in red) and two other load lines at VSWR 10: one that presents the maximum voltage stress and one that presents the maximum power dissipation. This maximum power dissipation is more than 2 times higher than the nominal power dissipation.

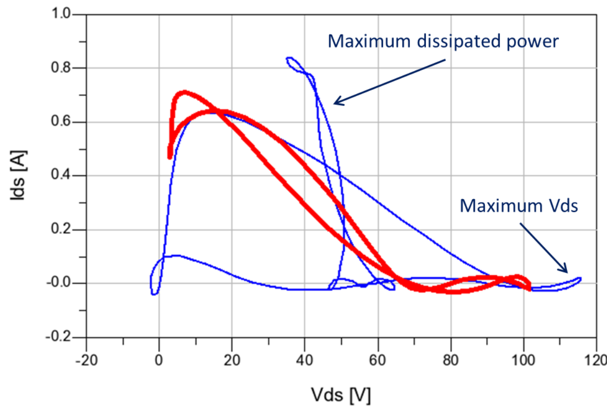

Fig. 2. Example of power-bar unit-cell load-line trajectories for external mismatch at VSWR 10 (thick red line is nominal 50 Ω load condition).

One of the characteristics of GaN technology is the high voltage breakdown level. This level is often much higher than two times the nominal bias voltage. Therefore the high voltage peaks caused by load mismatch are less of a problem than the high power dissipation that can occur. For this reason a protection circuit was designed that would first of all reduce the power dissipation in the transistors when mismatch occurs. But at the same time this circuit also reduces the high voltage peaks. The protection circuit and the architecture of the designed solid-state power amplifier is shown in fig. 3.

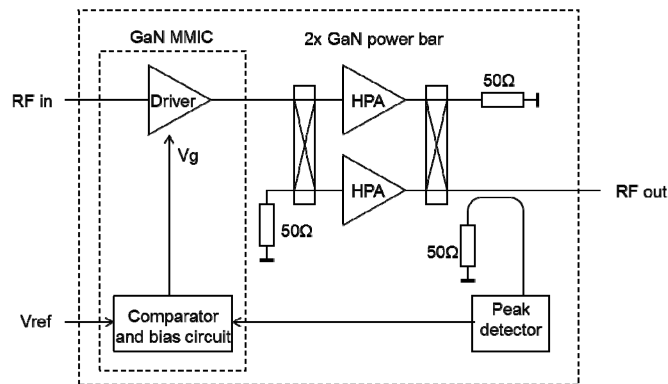

Fig. 3. Solid-state power amplifier module and protection architecture.

The solid-state power amplifier consists of an output-stage with two parallel GaN power-bars working with 90° phase difference and a GaN driver-stage. The 90° phase difference is implemented by two Lange Couplers. This configuration is not necessary for the protection mechanism, but does offer some extra balancing (reduced load-pulling) with respect to the worst case phase of the reflection coefficient. The protection works by sensing the reflected power, via a directional coupler and diode power detector. This signal is fed back to a comparator circuit that compares this level to an external defined reference level. As soon as the detected power level increases above a threshold, the gate voltage of the driver-stage is lowered, thus causing the driver to be pinched off and deliver less power to the output-stage. The protection level can be adjusted by changing the external reference voltage. The comparator also includes a gate-bias circuit to compensate for threshold voltage variations. The GaN driver-stage, comparator and gate-bias circuit are implemented on a single GaN MMIC.

III. POWER AMPLIFIER DESIGN AND REALIZATION

The solid-state power amplifier has been divided in two parts: a module with the two parallel power-bars and reflected power detector and a second smaller module with the driver-stage. In a future design and given the right GaN power-bar technology that also includes integrated passive components this power amplifier module could be implemented on a single MMIC. Two different power amplifiers have been designed: a version that uses the 0.25 µm and 0.5 µm AlGaN/GaN technology from FBH, for respectively the driver- and power-bar stage and a version that uses the 0.25 µm and 0.5 µm AlGaN/GaN technology from UMS, for respectively the driver- and power-bar stage. Both amplifier modules have used the following design approach:

The design of the power-bar module has started with load-pull measurements on unit cell transistors of the power-bar. Each power-bar consists of a number of these unit cells in parallel. For example, the used power-bar of UMS uses 6 transistors of 8x250 µm size in parallel. These load-pull measurements have been compared with load-pull simulations using the large signal transistor model. From this comparison a compromise load between maximum output power and maximum efficiency has been chosen. Output-matching networks have been designed to match this optimum load to 50 Ω. Next the input matching, including stability measures, has been designed. Two Lange Couplers have been used to combine the two power-bars. A directional coupler with diode detector has been added to sense the reflected power. A low-pass network has been included to ensure the stability of the feedback loop. This module is implemented on Rogers 6010.2 substrate with copper backing. The power-bars are directly mounted on this copper backing. Fig. 4 shows a photographs of the realized module.

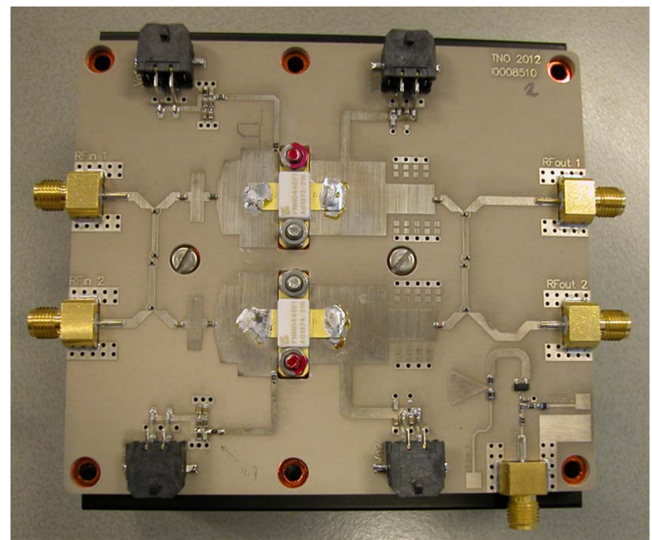

Fig. 4. Photograph of the power-bar module with FBH power-bars.

The driver module consists of a GaN MMIC and matching and biasing networks. The MMIC contains the driver transistor and the comparator with gate-bias circuit. Large signal models of the transistors and the process design kit have been used. No output-matching is included on the MMIC and only some pre-matching at the input. The schematic of the MMIC and the two MMIC photographs are shown in the following two figures.

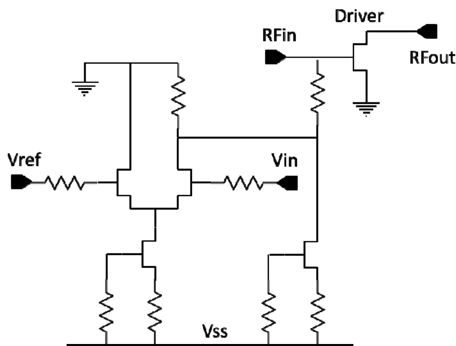

Fig. 5. Scematic of the driver MMIC.

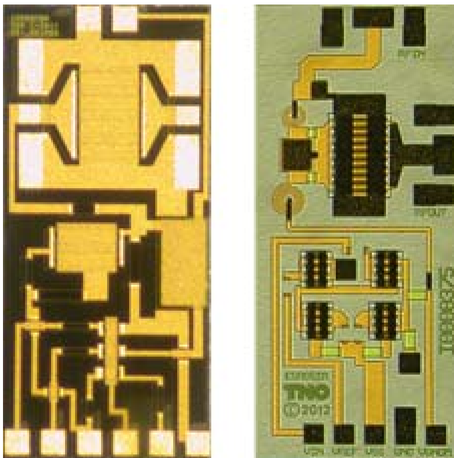

Fig. 6. GaN driver MMIC in FBH (left) and UMS (right) technology.

After wafer-processing, the functionality has been verified by on-wafer measurements. Also load-pull measurements have been performed to determine the optimum load impedance of the driver transistors. An output and input matching network has been designed on Roger 4003 substrate. This substrate is also mounted on a copper back plate, on which the driver MMIC is directly mounted. This module is shown in fig. 7.

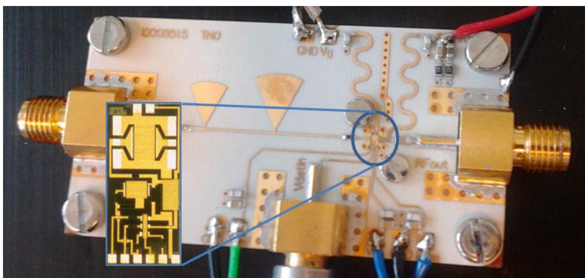

Fig. 7. Photograph of the driver module using the MMIC in FBH GaN technology.

IV. Measurement Results

For all large signal measurements a pulsed DC and RF signal is used with 60 µs pulse width and 6 kHz pulse repetition frequency (36% duty cycle), to represent real-life operating conditions for a radar application. First measurements have been performed on the driver and power-bar module separately to verify the correct functioning and large signal performance. The driver module delivers 39 dBm output power with 17 dB small signal gain at 1.55 GHz and 28 V drain bias supply in nominal operation. When the input voltage to the comparator, i.e. the signal coming from the reflected power detector, is increased, the gain and output power drop, although when driven far into compression self-biasing occurs and the output power and gain rapidly increase again. The performance of the stand-alone power-bar module has been measured at 40 V drain supply. 51 dBm output power and 16 dB small signal gain has been measured at 54% power added efficiency at 1.55 GHz.

Fig. 8 and 9 show the measured output power and power dissipation of the power amplifier module for several different scenarios. First the combination of driver and power-bar module has been measured without the protection feedback loop (dashed line). This situation gives the maximum output power. In this case, at 40 V drain bias, an output power of 51.2 dBm has been measured. Next the feedback loop is closed and measurements have been done at different reference voltage levels, with 50 Ω load or with a short at the output of the external test set (causing a reflection coefficient of 0.76 or VSWR 7.3). Even with a 50 Ω load the output power is being reduced by the feedback loop due to the limited directivity of the directional coupler (about 30 dB). This unwanted behavior can be reduced by increasing the negative reference voltage of the comparator, which will increase the threshold for activation of the protection mechanism. In fig. 9 the corresponding dissipated power is shown, for the situation with a shorted output. In this measurement the dissipated power has remained below the level that occurs under normal operation, up to a certain source-power level. Above this level the driver circuit starts to self-bias and the protection is no longer effective. Another measurement has been done with a short connected directly at the output of the amplifier module ("Real short"). Also in this case, when all output power is reflected, the dissipation level remains acceptable.

By using a manual double slug tuner the performance has been measured over a wide range of reflection coefficients. Fig. 10 shows the measured output power and related dissipated power at a fixed source-power of 24 dBm versus output reflection coefficient magnitude. The power dissipation remains relatively constant with increasing reflection coefficient while the output power reduces to zero for full reflection. Also indicated is the theoretical $1-|\Gamma|^2$ power reduction in case of load mismatch. The reaction time of the protection mechanism has been measured by activating the pulsed RF signal with a short at the output of the module, and monitoring the reflected power level and resulting gate-bias of the driver-stage. This bias goes from nominal to pinch-off condition in less than 0.5 µs after the reflected power level started to increase.

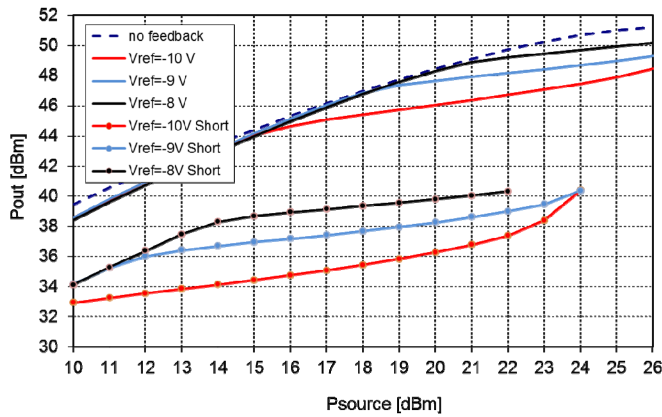

Fig. 8. Measured output power at 40 V drain bias and 1.4 GHz, for nominal operation (50 Ω load), with and without feedback loop, and with a short at the output, for 3 different settings of the comparator reference voltage.

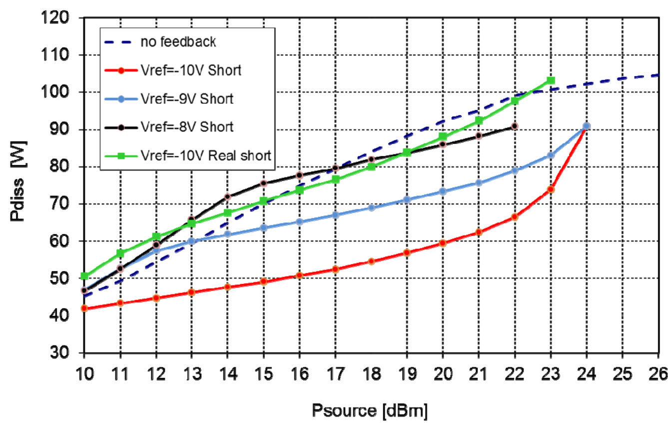

Fig. 9. Measured power dissipation at 40 V drain bias and 1.4 GHz, for nominal operation (50 Ω load) without feedback loop, and with a short at the output, for 3 different settings of the comparator reference voltage.

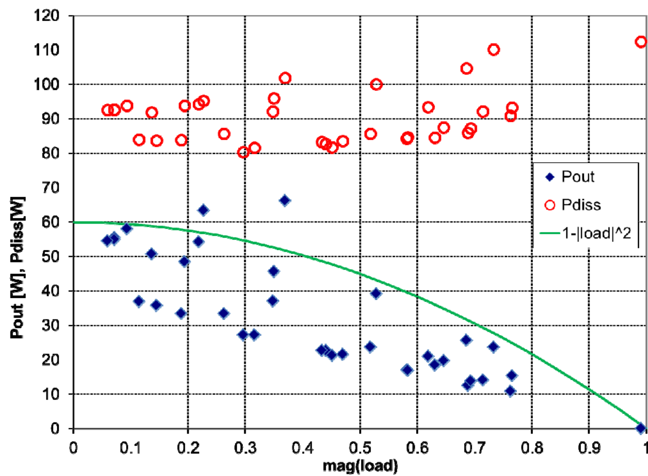

Fig. 10. Measured output power and power dissipation at 40 V drain bias, source-power of 24 dBm and 1.4 GHz, versus output reflection coefficient magnitude and phase.

V. Conclusions

A protection mechanism, based on reflected power detection, has been implemented in a GaN high power amplifier module, consisting of a GaN driver MMIC and GaN power-bar output-stage. A dedicated GaN MMIC has been designed as driver and incorporates the automatic gate-bias circuit.

This mechanism protects the amplifier against all load conditions, up to a short directly at the output of the module, without the use of a ferrite-based isolator. Because of this protection mechanism the dynamic load line of the power transistors does not exceed the nominal load line, both for voltage stress and power dissipation. A fast reaction time of less than 0.5 µs has been measured. An external reference voltage can be used to set the threshold level for activation of the protection.

Limitations of this concept are the limited directivity of the directional coupler, which causes the protection to act already when no reflection is present, and the self-biasing of the driver-stage. Because of this self-biasing, the driver cannot be driven far into compression.

In the current configuration the driver-stage and power-bar stage are two separate building blocks. But since both are realized in GaN technology, a future realization could use a fully integrated design to offer a self-protected GaN power amplifier module capable of withstanding any load condition.

Acknowledgments

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