Advances in maskless and mask-based optical lithography on plastic flexible substrates

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ABSTRACT

Organic flexible electronics is an emerging technology with huge potential growth in the future which is likely to open up a complete new series of potential applications such as flexible OLED-based displays, urban commercial signage, and flexible electronic paper. The transistor is the fundamental building block of all these applications. A key challenge in patterning transistors on flexible plastic substrates stems from the in-plane nonlinear deformations as a consequence of foil expansion/shrinkage, moisture uptake, baking etc. during various processing steps.

Optical maskless lithography is one of the potential candidates for compensating for these foil distortions by in-situ adjustment prior to exposure of the new layer image with respect to the already patterned layers. Maskless lithography also brings the added value of reducing the cost-of-ownership related to traditional mask-based tools by eliminating the need for expensive masks. For the purpose of this paper, single-layer maskless exposures at 355 nm were performed on gold-coated poly(ethylenenaphthalate) (PEN) flexible substrates temporarily attached to rigid carriers to ensure dimensional stability during processing. Two positive photoresists were employed for this study and the results on plastic foils were benchmarked against maskless as well as mask-based (ASML PAS 5500/100D stepper) exposures on silicon wafers.

Keywords: optical maskless lithography, spatial light modulator, pixel grid imaging, plastic electronics, flexible substrate

1. INTRODUCTION

Electronics are ubiquitous in everyday life, and they all require a common building block – the transistor. For the past few decades the advances in silicon-based electronics have driven the size of transistors into the nanometer regime, mainly due to processor and memory-related applications, with current state-of-the-art devices aiming at the 32 nm lithographic node. The relatively new field of flexible electronics faces new challenges, arriving not necessarily from the small dimensions of the transistors, but from the deformations and instability of the substrate [1,2,3].

Flexible electronics or products which incorporate flexible electronic devices have already found use in displays, OLED lighting and signage, RFIDs, and photovoltaics[4,5]. A key advantage of these products, besides functionality, flexibility, and light-weight is the low-cost. While some of the flexible electronics will be sold in niche markets, many of them will have to compete with mature technologies, already established for decades. To be able to compete, besides aspects related to performance, lifetime or environmental impact, flexible electronics need to have low manufacturing costs. Common perception in the field of flexible and plastic electronics is that low cost is associated with the ability of manufacturing devices on large area substrates with high throughput, possibly in roll-to-roll (R2R) or sheet-to-sheet manner[4,5]. Low-cost patterning techniques such as printing[3] are making their way into the flexible electronics market; however, applications in high-end products such as displays are limited due to relatively large dimensions of the printable structures and lower conductivity of metallic patterns. Photolithography adapted for the specific challenges of plastic electronics, and with lower production costs is an obvious choice. Versatility is a strong attribute of

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photolithography, as this technology has been employed in manufacturing MEMS, optoelectronics, processors and memories, as well as the backplanes in LCD and plasma TV displays. While optical lithography in the most advanced Si fabs is performed on 300 mm and soon on 450 mm Si wafers, the display industry uses for the new generations LCD displays substrates that are 2.2 x 2.5 m^2 (generation 8.5) or even larger. For flexible OLED-based displays, similar or smaller substrates should be employed, and manufacturing costs should be similar if they are to compete with main stream LCDs. Development of optical lithography on flexible substrates has already been studied by researchers in industry and academia alike, and the first organic flexible electronic displays are already available[4,6].

Common substrates for flexible electronics are metal foils, paper, and plastic, particularly poly(ethyleneterephthalate) (PET) and poly(ethylenenaphthalate) (PEN) [4]. PEN and PET have been widely employed for manufacturing flexible electronics, and these substrates are prone to non-linear deformations induced by heat, moisture, and mechanical stress[7,8]. Previous research has shown that mask-based lithography may be successfully employed for manufacturing transistors on plastic foils temporarily laminated on top of a rigid carrier[1]. While for small-size substrates on rigid carrier it is possible to cope with deformations, for large area free standing substrates or in roll-to-roll lines the deformations could be significant and difficult to cope with. The challenge is to align the second pattern with respect to the first one, for example source (S) and drain (D) electrodes with respect to the gate (G) (Figure 1).

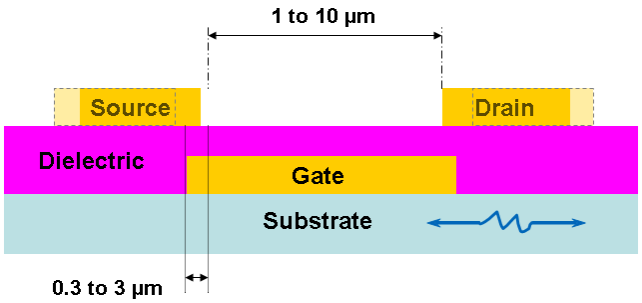


Figure 1: Representation of a metal-insulator-metal stack with bottom-gate architecture, and potential displacements (dotted lines) of S/D caused by non-linear deformations of the plastic substrate.

Linear deformations of the substrate would be relatively easy to account for in mask-based lithography by simply changing the magnification of the projected image, or the projected pattern. However, on plastic substrates shrinkage and expansion of the substrate could occur at the same time and on the same foil depending on the monitored direction, a result of foil anisotropy[7]. It is thus difficult to cope with these deformations on the fly, and a good solution would be projection of the corrected image without a mask. Maskless lithography has been around for a while[9] in two main embodiments, electron-beam-[10] and optical-based[11].

UV-based maskless lithography is a suitable candidate for manufacturing the back-plane of flexible displays, since it does not require the use of a rigid mask, and the projected image is formed by a multitude of laser beamlets, turned on and off by a computer assisted micromirror array[11,12]. The "mask" is a digital image file, which may be altered by the operator of the tool so that it compensates for the deformations introduced by processing steps (i.e. resist deposition, baking, handling, development, and etching). While flexibility is one of the appealing features of maskless lithography, cost reduction is another one, since expensive masks are not needed anymore in such a technology. One of the key applications of maskless lithography has been in prototyping, where frequent changes of designs and patterns are encountered.

While the exposure and the behavior of resists in mask-based optical lithography are well known, there are not many studies on performance of resists exposed with optical maskless tools. We performed a thorough analysis of two i-line (DNQ-based) resists candidates for maskless optical lithography at 355 nm pulsed radiation, and compared the results with i-line mask based exposure in a stepper. We selected three substrates for the current study: a 6" Si wafer, Au coated on Si wafer, and Au coated on top of a PEN foil which was temporarily attached on top a Si wafer to confer it stability during processing. We thus introduce a relatively new topic into the lithography field that is, UV maskless exposure on plastic flexible substrates. To help the reader relate to classic optical lithography, we chose to study the behavior of the resists on Si wafers as well.

2. MASKLESS IMAGING CONCEPT

2.1 Image formation

The maskless imaging tool contains a laser module operating at 355 nm wavelength that is coupled into an optical column. This component contains a spatial light modulator device which modulates the incident light such that an aerial image is formed on the wafer surface.

The imaging process starts with a gray scale bitmap input file with a pixel grid of 0.75 μm, thus enabling a minimum feature size of about 3 microns. The bitmap can contain 64 gray values which translate into variations of the exposure dose.

The use of gray levels in the bitmap affects the line edges of the patterns on the substrate. Gray levels can make smoother lines, especially in the case of diagonals but the contrast of the aerial image is then decreased. Printing with high contrast bitmaps is denoted by "on-grid" imaging. For other experiments, the gray levels will be used to influence sidewall angles (see section 4.1).

After defining the bitmap, the sequence of spot writing is determined. In the first step, the intensity values of the spots are calculated by taking into account the gray value pattern of the bitmap and the position of the spots with respect to the movement of the stage. In the second step the voltage set points of the mirrors of the spatial light modulator are calculated, based on the calibration data in which the voltage versus the light intensity is measured.

2.2 Exposure

After data processing and synchronization of the laser pulses, the scan movement of the stage and the image formation take place, and the substrates can be exposed. Vacuum is used to hold the substrate during the exposure sessions. In Figure 2 the principle of the pixel-grid-imaging writing process is illustrated for 4 consecutive moments of writing a gray scale image. The substrate moves while the spots are stationary. The spots are switched on and off to generate the patterns. The pattern is written by moving the stage relative to the optical columns.

If the dose delivered to the resist in one exposure step is not enough, it is possible to expose the substrate several times in order to get the necessary incident dose to the resist. The accuracy of the stage is high enough to expose the same layer multiple times at precisely the same position.

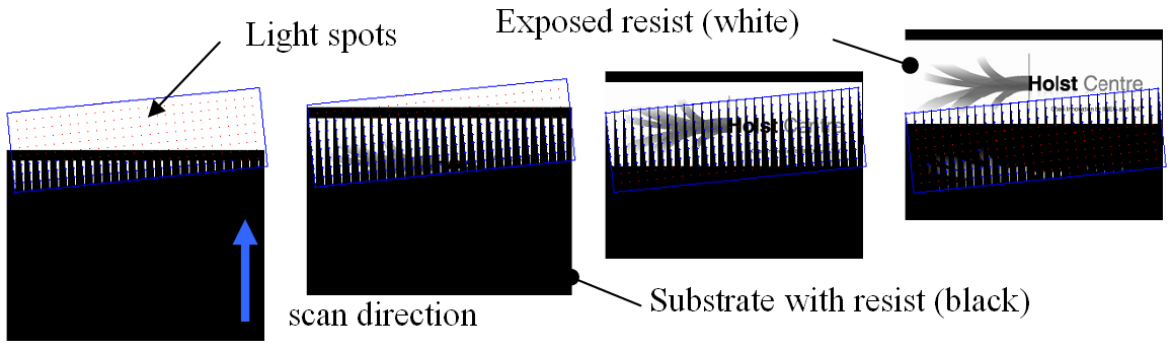


Figure 2: Artistic representation of the concept of pixel grid imaging illustrating four moments in the pattern writing process. The left image contains a substrate covered with unexposed resist (depicted in black). Further to the right, the final image is shown after the substrate will have been illuminated by the spots.

3. EXPERIMENTAL DETAILS

Two DNQ-based positive photoresists, a faster photospeed resist A and a lower photospeed resist B, were used in the experimental study. Both resists were deposited by spin coating followed by soft bake at 90°C for 60s. A commercial software package was used to calculate the dose-to-clear swing curves for both resists. Based on these simulations, the spin coating speed was optimized in order to achieve a soft bake film thickness which would ensure a point of minimum clearing dose on the swing curve: 3000 RPM for resist A gave a thickness of 1.14 μm whereas 2750 rpm lead to 0.82 μm for resist B.

Three different substrates were used in the present study: 6-inch silicon wafers, gold (Au)-coated Si wafers, and Au-coated 25 μm thick PEN foils laminated on top of 6" Si wafers, referred to as foil-on-carrier (FOC) samples. To promote adhesion, the surface of the Si wafers was exposed to HMDS-vapor priming prior to photoresist deposition. The Au layer was obtained by sputter deposition and its thickness was kept constant at 30 nm throughout the entire study. In order to increase the adhesion of Au to the silicon substrate, a 5 nm titanium adhesion layer was deposited prior to Au sputtering[2]. The handling of the 25-μm PEN foils poses serious challenges due to its thinness and electrostatic behavior. In order to facilitate the handling and make use of existing processing infrastructure, the PEN sheets were temporarily glued to rigid carriers by an in-house developed method[1,2]. The adhesive material is spin cast at high spin speed onto 6-inch Si wafer to obtain a layer of approximately 20 μm in thickness followed by the lamination of the plastic foil onto the glue-coated wafer. This method has several advantages: (i) ensures excellent mechanical and dimensional stability of the plastic foil during all processing steps, (ii) damage-free removal at the end of the process of the fully-patterned PEN substrate, (iii) flatness of the FOC better than 1 μm [1] which meets the requirements for exposure on the PAS 5500/100D stepper. The PEN foil is characterized by an intrinsic surface roughness which could have a negative impact on the quality of resist profiles by increased light scattering. In order to overcome this issue, a planarization layer was spin coated on top of the plastic substrate. This approach also eliminates the necessity of using Ti as gold adhesion enhancer. The 30-nm thick Au layer is thus directly sputtered on top of the planarization layer.

The exposures were performed with the mask-less optical lithography tool and an i-line (365 nm) ASML PAS 5500/100D, a step-and-repeat system with a 0.48 NA projection lens. The exposure dose was 50 mJ/cm^2 and 80 mJ/cm^2 for resist A and resist B, respectively. Subsequently, the resist A- and resist B-exposed samples were subjected to the post-exposure baking (PEB) step for 90s at 110°C and 60s at 110°C, respectively. A distinct commercially available developer was utilized for each photoresist as recommended by the photoresist manufacturers. The immersion development times were set at 70s for resist A and and 60s for resist B.

4. EXPERIMENTAL RESULTS AND DISCUSSION

4.1 Versatile pattern generation

As pointed out before, the main advantage of using the maskless lithography tool is given by its flexibility for writing patterns of various geometries in less time and with fewer costs than those involved in the manufacturing of new expensive masks. Some examples of the many possible patterns that can be easily generated by the maskless tool in only one exposure session are given in Figure 3. The scan direction was in all instances from top to bottom of the pictures. Right image shows a pattern of source and drain electrodes that could be used as the building block of a field-effect transistor to be incorporated in future flexible electronic devices. It is characterized by lines and spaces of nominal CD equal to 9.75 μm. The Holst Centre logo displayed in the centre of Figure 3 (left) highlights the imaging versatility of the tool which can expose any arbitrary user-generated pattern. Notice in both images the excellent capability of the tool in writing letters with very good contrast and contour lines which is achieved by synchronizing the on-/off-switching of contrast device micromirrors, laser pulsing and stage movement.

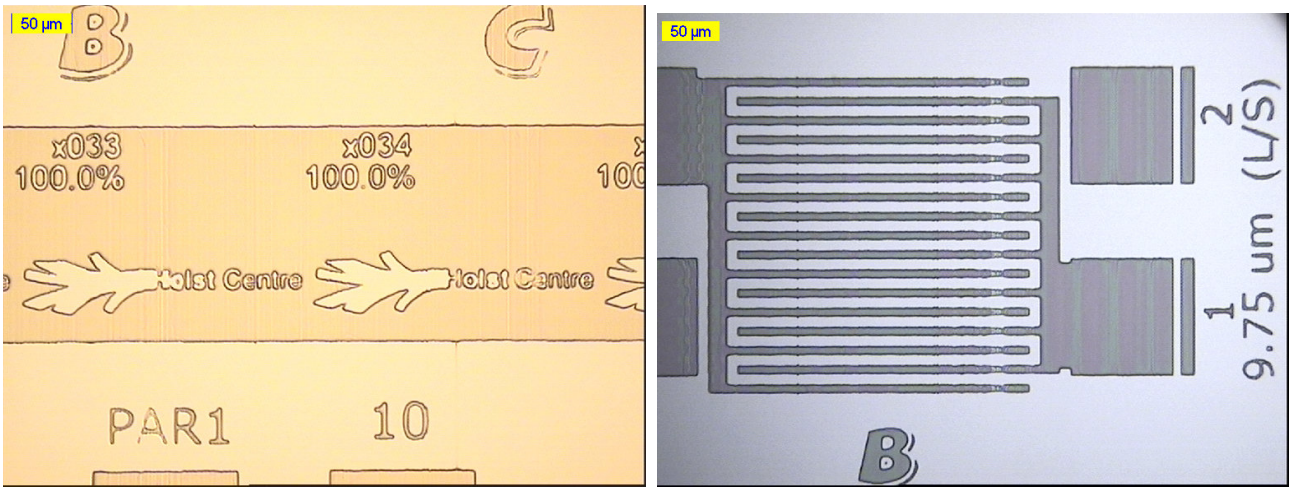


Figure 3: optical micrographs of two of the various patterns written with the maskless tool in only one exposure session. The logo of Holst Centre is depicted in the centre of the left image while the right picture displays "finger-like" source and drain electrodes.

In paragraph 2.2 the pixel grid imaging concept and the possibility of using various intensity levels (gray scales) by means of the micromirror tilting were described. An interesting application which arises by combining these two capabilities is the possibility of tuning the sidewall angle of resist lines. When the edges of the exposed features are aligned on the bitmap design grid on speaks about "on-grid" patterning; "off-grid" occurs when the pattern edges are slightly displaced with respect to the design grid. Then levels of grey scale are used to define the line edges. Two examples showing the influence of on- and off-grid imaging on the sidewall angles of resist A are depicted in Figure 4. The on-grid written resist line in the left picture shows steeper sidewalls than that of the off-grid counterpart. Estimates of the sidewall angle based on the top-view SEM images in Figure 4 suggest values of approximately 67^{O} and 45^{O} for the on-grid and off-grid patterns, respectively. The clearly defined tip of the resist line in Figure 4 (left) was simply obtained by the maskless lithography tool and is not due to any mechanical sectioning of the feature. Future improvements of this sidewall adjustment technique will be determined by the specific requirements of the targeted application of optical maskless imaging.

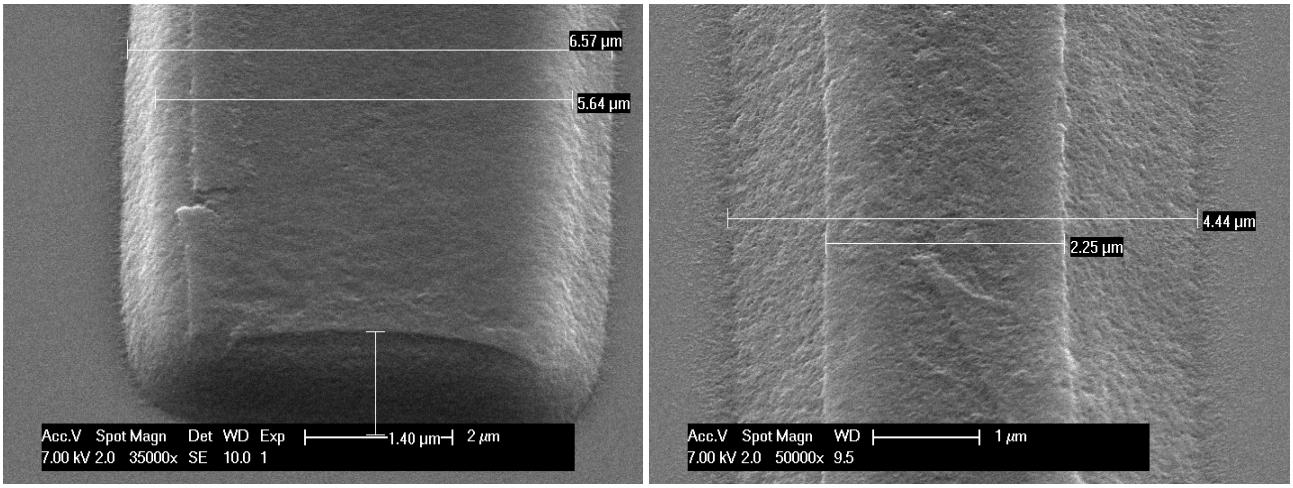


Figure 4: SEM micrographs of two resist A lines patterned with different approaches. Left picture shows a line written with on-grid imaging whereas off-grid imaging is depicted in the right picture. Notice the steeper sidewall obtained with on-grid imaging.

4.2 Resist profile analysis

One of the conventional approaches to characterize the resist profiles is to perform scanning electron microscopy (SEM) on cross sections through the resist features. Obtaining cross sections with a clear cut through the resist on silicon and on silicon + gold wafers proves to be an easy procedure thanks to the native cleaving directions of the silicon lattice. However, performing the same procedure on a thin polymeric foil as used in present study (25 μm PEN foils) proves to be extremely cumbersome. Taking this into account, atomic force microscopy (AFM) was employed to acquire the three-dimensional (3D) profiles of the resist lines for all samples investigated in this work. This also has the advantage of leaving the samples practically unaltered, as opposed to the SEM approach. In this case a few nanometer thick Au or platinum layer should have been deposited on the samples in order to ensure a conductive top surface. After AFM analysis the samples can be sent to further processing such as the wet etching of gold patterns.

The results are summarized for resist A and resist B in Table 1 and Table 2, respectively as a function of substrate (Silicon, silicon + gold, PEN foil + planarization layer + gold) and exposure technique (PAS 5500/100D stepper or the optical mask-less lithography tool). We targeted two different critical dimensions (CD) with the maskless tool, 9.75 μm and a lower value of 5.25 μm. They were benchmarked against 10 μm and 4 μm lines written with the step-and-repeat projection lithography tool. The non-integer values of the targeted CD's in case of the maskless device are caused by the pixel writing grid which constrains the feature sizes to be multiples of 0.75 μm needed for the high contrast bitmaps.

Below each AFM picture, the line width value measured at full width at half maximum is indicated. The variation in CD is very small in the case of stepper exposures, being less than 1%. Therefore, only the average value is given for the PAS 5500 data. On the other hand, the not yet optimized exposure conditions of the maskless lithographic tool caused more significant linewidth variation across the three AFM-probed resist lines. In order to give a quantitative indication of this CD non-uniformity, the minimum and the maximum value within the three imaged lines is reported below the AFM profile picture. The variation ranges from 0.21 μm (Table 2, 5.25 μm CD, Si + Au / FOC + Au substrates) up to 1.88 μm (Table 1, 9.75 μm CD, FOC + Au substrate). The main reason for this significant CD non-uniformity lies in the inhomogeneous substrate illumination through the MLA component. However, on the maskless tool one could possibly easily compensate for this non-uniformity by applying optical proximity corrections in the bitmap files, more convenient than correcting the masks. Inhomogeneous illumination may be caused by contaminated MLA (resist outgassing can occur during exposure followed by deposition on the micro-lenses), non-uniform electronic driving of the spatial light modulator (SLM) micro-mirrors, and spatial or temporal fluctuations in the laser power incident onto the SLM device. For these reasons, it was calculated that there is an approximately 20% inaccuracy in determining the exact dose deposited in the resist with the maskless tool. Thus even if a total dose of 50 mJ/cm^2 and 80 mJ/cm^2 was targeted for resist A and B respectively, it is likely that a slightly higher energy dose was projected on the samples.

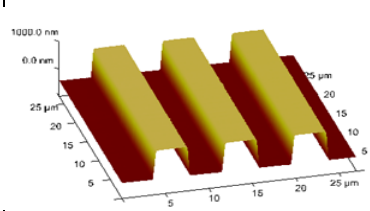
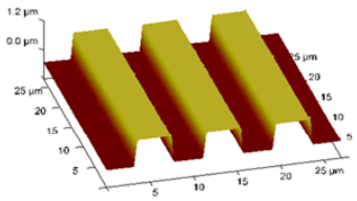
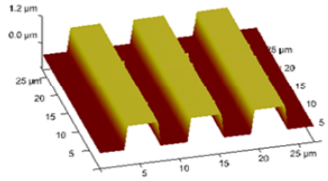
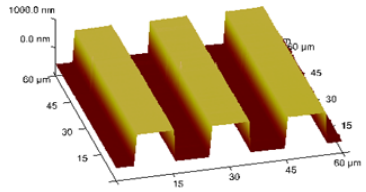
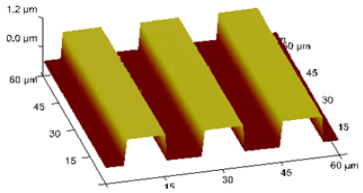
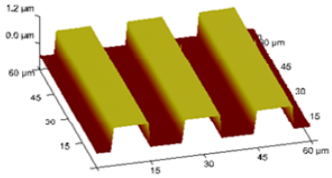
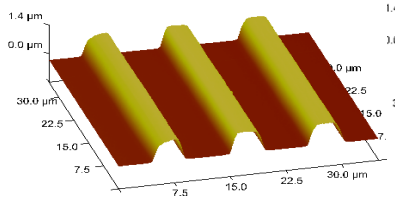
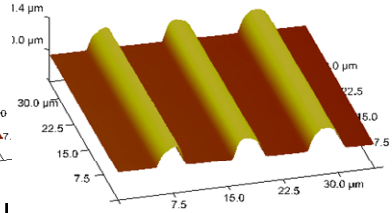
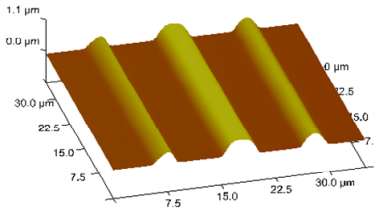
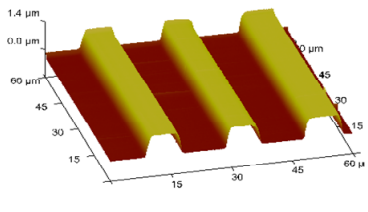
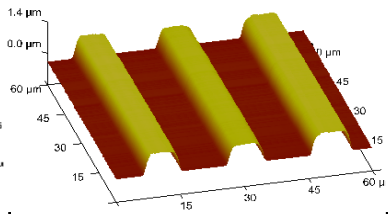
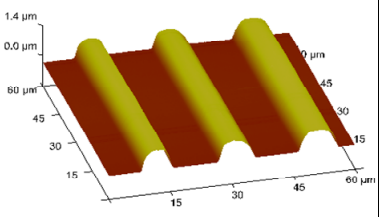
Expo-sure	CD	Si	Si + Au	FOC + Au
PAS 5500/100D	4 µm	 3.97 µm	 4.27 µm	 4.15 µm
	10 µm	 10.00 µm	 10.47 µm	 10.35 µm
maskless	5.25 µm	 3.62 - 4.17 µm	 3.01 - 3.97 µm	 2.26 - 3.97 µm
	9.75 µm	 7.73 - 8.79 µm	 7.85 - 8.79 µm	 6.33 - 8.20 µm

Table 1: AFM 3D resist profiles for resist A summarized by substrate type and exposure method. For each combination of exposure technique and substrate two critical dimensions were targeted in order to assess the imaging performance within two size ranges of the optical maskless tool versus the conventional stepper exposure: 9.75 µm and 5.25 µm for maskless and 10 µm / 4 µm for mask-based. The measured line widths are mentioned below the images with two small differences. In the case of mask-based lithography (PAS 5500/100D exposures), the CD variation is on the order of tens of nanometers being more a consequence of the measurement inaccuracy of the AFM tool, so only the average of the three line measurements is reported. The not yet optimized exposure conditions of the maskless tool caused more significant linewidth variation. We report the minimum and the maximum value out of the three measured lines.

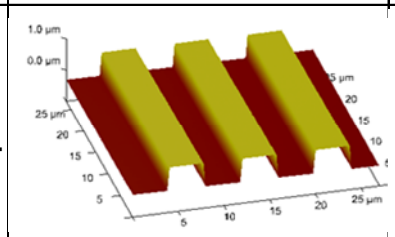
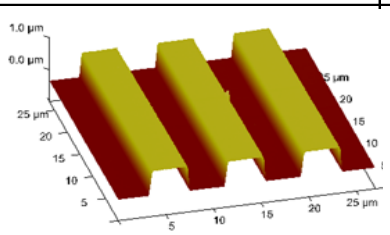
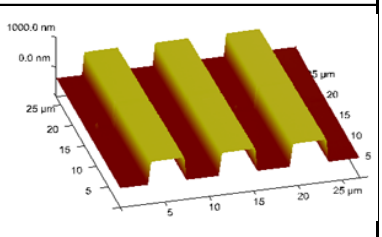
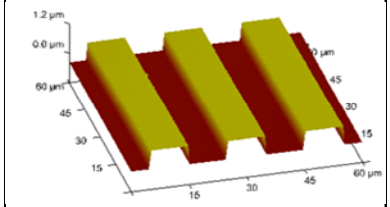
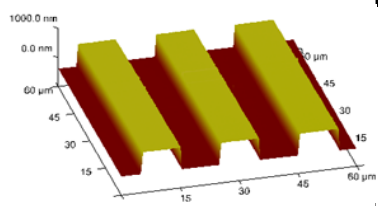
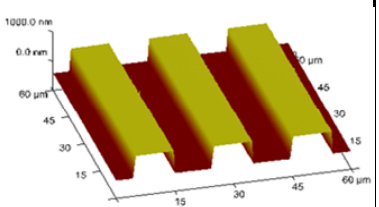
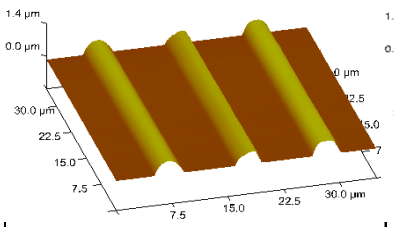
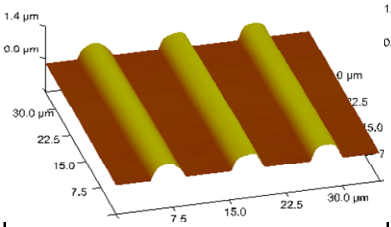
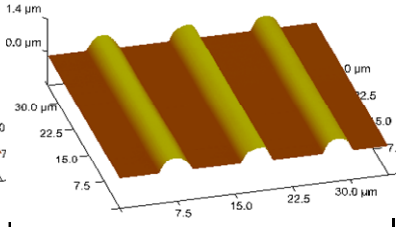
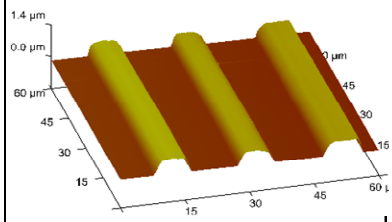
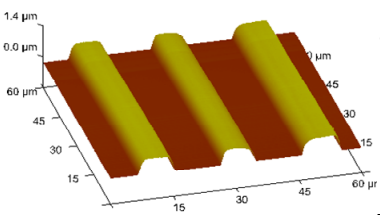
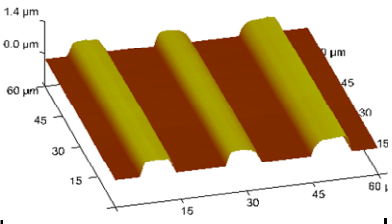
Expo-sure	CD	Si	Si + Au	FOC + Au
PAS 5500/100D	4 µm	 3.92 µm	 3.97 µm	 4.06 µm
	10 µm	 10.04 µm	 10.00 µm	 10.16 µm
maskless	5.25 µm	 2.80 - 3.08 µm	 3.49 - 3.69 µm	 3.15 - 3.35 µm
	9.75 µm	 7.15 - 8.32 µm	 7.38 - 8.32 µm	 7.15 - 8.44 µm

Table 2: AFM 3D resist profiles for resist B summarized by substrate type and exposure method. For each combination of exposure technique and substrate two critical dimensions were targeted in order to assess the imaging performance within two size ranges of the optical maskless tool versus the conventional stepper exposure: 9.75 µm and 5.25 µm for maskless and 10 µm / 4 µm for mask-based. The measured line widths are mentioned below the images with two small differences. In the case of mask-based lithography (PAS 5500/100D exposures), the CD variation is on the order of tens of nanometers being more a consequence of the measurement inaccuracy of the AFM tool, so only the average of the three line measurements is reported. The not yet optimized exposure conditions of the maskless tool caused more significant linewidth variation. We report the minimum and the maximum value out of the three measured lines.

Another topological difference between the mask-based and the mask-less written resist features consists in the shape of the top part of the resist line. As shown in the comparative display in Table 1 and Table 2 the top part of the lines printed by the optical maskless tool exhibits a rounded profile as opposed to the flat top surface attained by mask-based lithography. This is highlighted in Figure 5 where four cross sections through the 3D AFM profiles are given for resist A and B coated on the FOC+Au layer stack for both the PAS 5500/100D and the maskless exposures.

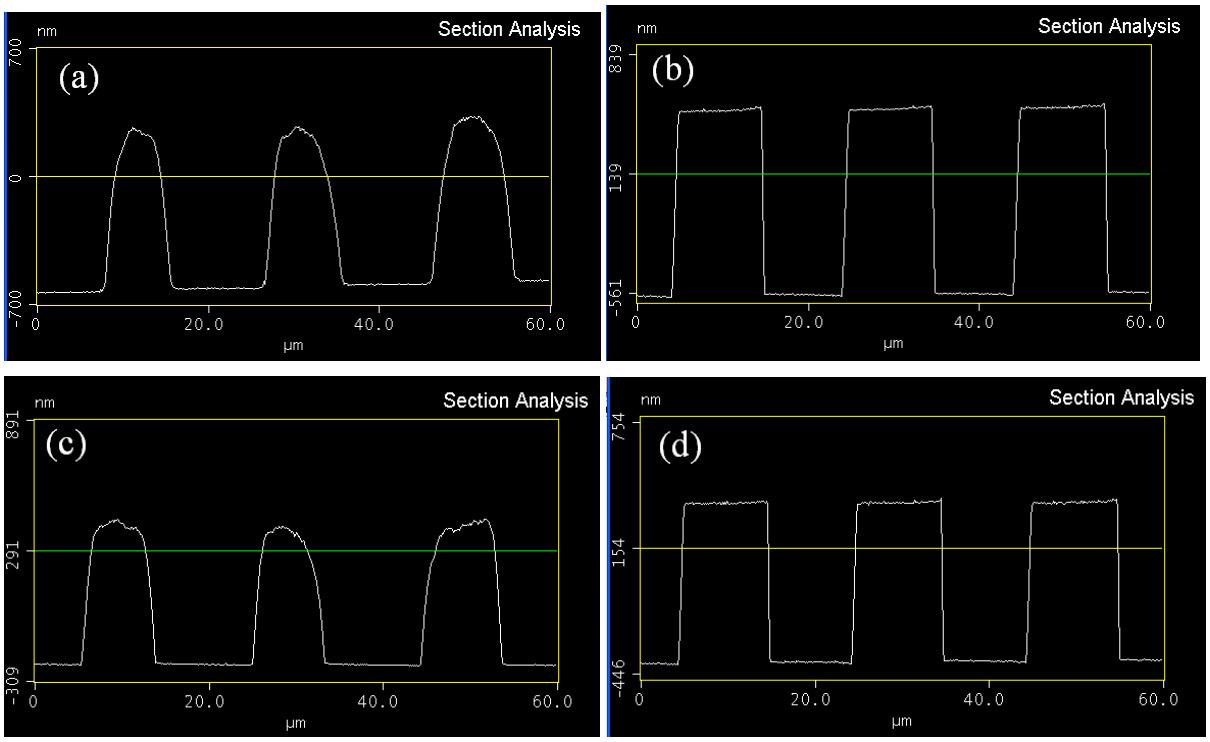


Figure 5: cross sections through the 3D AFM resist profiles in Table 1 and Table 2 for the two resists coated on the FOC+Au layer stack: resist A exposed with the maskless tool CD 9.75 µm (figure (a)) and with the stepper CD 10 µm (figure (b)), and resist B exposed with the maskless tool CD 9.75 µm (figure (a)) and with the stepper CD 10 µm (figure (d)).

The difference between the flat and round-shaped profiles stems from the inner properties of the light projection mechanism employed in the two investigated exposure tools. The PAS 5500/100D stepper allows for a high image contrast between exposed and unexposed areas on the sample. Hence the steepness of the sidewalls approaches 90^{o} and the flatness of the top surface. On the other hand, the maskless system which is still a prototype tool does not yet provide the desired light contrast due to significant levels of stray light which cause dark exposure of the not-to-be-patterned areas of the positive resist. This tool artifact also explains the resist loss of the maskless exposed patterns which amounts to 16%-19% of the film thickness of mask-based samples.

4.3 Organic field effect transistor obtained by maskless lithography

A functional field effect transistor (FET) with a non-patterned gate was manufactured by defining the source/drain electrodes by means of the optical maskless tool. An n^{++}-doped silicon wafer acted as the gate and a 224 nm thick dielectric layer of SiO_2 was thermally grown on top of it. A layer of Au 30 nm in thickness was then sputtered using a thin layer of Ti as an adhesion enhancer of the gold to the SiO_2. The source/drain electrodes were patterned into the resist by maskless lithography and subsequently wet etched into the Au layer (see Figure 6).

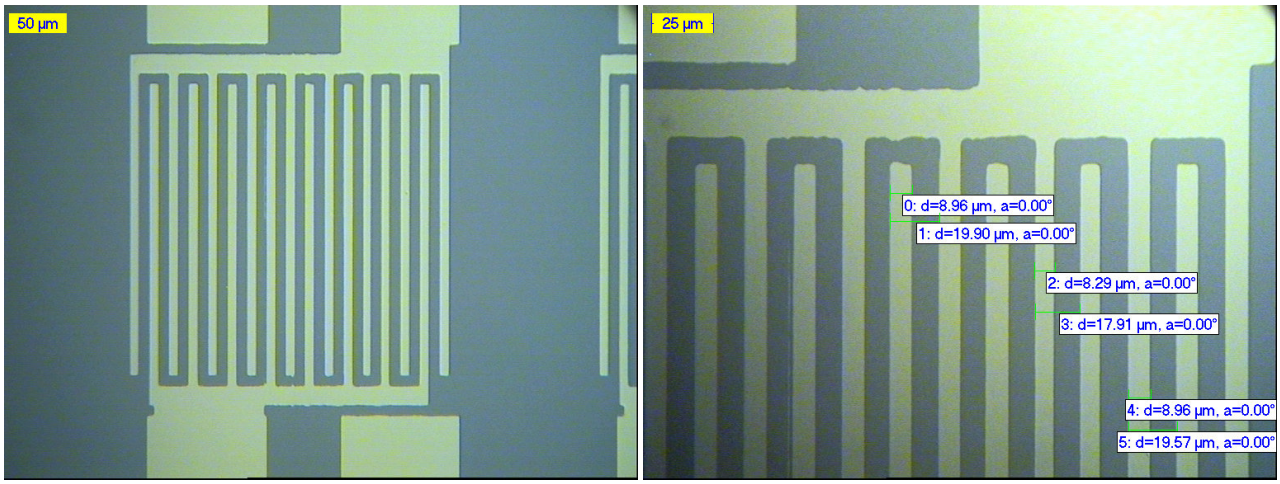


Figure 6: optical micrographs of the S/D electrodes patterned by the maskless lithographic tool and wet etched into the gold layer. Left image provides a zoom-in on the electrodes with typical line widths.

Pentacene was used as the organic semiconductor (OSC) and was deposited drop wise on top of the electrodes. The transistor transfer characteristics are shown in Figure 7 with performance variations due to the large number of investigated devices. Prior to pentacene deposition, the surface was covered with a self-assembled monolayer which improves the morphology of the organic semiconductor grown on metal. Transistor performance may improve as another OSC deposition method is chosen (e.g. evaporation).

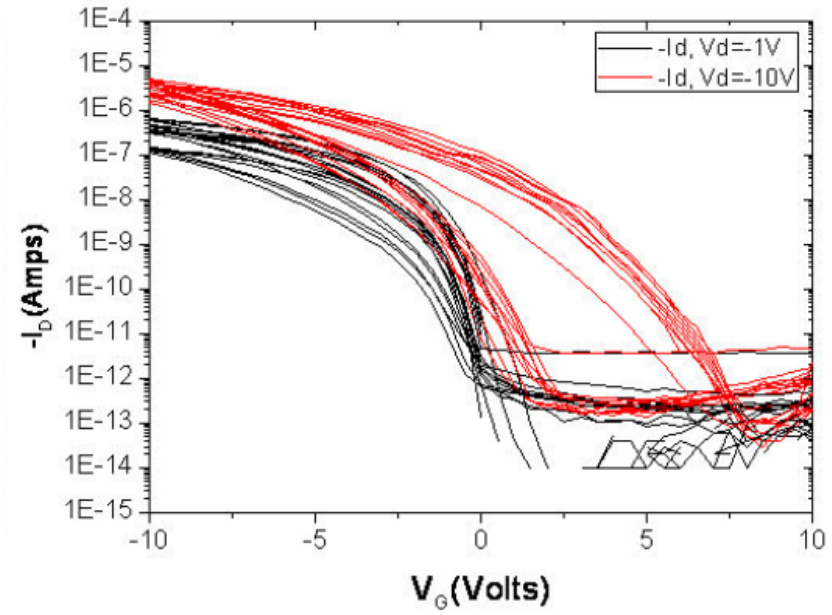


Figure 7: transfer characteristic of an FET with non-patterned gate (n++-dopes silicon wafer) and S/D electrodes patterned with the optical maskless tool.

5. CONCLUSIONS

Results on positive photoresist exposures on plastic flexible substrates by means of optical maskless lithography were presented in this paper. The presented results blend the new promising technology of organic flexible electronics with the imaging flexibility brought by using a maskless optical exposure tool.

In order to benchmark the capabilities of this emerging optical lithographic approach, exposure tests were also performed with an industry established mask-based step-and-repeat exposure tool, an ASML PAS 5500/100D stepper. Exposures were performed on gold-coated 25 μm thick PEN substrates temporarily laminated to rigid carriers and on 6" Si wafers. Lines and spaces were evaluated at two different critical dimensions to assess the performance of the maskless tool in a broader size range. Maskless tool-related imperfections in the exposed resist images particularly refer to CD non-uniformity and rounded-shaped top profiles. They are not characteristic of the general concept of optical maskless lithography and can be mitigated by further improvements in the tool's hardware and software capabilities.

Preliminary results on organic FET transistors with non-patterned gate and S/D electrodes written by maskless lithography were shown. Strategies to improve the transistor performance (e.g. by using different semiconductor deposition methods) are now being investigated.

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