Broadband S-band Class E HPA

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***Abstract*— A broadband class E High Power Amplifier (HPA) is presented. This HPA is designed to operate at S-band (2.75 to 3.75 GHz). A power added efficiency of 50% is obtained for the two stage amplifier with an output power of 35.5 dBm on a chip area of 5.25 x 2.8 mm^2.**

I. Introduction

In a radar T/R module the cost, size, output power and efficiency of the High Power Amplifier (HPA) play an important role. To improve the efficiency a class E design can be employed. This is at the expense of reduced output power or increased size. In recent years a large number of papers has been published on this subject. Most papers however show mostly one stage designs and designs for a bandwidth not sufficient for Radar applications. According to the article by Sokal [1] it should be possible to obtain wider bandwidth than is published for most Class E amplifiers. The idea behind class E operation is to avoid simultaneous voltage over the transistor and current through the transistor since the product of voltage and current gives dissipation. In class E this is obtained by the load applied which assures that the voltage over the transistor is returned to zero before the transistor starts to conduct. To improve the gain of the HPA a two stage design is made with the first stage operated in class AB. To enable a compact design the amplifier is made as an MMIC without requiring off-chip components. The remainder of this article is divided into three sections. The first section describes the design of the HPA, the second section shows the measurement results and in the last section some conclusions are drawn.

II. Design

The design has been realized in the 0.5 µm GaAs pHEMT process, PP50-11, of WIN Semiconductors. The design of the output stage starts with the maximum voltage, output capacitance and maximum current of the transistors in the output stage. This determines the maximum operating frequency for class E operation [2]:

$$f_{MAX} \approx \frac{I_{MAX}}{56.5 C_{out} V_{DS}} \qquad (1)$$

For the WIN PP50-11 process the maximum current is 0.4 A/mm and the output capacitance is 0.34 pF/mm. The drain voltage is selected to be 7 V since the peak drain voltage is [1]:

$$V_{Dpeak} = 3.562 \cdot V_{DS} - 2.52 \cdot V_{DSAT} \qquad (2)$$

The drain bias voltage (V_{DS}) of 7 volt will give 22 V peak drain voltage (V_{Dpeak}) with a saturation voltage (V_{DSAT}) of 1 V. This yields a maximum frequency of 3.5 GHz. By compensating the output capacitance with an inductor the operating frequency can be increased somewhat to the desired maximum frequency of 3.75 GHz.

By using the equations in [3] the component values of the load network depicted in figure 1 can be determined. The load resistance that is found in this way is lower than 50 Ω, so a transformer or matching network is required.

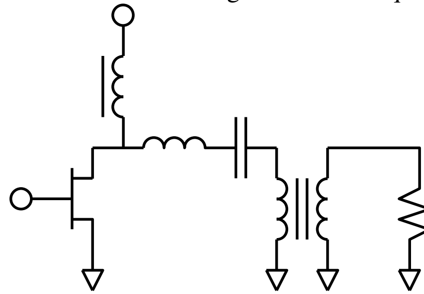

Fig. 1 Schematic of Class E load network with transformer to transform the load resistance to 50 Ω.

The transistor is biased just above pinch-off at a gate voltage of -1.4 V. This is done to increase the gain and as such reduce the effect of the input stage on the overall efficiency. To obtain a high efficiency over the desired frequency band an optimizer is used to shift the load at the fundamental and harmonic frequencies.

The classical class E network based on calculation gives a drain efficiency of 60%. Further optimization improves the drain efficiency with a sinusoidal gate drive to 75% at the expense of output power. Sacrificing a small amount of efficiency can give significantly more output power. The selected load gives a high efficiency with sufficient output power. The result is a chip size that is still reasonable.

The procedure to determine the load applied to the output of the transistor is an iterative procedure:

1. Determine the optimum load for overall efficiency versus the gate voltage with the standard class E network.

2. Make an output matching network providing the load required at the fundamental and try to move the harmonic termination to the required value.
3. Determine the load at the fundamental with the harmonic termination from the output matching network.
4. Iterate points 2 and 3.

The load found with this procedure is different than the class E load calculated using either [1] or [3]. Figure 2 shows the simulated drain voltage and drain current at 3.3 GHz. It can be seen that the drain current is already increasing at the moment that the drain voltage is not yet zero. Please note that the current through the capacitances present in the transistor is also present in the drain current plotted. For a rising drain voltage this will lead to an increased drain current and for a falling drain voltage to a reduced and even negative drain current.

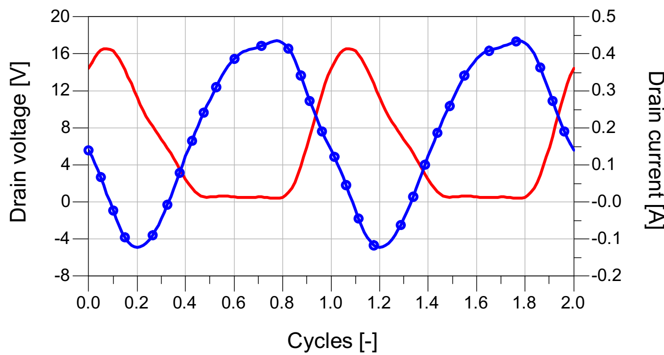

Fig. 2 Simulated drain voltage, without markers on left axis, and drain current, with markers on right axis at 3.3 GHz.

For the efficiency of the transistor it is important to have a short at the second harmonic at the gate. This will force the driving voltage of the gate from a triangular waveform to a more sinusoidal waveform, which is closer to the ideal square waveform required for switching the transistor. This increases the simulated drain efficiency of the transistor from 70 to 75%. The resulting harmonic terminations at the drain at the second and third harmonic are close to an open.

Table I lists the loads at the fundamental frequency that have been obtained using this procedure.

TABLE I
FOUND LOADS VERSUS FREQUENCY FOR AN 8X300 TRANSISTOR AT A DRAIN VOLTAGE OF 7 V AND A GATE VOLTAGE OF -1.4 V

Frequency [GHz]	Load [Ω]
2.6	29.8 + j21.9
2.8	22.3 + j23.1
3.0	21.6 + j20.9
3.2	21.3 + j20.0
3.4	20.3 + j19.7
3.6	18.3 + j18.5
3.8	17.5 + j18.1
4.0	17.1 + j18.0

The required load is provided to the eight transistors in the output stage by the output network. It also provides the bias to the drain of the transistors. Special care is taken to minimize the loss the network and provide the right harmonic terminations.

The interstage network matches the input impedance of the output stage to a class AB load used by the input stage transistor. It also contains stabilization networks to stabilize the output stage transistors. To improve the efficiency of the output stage a short at the second harmonic is applied at the input of the output stage transistors. The input stage is biased at a gate voltage of -1.2 V instead of -1.4 V to improve the gain.

The input network matches the input stage to 50 Ω. Also here the second harmonic at the gate is shorted to have a more square gate voltage. This improves the efficiency of the input stage even for the lower drive level present at that point.

A gate bias circuit has been designed to compensate for the process variations. The design is based on [4] with an extra source follower to reduce the output impedance without requiring excessive amounts of current. An impedance of 10 Ω or lower is required. Without a source follower this will result in a current of 140 mA flowing through a resistor, which is unacceptable. Low output impedance is required to reduce the effect of negative gate currents that can flow when the breakdown-voltage is exceeded during short periods. The negative gate current shifts the bias point of the output stage from just above pinch-off to a class AB bias point. This shift in bias point will reduce the efficiency. A lower impedance of the bias circuit will reduce the shift in bias point and as such reduce the reduction in efficiency. As can be seen in figure 3 the simulated gate to drain voltage exceeds the breakdown voltage of 20 V for frequencies in the lower part of the band.

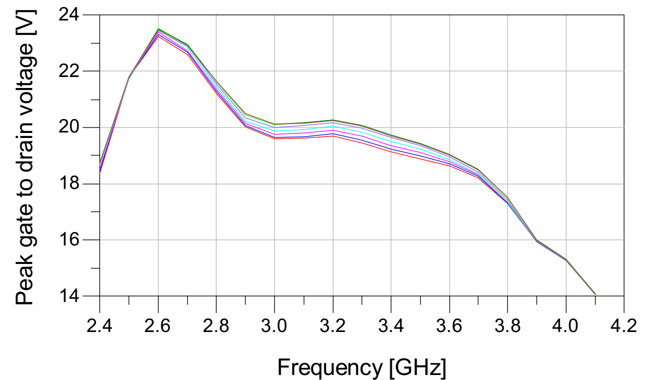

Fig. 3 Simulated peak gate-to-drain voltage of the transistors in the output stage.

III. MEASUREMENT RESULT

Figure 4 shows a chip photograph of the fabricated S-band class E amplifier.

It can be seen that the output stage takes approximately half of the chip area. After on-wafer small signal screening selected chips have been mounted on a CuMo carrier for large signal characterization. During the on-wafer screening the designed gate bias circuit was not functional due to an

oscillation around 12 GHz. The oscillation is due to incorrect modelling of inductance in series with a decoupling capacitor in the gate bias circuit. For this reason the gate bias circuit was bypassed during the measurements. The resulting on wafer S-parameter variation is therefore much larger than would normally be expected.

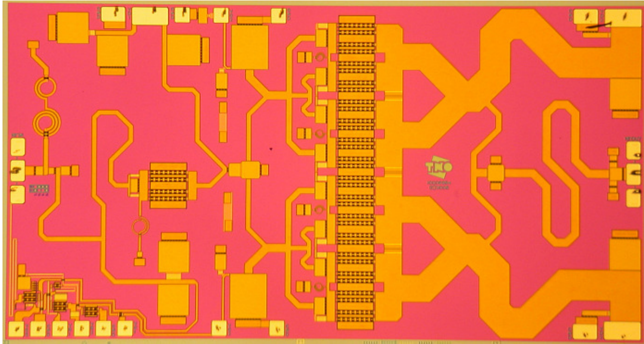

Fig. 4 Chip photograph of broadband S-band class E amplifier, chip size 5.25 x 2.8 mm^2.

Figure 5 shows the small signal gain. The thick lines are the 3σ borders of the measurement data. The thin line without markers is the original simulation result. The gain is 1 to 2 dB lower than expected and has a large variation.

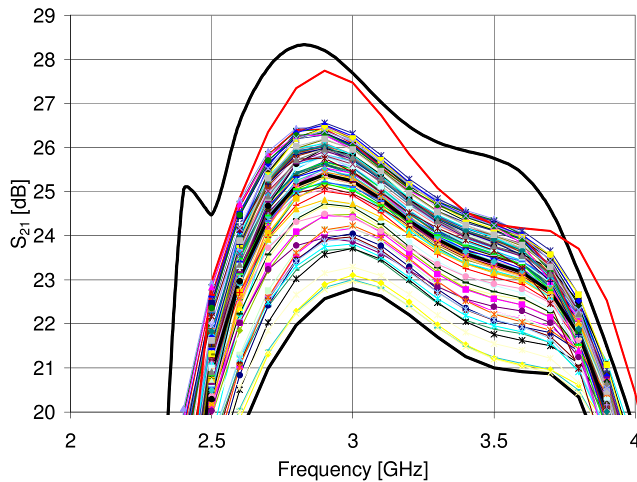

Fig. 5 Small signal gain (S_{21}) measured on-wafer at drain voltage of 7 V.

For the small signal input matching depicted in figure 6 the variation is smaller and also the simulated input matching (red line without markers) is close to the measurement result.

Figure 7 depicts the output matching. Since the load used is far from the conjugate match of the transistors the matching is only -6 dB for some frequencies. The simulation of the output matching (red line without markers) is in the bundle of measurements.

Figure 8 shows the measured power added efficiency (PAE) of three samples together with the simulation result. The PAE is above 50% from 3 to 3.75 GHz. In the low end of the band the PAE is reduced, this is in the region where the gate-to-drain voltage exceeds 20 V. Since the bias circuit has been bypassed by using a back-up resistive divider the impedance of the gate bias circuit is larger than with correctly operating bias circuit. At the low end of the frequency band negative gate current starts to flow that increases the DC gate voltage. The bias point is shifted from just above pinch-off to a class AB bias point. As a consequence the efficiency is reduced for these frequencies.

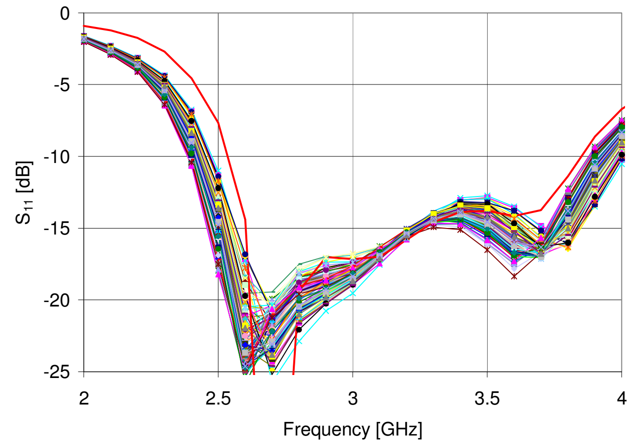

Fig. 6 Small signal input matching (S_{11}) measured on-wafer at V_{DS}= 7 V.

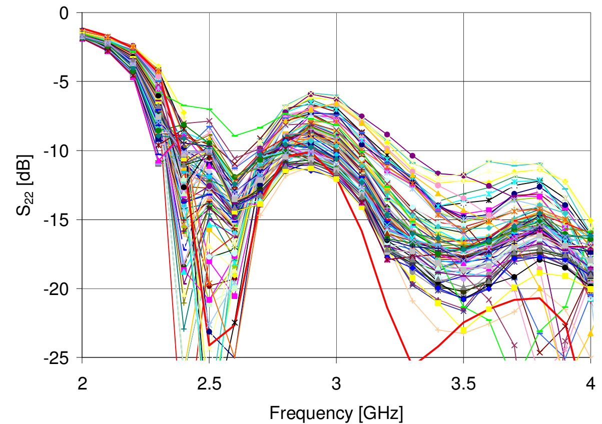

Fig. 7 Small signal output matching (S_{22}) measured on-wafer at V_{DS}=7 V.

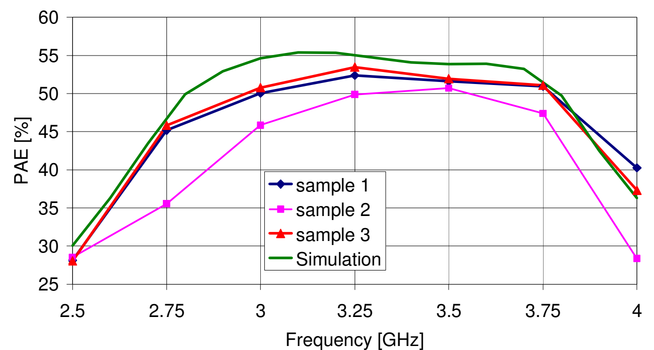

Fig. 8 Measured PAE of three samples and simulation result at V_{DS}=6 V.

Figure 9 shows the measured output power of three samples together with the simulation result. An output power of 35.5 to 37 dBm is achieved, which is close the simulation result for 1 sample but 1 to 2 dB lower for the other two samples. The measured output power is about 3 dB lower than would be

achieved using a class AB design. This is due to the fact that for a class AB design a higher drain voltage can be used. In addition the class E load used is not optimal with respect to output power, but for efficiency.

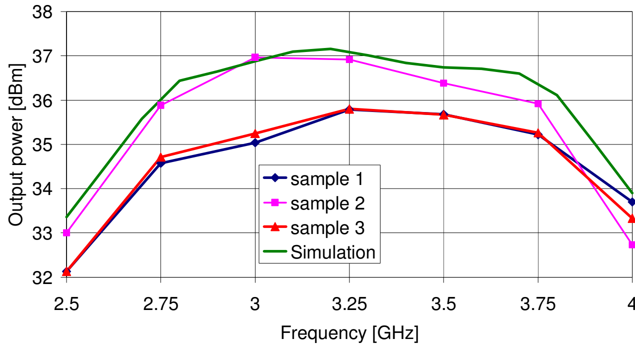

Fig. 9 Measured output power of three samples and simulation result at a drain voltage of 6 V.

Figures 10 and 11 show the PAE and output power of sample 1 versus the drain voltage. It can be seen that the efficiency is greatly reduced at drain voltages of 7 and 8 V. This is due to the shift in gate voltage caused by negative gate current, which would be much less with a correct gate bias circuit.

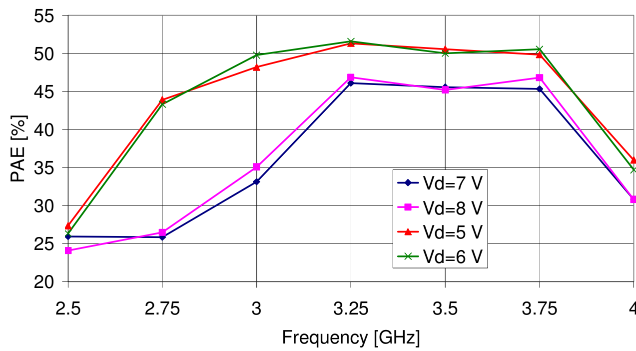

Fig. 10 Measured PAE of sample 1 versus drain voltage.

The output power is 2 to 3 dB higher at 7 and 8 V. The difference of 1 to 1.5 dB is larger than would normally be expected due to the shift in gate voltage.

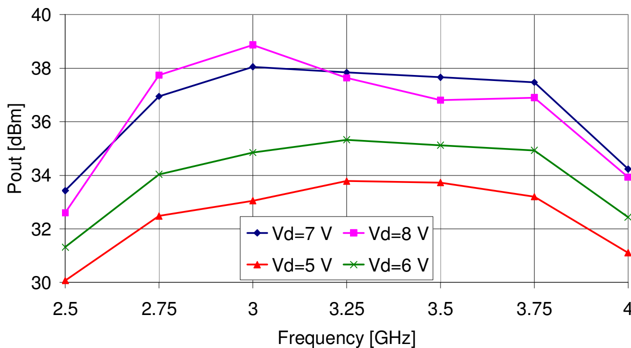

Fig. 11 Measured output power of sample 1 versus drain voltage.

Table II lists a summary of typical performance achieved with this design at a drain voltage of 6 V.

TABLE II
TYPICAL PERFORMANCE AT A DRAIN VOLTAGE OF 6 V FROM PULSED MEASUREMENTS

Parameter	**Unit**	**Value**	**Remark**
Frequency	GHz	2.75 – 3.75	<1 dB power variation
Drain supply	V	6	
PRF	kHz	10	
Duty Cycle	%	10	
Ambient temperature	°C	25	
Output power	dBm	35.5	Input power 15 dBm
Gain	dB	20	Input power 15 dBm
PAE	%	50	
Input reflection coefficient	dB	< -12	

IV. CONCLUSIONS

A broadband S-band class E amplifier with 50% PAE and a large signal gain of 20 dB has been designed and measured. The small signal measurement and simulation results are in close agreement. The large signal PAE has a reasonable fit, but the output power is 1 to 2 dB lower than simulated. Due to a non-functional gate bias circuit the drain voltage has been reduced from 7 to 6 V. With a functional gate bias circuit a drain voltage of 7 V can be used which leads to 1 to 1.5 dB more output power at the same efficiency.

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