X-band Phase-Shifting Dual-Output Balanced Amplifier MMIC

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***Abstract* — An X-band MMIC containing two 6 bit phase shifters and 1 Watt amplifiers in balanced configuration has been developed. The device has two output ports. The balance between the output powers of the two ports can be controlled via de phase shifter settings. This MMIC could be applied in systems where variable linear polarisation control is required, such as polarimetric radar or satellite communication systems. The MMIC has been developed in the 6-inch 0.5 µm power GaAs pHEMT process (PP50-11) of WIN Semiconductors.**

I. INTRODUCTION

Balanced amplifiers are frequently used components in microwave systems. A commonly used configuration consists of a 90° coupler at the input which divides the power over two equal branches that contain the amplifiers. At the output the same type of coupler is used in order to combine the signals in phase. This results in an output signal at one output of the coupler. The second output is terminated in 50 Ω and in the ideal case (i.e. perfect phase balance and no reflections in the branches) no power is delivered from this output.

By controlling the insertion phase of the individual branches the summation of the two signals at the output coupler can be controlled. The power at each of the coupler outputs now depends on the phase settings of the branches. This yields an amplifier with two outputs; the balance between the output powers of the two output ports can be controlled by adjusting the phase shifters settings. Benefit of this methods of amplitude control is that the individual amplifiers can always operate at there maximum power level which means that an equal amount of power is available for all balance settings and furthermore the efficiency remains constant.

This paper describes such a balanced amplifier with output balance control. A possible application is linear polarisation control for example in polarimetric radar or satellite communication systems. In such a system the device is used combination with a dual polarization antenna where the individual outputs are connected to the two (H and V) inputs of the antenna. Since the overall insertion phase is also adjustable, the amplifier is suitable for application in a phased array transmit module.

II. OPERATING PRINCIPLE

The topology of the developed MMIC is shown in Fig. 1. The two branches of the balanced amplifier each contain a six bit phase shifter and an amplifier. The input signal of the MMIC is distributed to the two branches with a Wilkinson power divider. At the output the two signals are combined using a Lange coupler. The two outputs of the MMIC are indicated as out H and out V.

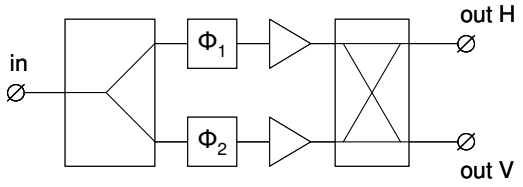

Fig. 1. Topology of MMIC.

With the given topology both the insertion phase difference Θ between the two branches as well the overall insertion phase can be controlled. The voltage ratio for the signals from the two output ports is given by (see Appendix):

$$\frac{H}{V} = \frac{\cos\Theta}{1+\sin\Theta} \qquad (1).$$

Equation (1) is zero for Θ=+90°. Furthermore if Θ approaches -90°, (1) will approach ±∞. This implies that for a differential phase setting of +90°, all the power comes from output V, while for a differential phase setting of -90°, all the

power comes from output H. It is also seen that (1) is real, which means that the output signals are in-phase or have opposite phase, in spite of the phase shifter settings. This is important to guarantee linear polarization when the device is used in direct combination with an antenna.

The setting for the phase shifters Φ_1 and Φ_2 can be obtained from the required differential phase setting Θ and overall phase setting φ according to:

$$\Phi_1 = \varphi + \frac{\Theta}{2} \qquad (2a)$$

and

$$\Phi_2 = \varphi - \frac{\Theta}{2} \qquad (2b).$$

III. Design and Realization

The phase shifters have a resolution of 6 bits, corresponding to an LSB value of 5.625°. A block diagram of the realized MMIC is shown in Fig. 2. The order of the phase sections is optimized for power performance. Each amplifier contains two stages. The transistors of the stages have eight gate fingers with a width of 150 µm each. The drain voltage of the transistors is 8 V and the transistors are biased at class AB. The target operating frequency band of the MMIC is 8.5 to 11 GHz.

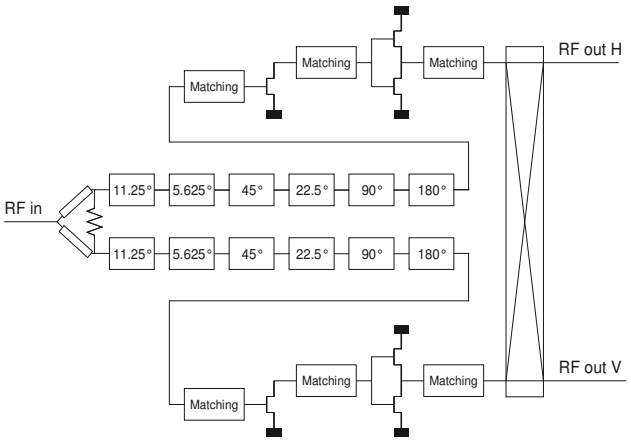

Fig. 2. Block diagram balanced PSPA.

The MMIC is designed in the PP50-11 0.5 µm pHEMT GaAs power process of WIN semiconductor. The layout of the MMIC is depicted in Fig. 3. The Wilkinson divider is located at the centre of the device. The two branches containing the phase shifters and amplifiers are mirrored with respect to each other. Each phase shifter has its own digital control logic which enables the use of single ended LVCMOS compatible digital control signals [1]. The gate biasing of the HPA is performed by an active gate bias circuit with 100% of compensation for threshold voltage variation [2].

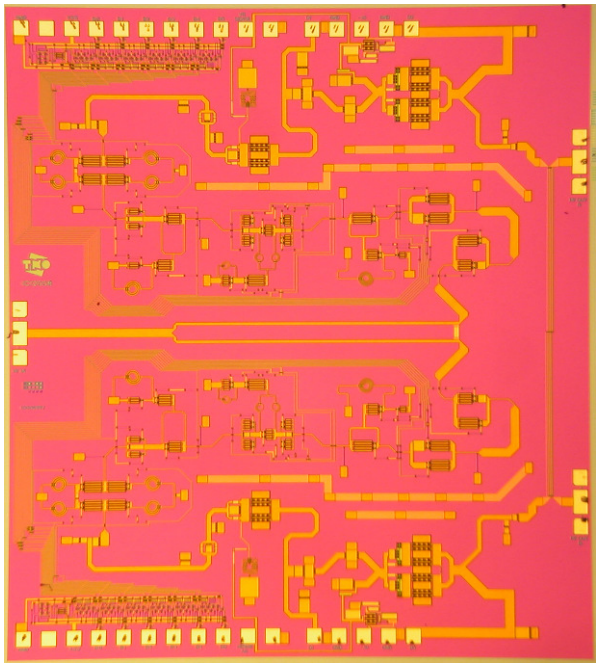

Fig. 3. Photograph of balanced PSPA MMIC. Chip dimensions are 4.8 x 5.3 mm^2.

IV. Measurement Results

The small signal gain of the path from the input to output H is shown versus frequency in Fig. 4. Here the overall phase setting φ is varied from 0° to 360° while the differential phase Θ is kept constant at 0°. With this differential phase setting the output power is equally divided between the two outputs. It is seen that the small signal gain of this path varies between 4 dB and 7 dB. An equal gain was measured for the path from input to output V.

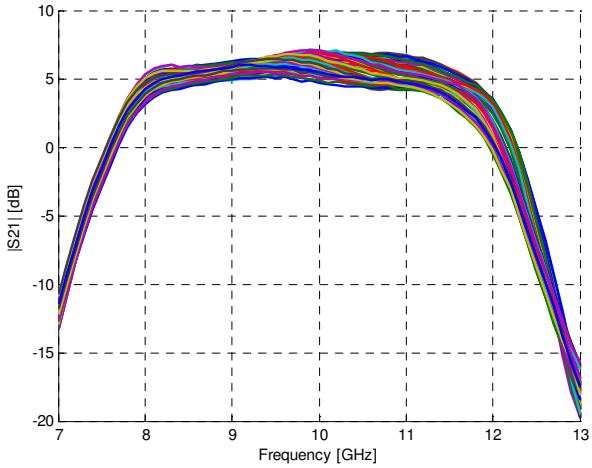

Fig. 4. Small signal gain for different values of φ, Θ=0°, Vd=8 V, Vgg=-10 V, T_A=25 °C.

The small signal input matching is shown in Fig. 5 for all possible combinations of Θ and φ. For the majority of phase states the matching is better than -9 dB within the operating frequency band.

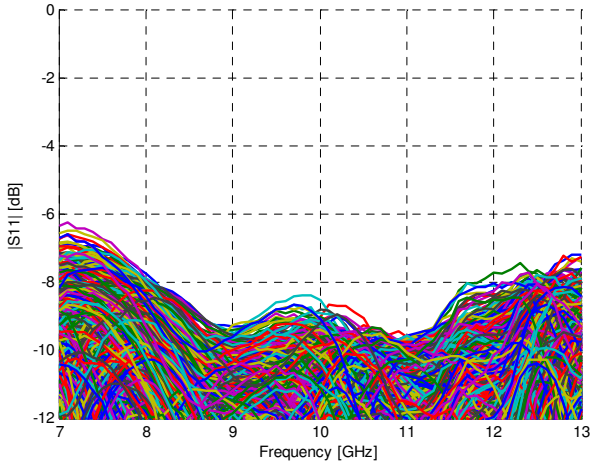

Fig. 5. Small signal input matching for different values of φ, Θ=0°, Vd=8 V, Vgg=-10 V, T_A=25 °C.

The small signal output matching on both outputs is shown in Fig. 6 for all possible combinations of Θ and φ. The matching is better than -17 dB within the operating frequency band.

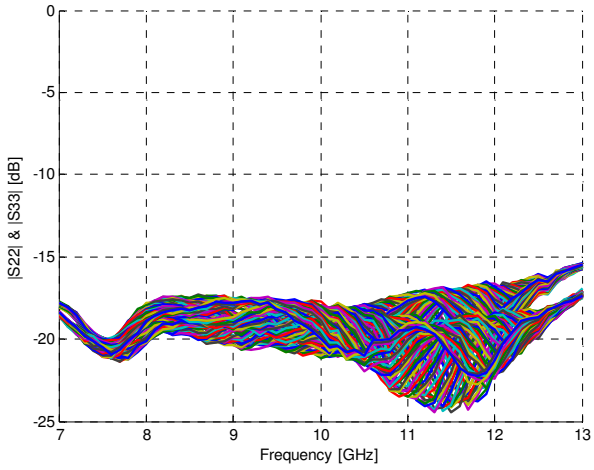

Fig. 6. Small signal output matching for different values of φ, Θ=0°, Vd=8 V, Vgg=-10 V, T_A=25 °C.

The output power at the individual outputs together with the total output power at the 1 dB compression point is shown in Fig. 7 as a function of frequency for a single differential phase setting Θ of 0°. It is found that for frequencies between 8.5 GHz and 11 GHz, the total output power varies between 33.8 dBm and 34.5 dBm.

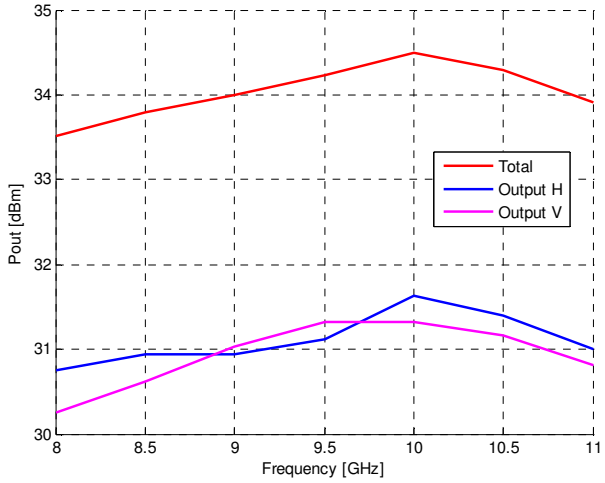

Fig. 7. Total and individual output power versus frequency Θ=0°, φ=0°, P_S=29 dBm, Vd=8 V, Vgg=-10 V, T_A=25 °C.

Fig. 8 shows the output power distribution over the two output ports as a function of differential phase setting Θ for all possible values of φ. It is seen that the total output power is constant within 0.5 dB while the output power on the individual V and H ports are varying with Θ as described by (1). The total output power variation as result of varying φ is approximately 0.2 dB.

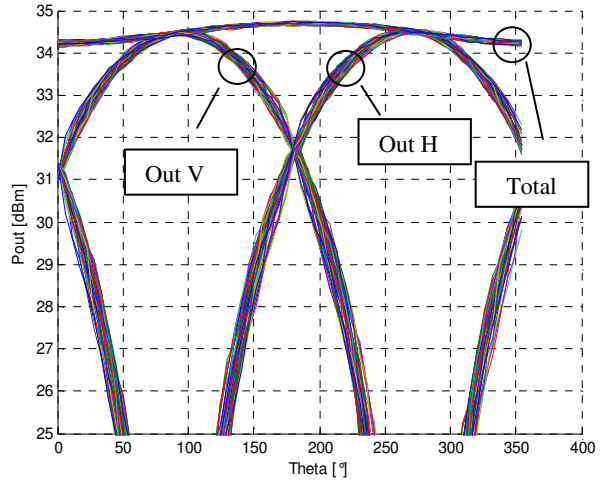

Fig. 8. Output power versus Θ, φ=0 to 360°, f=9.5 GHz, P_S=20 dBm, Vd=8 V, Vgg=-10 V, T_A=25 °C.

The difference between the insertion phase of the two paths from input to H and input to V is shown in Fig. 9 as a function of Θ for all possible values of φ. It is seen that around Θ settings of 0 ° and 180 ° the insertion phase difference is 0 ° or 180 °. This corresponds to the conclusion drawn from the fact that (1) is real. Around Θ settings of 90 ° and 270 ° the insertion phase difference deviates from the expected 0 ° or 180 °, due to fact that the output signals at one of the ports is very small at these settings, as was already seen in Fig. 8. In

the ideal case the signals at these settings are zero which causes the phase difference to be undefined.

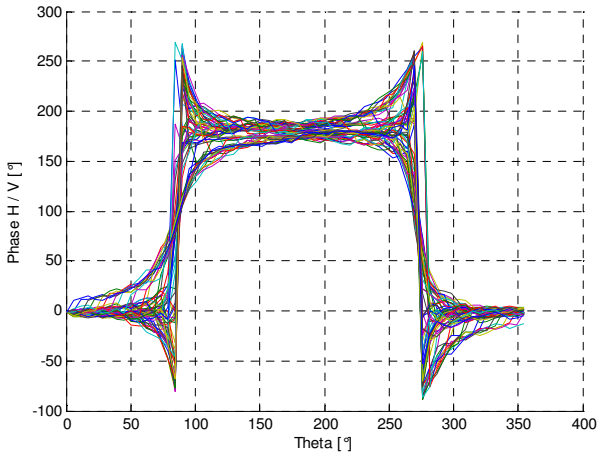

Fig. 9. Small signal phase difference between output ports versus Θ, φ=0 to 360°, f=9.5 GHz, Vd=8 V, Vgg=-10 V, T_A=25 °C.

V. Conclusion

A balanced phase shifting amplifier with two outputs has been designed. It is demonstrated that the distribution of the output power over the two outputs can be controlled with the phase shifter settings. A possible application of such an amplifier is variable linear polarisation for polarimetric radar or satellite communication systems.

Appendix

The equation for the voltage ratio between the two output signals is derived. Starting point is the topology repeated in Fig. 10.

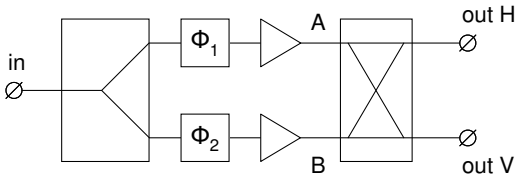

Fig. 10. Topology of MMIC.

It is assumed that the Wilkinson divider is ideal and both amplifiers have the same insertion gain. Therefore the phase difference between the two input signals of the Lange coupler A and B equals the difference between Φ_1 and Φ_2:

$$A = B \cdot e^{j(\Phi_1 - \Phi_2)} = B \cdot e^{j\Theta}.$$

If B is defined as unity than $A = e^{j\Theta}$.

When the Lange coupler is assumed to be lossless, the signal at H is given by:

$$H = \frac{A - j \cdot B}{\sqrt{2}} = \frac{e^{j\Theta} - j}{\sqrt{2}}.$$

For the signal at V holds:

$$V = \frac{B - j \cdot A}{\sqrt{2}} = \frac{1 - j \cdot e^{j\Theta}}{\sqrt{2}}.$$

The ratio between H and V can now be expressed as:

$$\frac{H}{V} = \frac{e^{j\Theta} - j}{1 - j \cdot e^{j\Theta}}.$$

Multiplying the numerator and denominator with $1 + j \cdot e^{-j\Theta}$ yields after manipulation:

$$= \frac{e^{j\Theta} + e^{-j\Theta}}{2 + j\left(e^{-j\Theta} - e^{j\Theta}\right)}.$$

By substituting $e^{j\Theta} + e^{-j\Theta} = 2\cos\Theta$ and $e^{-j\Theta} - e^{j\Theta} = -2j\sin\Theta$ and manipulating:

$$\frac{H}{V} = \frac{\cos\Theta}{1 + \sin\Theta}.$$

References

[1] M. van Wanum, G. van der Bent, M. Rodenburg, A.P. de Hek, "Generic robust LVCMOS-compatible control logic for GaAs HEMT switches", *EuMIC 2006*, Manchester, September 2006.

[2] A.P. de Hek, E.B. Busking "On-chip active gate bias circuit for MMIC amplifier applications with 100% threshold voltage variation compensation", *EuMIC 2006*, Manchester, September 2006.