Robust X-band LNAs in AlGaN/GaN technology

J.P.B. Janssen[1], M. van Heijningen[1], G.C. Visser[1], M. Rodenburg[1], H.K. Johnson[2], M.J. Uren[2], E. Morvan[3] and F.E. van Vliet[1]

[1]*TNO Defence, Security and Safety*
Oude Waalsdorperweg 63 Den Haag, The Netherlands
[1]jochem.janssen@tno.nl
[2]*QinetiQ Ltd.*
Malvern, Worcestershire WR14 3PS, United Kingdom
[3]*Alcatel- Thales III-V lab.*
Route de nozay, 91460 Marcoussis, France

Abstract— **Gallium-Nitride technology is known for its high power density and power amplifier designs, but is also very well suited to realise robust receiver components. This paper presents the design, realisation and measurement of two robust AlGaN/GaN low noise amplifiers. The two versions have been designed in the Alcatel-Thales III-V lab AlGaN/GaN microstrip technology and in the QinetiQ AlGaN/GaN coplanar waveguide technology. Both LNAs operate at X-band. An input power handling of >41 dBm for the first iteration design of the Alcatel-Thales III-V lab version has been published [3][5]. The designs and measurement results of the two realised low noise amplifiers are presented in this paper. The results show that gallium nitride is a suitable technology for robust receiver design.**

I. INTRODUCTION

The wide bandgap semiconductor technology Gallium-Nitride (GaN) is well known for its high power density and many high power amplifier designs [1]. Because of the large breakdown voltage of HEMT devices realised in the AlGaN/GaN technology, it is also possible to use this technology to design robust receiver components. GaN technology has already shown the capability for low noise performance, and even with a technology optimised for high-power applications, good and robust low noise amplifiers (LNA) can be realised [2],[3]. Because of the high power handling also switches can be designed that could replace the current ferrite circulators in Transmit/Receive (TR) modules. This paper will present the design and measurement results of two LNAs, which can be used to realise a robust receiver front end. One LNA designed in the AlGaN/GaN process of QinetiQ and one version in the AlGaN/GaN process of Alcatel-Thales III-V lab. First in section II the application of these MMICs in a TR module front-end is described. Section III gives details on the used AlGaN/GaN processing technologies. Next the LNA designs are described and the measurement results are presented.

II. ROBUST RECEIVERS

Current TR modules for radar and telecommunication applications usually include a limiter on the receive side to protect the GaAs LNA against too high input power. This limiter is often realised with discrete and expensive components, such as PIN diodes. As presented in [2] and [3], GaN LNAs can withstand input power levels up to 41 dBm and a smaller limiter or no limiter at all could be used. Thereby the bulky and expensive circulator can be replaced by a GaN TR switch. Overall this will result in smaller, more light-weight and finally cheaper TR modules [3], [4].

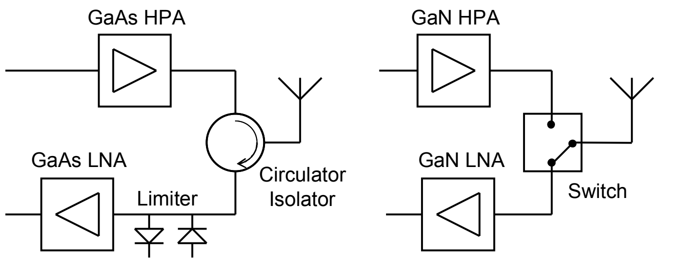

Figure 1 A schematic of a classical GaAs based front-end and a robust GaN front-end.

III. TECHNOLOGIES

The LNAs presented are designed in two AlGaN/GaN technologies. The first LNA is designed in the coplanar waveguide process (CPW) of QinetiQ. The second LNA is design in the microstrip process of Alcatel-Thales III-V lab. A description of both technologies is presented in this section.

A. QinetiQ AlGaN/GaN CPW technology

The circuits were implemented using the coplanar waveguide GaN MMIC technology established at QinetiQ. The epitaxial growth was carried out in a Thomas-Swan CCS MOVPE reactor and used a layer structure consisting of 25 nm of undoped $Al_{0.25}Ga_{0.75}N$ on a 1.9 µm thick Fe doped insulating GaN layer grown on 3” 4H SI SiC. The process flow was fairly conventional, using TiAlPtAu alloyed Ohmic contacts and a NiAu 0.25 µm T gate. Devices were passivated with a PECVD $SiN_x/SiO_2/SiN_x$ multilayer dielectric stack which doubled as the MIM capacitor dielectric and had a breakdown voltage >200 V. Thin film resistors were implemented using NiCr with a sheet resistance of 27 Ohm/sq. Inductors and coplanar transmission lines were implemented in 3 µm plated gold with air-bridged underpasses using a 0.8 µm evaporated gold feed metal layer. The GaN HFETs had a contact resistance of 0.31 Ohm.mm, gm of 270 mS/mm, Idss0 of 980 mA/mm, pinch-off voltage of -4.9 V, an on-resistance of 3.7 Ohm.mm, f_T of 45 GHz and a gate breakdown voltage >70 V.

B. Alcatel Thales III-V lab microstrip technology

The MMICs have been processed on a multi-project wafer in the high-power AlGaN/GaN technology of the Alcatel-Thales III-V lab "Tiger". The electrical isolation of devices was performed by helium implantation. Ti/Al/Ni/Au ohmic contacts were formed using rapid thermal annealing at temperature of 900°C. Mean contact resistance extracted from TLM measurement is 0.21 Ω.mm. Mo-based T-gates with 0.25 µm length were defined by electron beam lithography. The devices were then passivated using plasma enhanced chemical vapour deposition (PECVD) of SiO_2/Si_3N_4 at a temperature of 340°C. Interconnects were made with evaporated Ti/Pt/Au and electroplated gold for the 3D interconnects (bridges). Passive elements consist in PECVD nitride MIM capacitors, NiCr resistors and evaporated Ti/Pt/Au inductances. After front side processing, the SiC wafer was mounted on a sapphire substrate and thinned down to 100 µm. Plasma etching via-holes technology was used to ground the devices. Vias and back side metallization consisted in sputtered TiW/Au and Au plating.

IV. LNA DESIGNS AND RESULTS

The LNAs presented in this paper concern second iteration designs in the two different technologies as described in the former paragraph. A complete redesign is carried out for the QinetiQ LNA, while the III-V Lab LNA is an improvement of the 1st iteration design [3][5]. The gain for both LNAs was targeted on 19 dB, the noise figure lower than 2 dB and survivability of 41 dBm input power. The bandwidth was targeted on 8 GHz – 11 GHz.

A. LNA in QinetiQ technology

The LNA designed in QinetiQ technology is a three stage LNA based on a 2x125 µm device for the first stage and 4x125 µm devices for the second and third (output) stage.

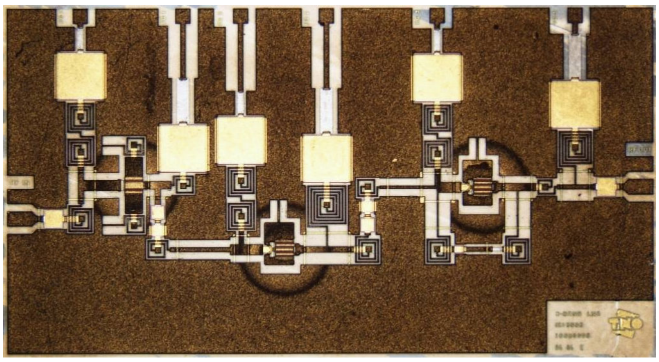

Figure 2 Photograph of the QinetiQ LNA (2.3 x4.3 mm)

The first stage is carried out with source inductance to employ source degeneration to be able to match S_{11} and Γ_{opt} simultaneously. Two inductors were used for each source, because no airbridge is available for 2 fingered FETs. The second stage is designed for maximum gain and uses therefore no source degeneration. An RLC feedback network is employed in the output stage from drain to gate to flatten the gain over the frequency band.

The used transistor models are based on noise parameter and noise figure measurements and S-parameter measurements. A photograph of the realised LNA is presented in Figure 2.

B. LNA in III-V lab technology

The LNA designed in the microstrip technology of III-V Lab is based on earlier successful designs as presented in [3]. The goal of this design was to improve its performance. More gain is needed and the noise figure has to be lower.

The LNA is build-up of two stages based on 4x75 µm devices in each stage. The first stage is designed for minimum noise figure and maximum gain. Therefore source degeneration is used to match S_{11} and Γ_{opt} simultaneously. The output stage is implemented with an RLC feedback network to flatten the gain over frequency. The transistor models are based on noise parameter and noise figure measurements and S-parameter measurements. A photograph of the LNA is presented in Figure 3.

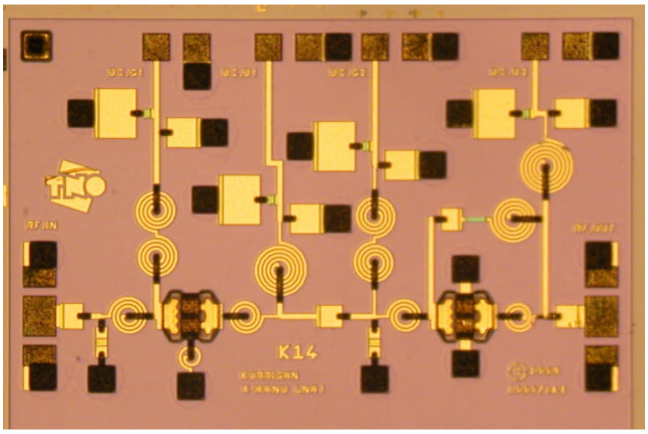

Figure 3 Photograph of the III-V lab LNA (1.6 x2.2 mm)

V. MEASUREMENT RESULTS

The measurement results of the LNAs are presented in this section. Small-signal measurements, concerning S-parameters and noise figure, were carried out with an Agilent PNA-X network analyser. Large signal measurements to determine 1 dB compression point were carried out in continuous wave mode.

Due to the limited number of available samples no destructive measurements were carried out to analyze the high power survivability.

A. *Results of the Qinetiq LNA*

The QinetiQ LNA is simulated and measured with a drain voltage of 15 V for each gain stage. The drain current is biased at 27 mA for the first stage and 42 mA for the second and third stage.

Figure 4 shows the gain of the QinetiQ LNA. The simulated gain is more than 23 dB in a large area of the target frequency band with gain flatness of ±1 dB. The measured gain is lower, due to oscillation at 40 GHz. Therfore large signal measurements were not carried out. The noise figure is simulated lower than 2 dB in the same frequency band. The measurement results match well with the simulated noise figure, which is lower than 2 dB up to 10.5 GHz (Figure 5).

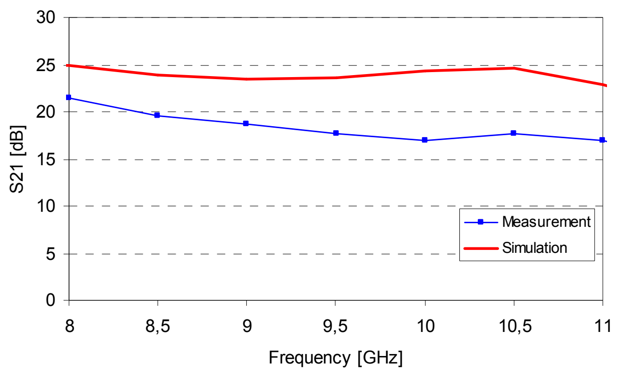

Figure 4 Simulated and measured gain of the QinetiQ LNA.

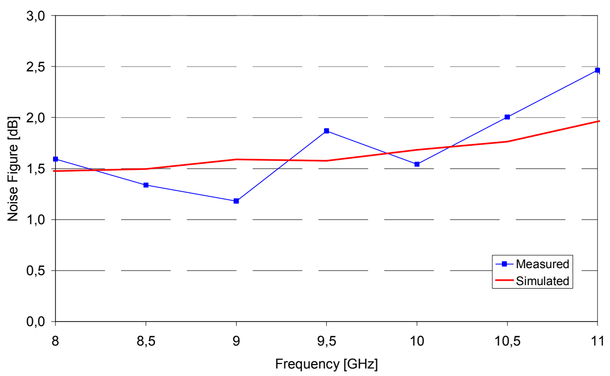

Figure 5 Simulated noise figure of the QinetiQ LNA.

Figure 6 shows the input return loss (S_{11}). The simulated S_{11} is lower than -8 dB in the complete target frequency band. The measured S_{11} is worse on the low side of the frequency band, up to -2.5 dB at 8 GHz. The simulated output return loss (S_{22}), which is presented in Figure 7, is better than -10 dB at X-band. The measured S_{22} rises at the high side of the frequency band.

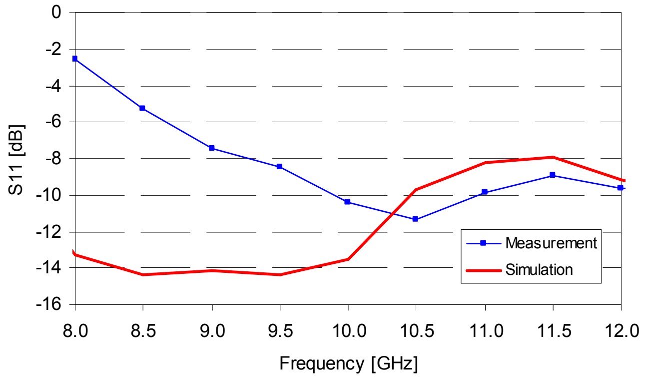

Figure 6 Simulated and measured input return loss of the QinetiQ LNA.

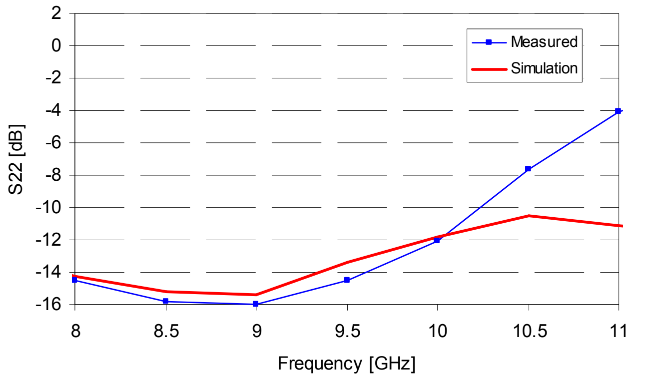

Figure 7 Simulated and measured output return loss of the QinetiQ LNA.

B. *Results of the III-V lab LNA*

The LNA, designed in III-V lab technology is simulated and measured with a drain voltage of 15 V and a drain current of 20 mA for both gain stages.

The simulated gain of the LNA is more than 18 dB at X-band (Figure 8) with gain flatness of ± 0.5 dB. The measured gain turns out around 20 dB, which is more than 1 dB higher than the simulated gain. The noise figure is simulated lower than 2.5 dB at the same frequency band and the measured noise figure matches good with the simulations and is flat in the complete frequency band. The simulated and measured noise figures are presented Figure 9.

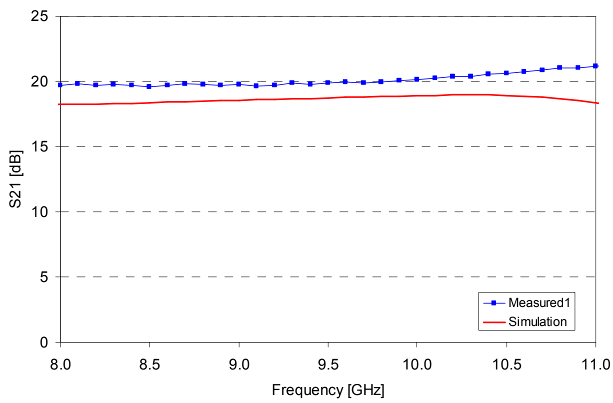

Figure 8 Simulated and measured gain of the III-V lab LNA.

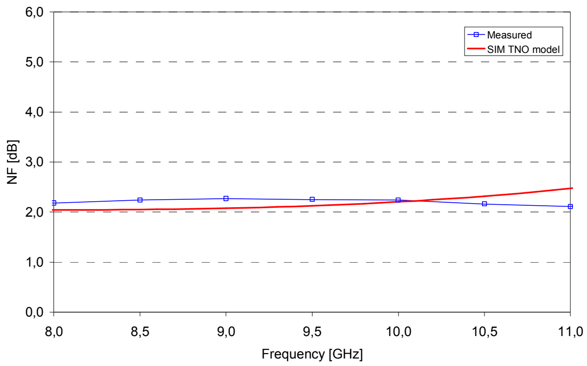

Figure 9 Simulated and measured noise figure of the III-V lab LNA.

Input return loss, as presented in Figure 10 is kept lower than -9 dB in simulation, which is a direct trade-off with the noise figure. Measurement shows a higher input return loss, partly due to a frequency shift. Also the measured output return loss is higher than the simulated value of lower than -14 dB in X-band (Figure 11).

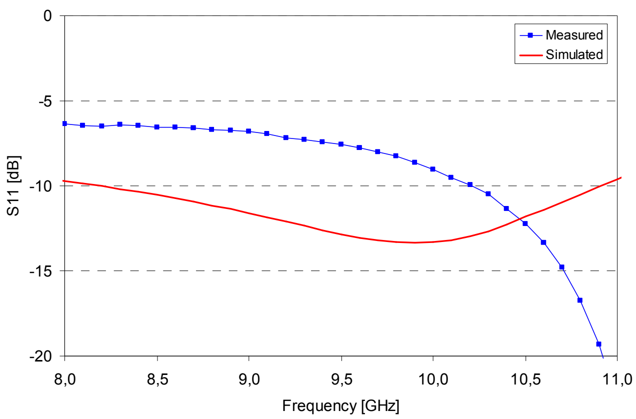

Figure 10 Simulated and measured input return loss of the III-V lab LNA

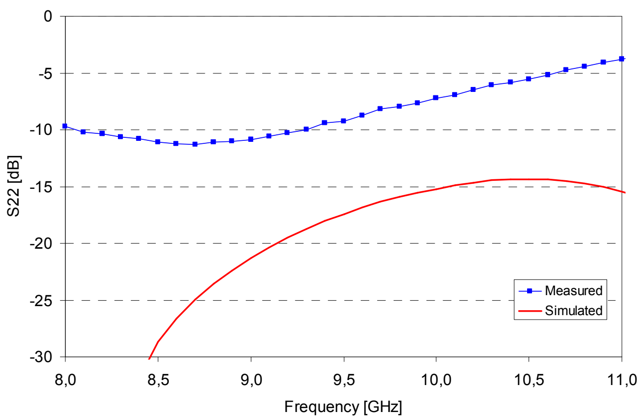

Figure 11 Simulated and measured output return loss of the III-V lab LNA.

Figure 12 presents the measured power transfer curve of the LNA. Despite the fact that the curve shows soft compression, the compressed output power level is higher than 20 dBm, which is higher than the measured range.

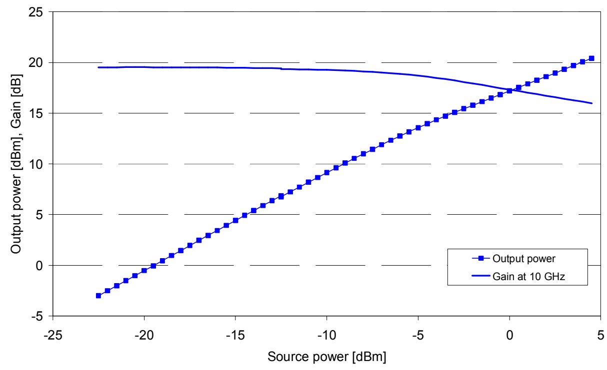

Figure 12 Measured output power and gain at 10 GHz.

VI. Conclusions

Two low noise amplifier circuits were succesfully designed in two different gallium nitride MMIC processes. One circuit is designed in QinetiQ coplanar waveguide technology and the second circuit is designed in the Alcatel-Thales III-V lab microstrip technology.

Despite that some mismatch between simulation and measurement is presented, the key results match well with the simulations and the noise figure measurement results are promising for designs in processes optimised for high power applications. Measurement also shows that high 1 dB compression points can be achieved.

In general the results show that gallium nitride technology is, besides for high power applications, suitable for robust receiver design.

Acknowledgment

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