GaN-HEMT VSWR Ruggedness and Amplifier Protection

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ABSTRACT

This paper presents the initial results in a study aimed at exploring the use of GaN-devices in applications where they are at risk of being exposed to high output voltage-standing-wave-ratio (VSWR) conditions. A measurement method developed to identify the limits of such stress is described together with the first results from measurements of novel FBH GaN-HEMT technology. Furthermore a circuit design aimed at preventing excessive operation under high output VSWR conditions is presented. The first findings suggest that the investigated devices are very robust to VSWR stress and the suggested protection circuit with a power-down cycle in the 100 ns range is sufficient to ensure a long lifetime with little degradation of RF performance.

I INTRODUCTION

There are many situations where RF-power amplifiers (PA) are at risk to be exposed to high reflections, i.e. high voltage-standing-wave-ratio (VSWR) conditions on their output, some unintentional due to bad handling of components and some more system incorporated. In for example Radar systems the transmitted signal is expected to return and at a system level that constitutes a reflection entering the system. During test of Radar system under non-anechoic conditions these reflected signals may be substantial and possibly cause overload with failure or reduced lifetime as a consequence. In many cases the power amplifier in the transmitter is therefore efficiently shielded from seeing any reflections by isolators on the output of the amplifier. These isolators are often based on ferrite solutions and introduce both bandwidth limitations and non-linearities. With a robust device technology in the PA, systems can be designed to withstand high VSWR without the use of isolators on the output enabling PAs with larger bandwidth and higher dynamic range [1]. Eliminating the isolators will also reduce the weight and size, two crucial parameters in for example space applications, and will enable higher levels of integration. This work presents a characterization method to test GaN devices for operation under VSWR stress and to identify safe operating regions with regards to high VSWR ruggedness. A circuit level approach to protect these devices from operating under unsafe VSWR conditions is also presented.

II VSWR STRESS TESTING

The VSWR stress test can be divided in two main issues:

1. Identifying the parameters that can be used as markers for when a device can be considered as permanently affected by stress and setting the limiting values for these markers

2. Setting up test-conditions that can properly emulate device operation for a real amplifier working under high VSWR conditions

Markers and Failure Conditions

Besides catastrophic failure with total malfunction as result there are slow aging processes in all semiconductors regardless of technology. GaN devices has been tested in this work and one of the most sensitive parameters in GaN devices often used do detect permanent damage is the gate quiescent current (I_{GQ}) [2]. In this work a post-stress change after burn-in of a factor 2 for I_{GQ} was used as a failure criteria. The mechanisms and parameters affected may be different for different technologies but the effect is the same, overall reduced performance of the PA over time. From an application perspective this makes the RF-power parameters the most interesting to test pre- and post- stress. In this work an output power (P_{OUT}) reduction of 1 dB post-stress was considered as permanent damage.

Since this work is based on GaN it has to be noted that some of theses parameters are not always constant under all operation conditions but may vary over time due to charging of traps that may cause temporary bias drift often noted as dispersion. In this work these effects have been monitored and all test have been conducted under similar operating conditions.

Emulating High VSWR Operating Conditions

High VSWR on the output of a power amplifier does not necessarily imply that a high VSWR is seen at the device reference plane internally in the amplifier, Fig 1.

The output matching network that provides a stable impedance on the load side is usually optimized for P_{OUT}. It constitutes a filter that transforms the reflection seen at the output (Γ_{VSWR}) of the amplifier. More losses in the load matching network reduces the size of the mapped reflections from the amplifier output which produce a lower stress (Γ_{Stress}) for the device. VSWR stress tests conducted at a test-board interface therefore impose considerably less stress on the device than a test conducted directly on the transistor output [3]. Measured on a board with impedance matching the device can however be kept in a safe operating region with regards to oscillations which may be necessary for high power devices. To provide a good design-basis with VSWR tests valid for any matching network regardless of network losses the tests in this work were carried out on-wafer directly at the device reference plane. Possible oscillations where monitored and catastrophic failure during oscillations where prevented using a fast drain current safe eFuse [4].

Test Setup

The VSWR stress tests were conducted in an on-wafer load- and source- pull test setup shown in Fig. 2. The RF-source was a performance-signal-generator (PSG) from Agilent. It provided the 2 GHz signal used in the tests and had the option to work in pulsed mode with RF-pulses down to about 20 ns pulse-width. A Miteq pre-amplifier was used capable of delivering more than 30 dBm output power in this frequency range. It was characterized under pulsed operation and had no severe impact on the pulse shape. Input and output matching was conducted in a Focus load-pull tuner system. Power, gain and efficiency were measured using the Load-Pull explorer software from Focus Microwaves. The load-pull system was calibrated down to the probe-tip interface using two-tier method and an ISS standard calibration substrate from Cascade.

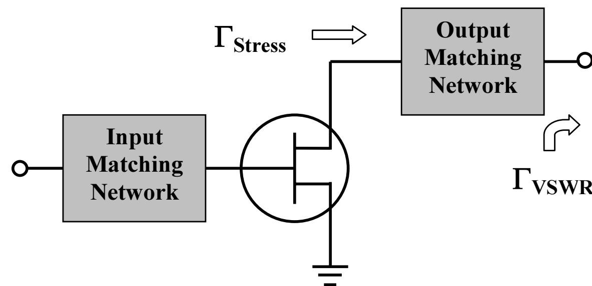

Fig. 1, Schematic outline of a power amplifier with stress and VSWR reference planes identified.

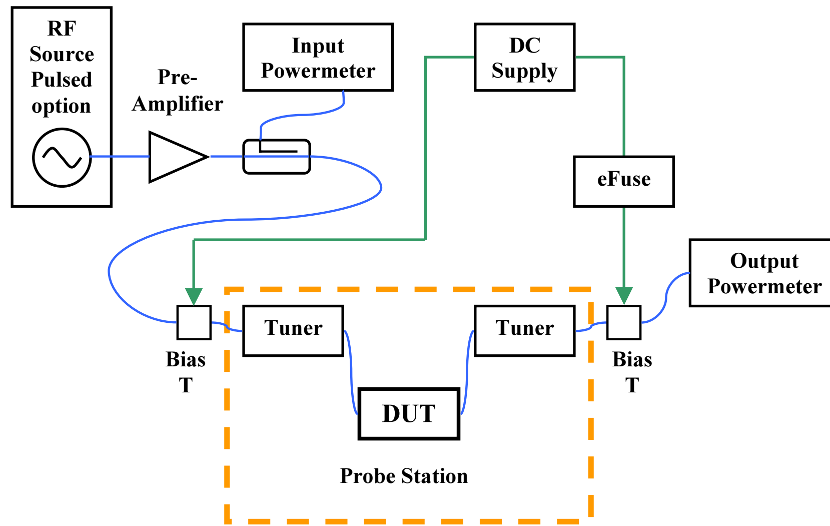

Fig. 2, Outline of the load- and source- pull system used in the VSWR stress tests.

Test Outline

The tests were conducted on three samples of a two-finger device with a total gate-width of 0.25 mm at a low class-AB bias point with a quiescent drain current (I_{DQ}) of 5-10% of the maximum drain current at a supply voltage of 35 V. Initially load- and source- pull was conducted to find the optimum matching for maximum P_{OUT}. The 2 dB compression point (P_{2dB}) was then identified in a power sweep. At the P_{2dB} available source power (P_{AVS}) the VSWR was altered in an increasing range from the optimum point at different phase-angles. Between each increase of VSWR the DC marker parameters I_{GQ} and I_{DQ} where measured together with a full RF-power sweep with the matching impedances restored to their initial optimum position. The VSWR stress tests had a duration of about 20 seconds per impedance point. For devices that showed an altered performance in any VSWR position a reduced time VSWR stress exposure for this point was possible by configuring the signal generator for pulsed operation down to 20 ns pulse-time. This was to verify the minimum time needed as activation time for a circuit based protection system.

In this initial work the studied device showed no degraded performance at the exposed 20 second time per point or totally 40 minutes high VSWR stress over 132 impedance points shown in Fig. 3. The reduced time test therefore never had to be used and marker monitoring was performed first after all impedance points had been measured.

The markers where were therefore monitored at four test instances:

1. Initially after optimum impedances were found
2. Post a power sweep at optimum impedance
3. After cooling
4. Post a full VSWR stress test at 132 impedance points

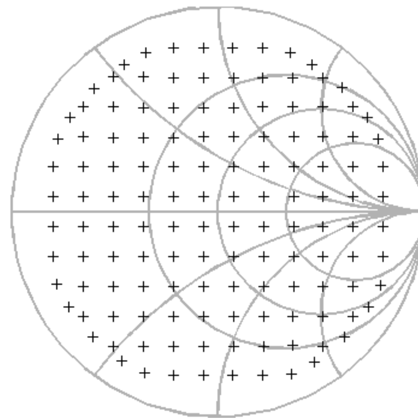

Fig. 3, Measured impedance points in the on-wafer VSWR stress-test.

III STRESS TEST RESULTS

The typical initial spread in output power between individual samples is shown in Fig. 4.

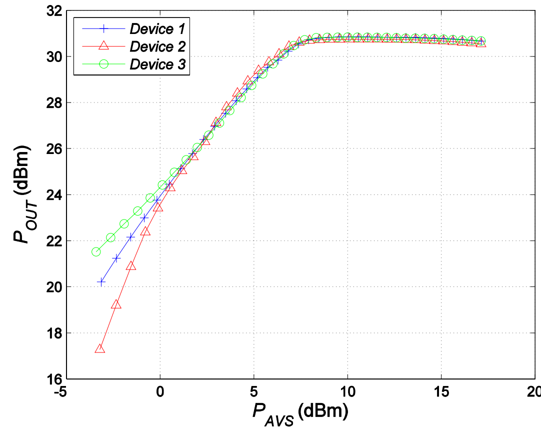

Fig. 4, Initial output power of three measured devices at a low class-AB point with a supply voltage of 35 V.

As can be seen the main difference is at low input power mainly due to the strong effect the power has on the charging of possible traps at the low bias-point. The effect seen is mainly a slight shift in threshold voltage due to this charged traps. In Fig. 5, typical changes with stress of the two monitored DC parameters are illustrated when measured at the four monitoring instances. As can be seen there is a large shift in gate current prior to VSWR stress merely from the first power sweep. This is considered to be caused by initial "burn-in" effects where charges are finding their initial positions and states. No further large changes are noted after cooling time and post VSWR stress. Fig. 6 shows the change in transducer gain (G_T) and Fig. 7, shows the change in drain efficiency (η_D) before and after stress.

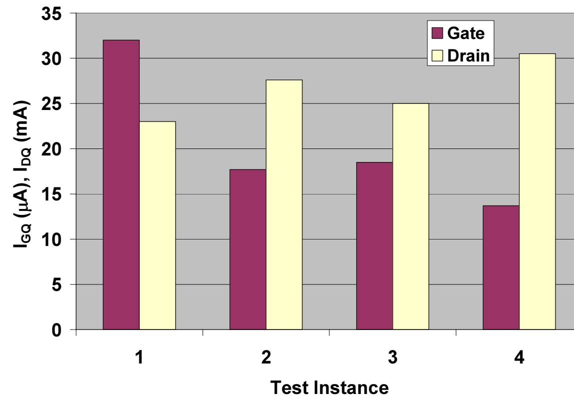

Fig. 5, Change in the monitored quiescent currents during test.

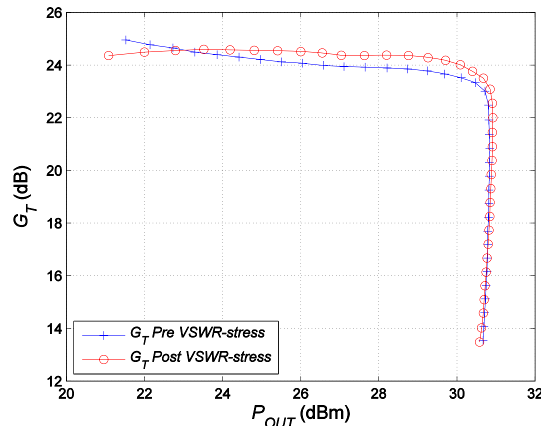

Fig. 6, Gain pre and post stress in a low class-AB bias point with a supply voltage of 35 V.

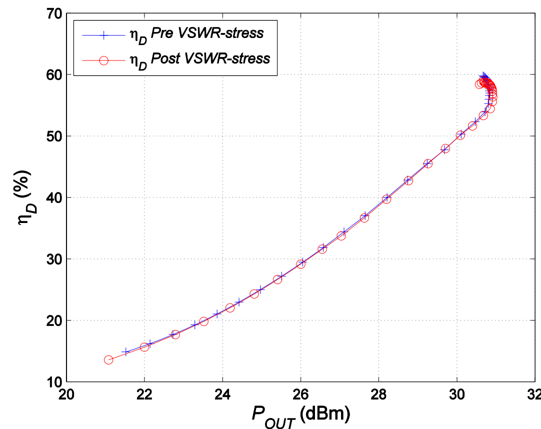

Fig. 7, Drain efficiency pre and post stress in a low class-AB bias point with a supply voltage of 35 V.

The change in maximum output power is less than 0.5 dB before and after VSWR stress which is considered to be within the limit considered as no permanent damage and the drain efficiency change is within ±2 % which is also considered to be insignificant .

Stress result discussion

Another factor that became clear from the measurement study is the impact of the forward gate current. Fig. 8 shows the gate current increase with power drive. This is a normal current increase due to forward current flowing in the diode at the gate-source of the device when the power on the input is sufficiently high to exceed the gate diode forward voltage. This diode is not dimensioned to conduct high currents and there is a limit for when material changes may occur due to high temperature and electro migration conditions. From the load impedance sweep shown in Fig. 9, it can be seen that there are unfavorable impedances where high forward current is flowing at less output power. These are clearly load impedances that should be avoided.

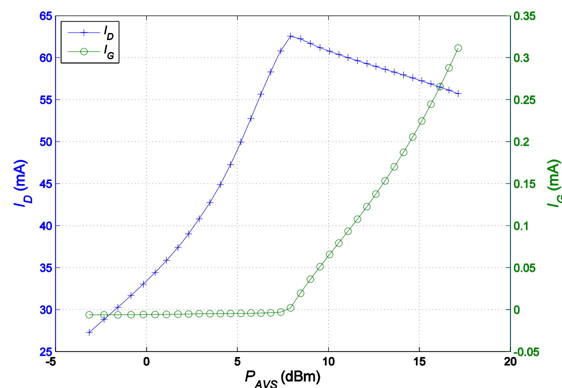

Fig. 8, Drain and gate current as a function of available input power.

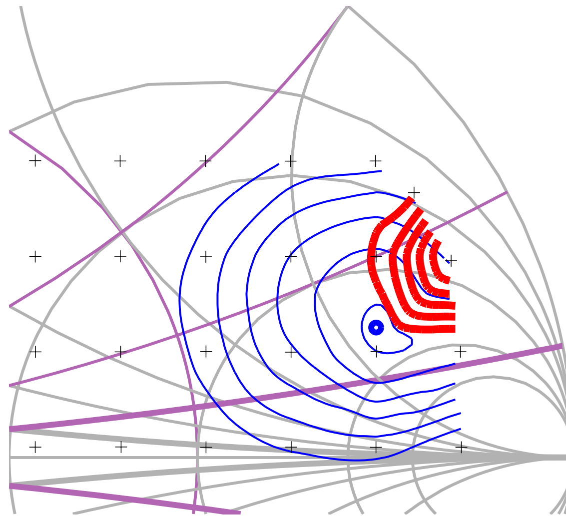

Fig. 9, P_{OUT} contours (thin-blue, -1dB contours) and forward gate current contours (bold-red, 0.5 mA contours).

IV CIRCUIT BASED HIGH VSWR PROTECTION

When the safe operating limits for the transistors have been determined, measures can be taken to prevent the voltages and current from exceeding these limits [5]. As mentioned in section II the external output matching network of the PA maps the external mismatch to impedance levels around the optimum transistor load. These transistor loads variations have a direct effect on the dynamic drain voltage and current values.

A circuit is proposed which protects the PA against high external VSWR values. The results of the stress test measurements imply that the main effect of mismatch is the increased amount of gate current. This limits the allowed mismatch applied internally to the transistors in the PA for a specific load phase. Due to the magnitude and phase of the transfer of the output matching, it is not possible to generally translate this limit to the output port of the PA. Especially the phase constraint will depend strongly on the output matching network applied. Furthermore, it is known that mismatch also influences the dissipation and therefore the channel temperature of the transistors. For these reasons the protection circuit is triggered by the magnitude of the measured reflection only. The exact protection threshold can be determined by simulation, taking into account the limits obtained from the stress measurements.

The topology of the two stage, self protecting amplifier circuit is depicted in Fig. 10. Protection is based on the measurement of reflected RF power. This reflected power is sampled and the magnitude is detected with a diode based peak detector. The output voltage of the peak detector is compared against an externally adjustable reference value with a compare and control circuit which also applies the gate bias voltage to the driver stage. If the output voltage of the peak detector exceeds the reference values, indicating that the level of reflected power is above the allowed limit, the gate bias voltage of the driver stage is reduced. This results in lower gain for the driver stage which lower the stress of the output stage.

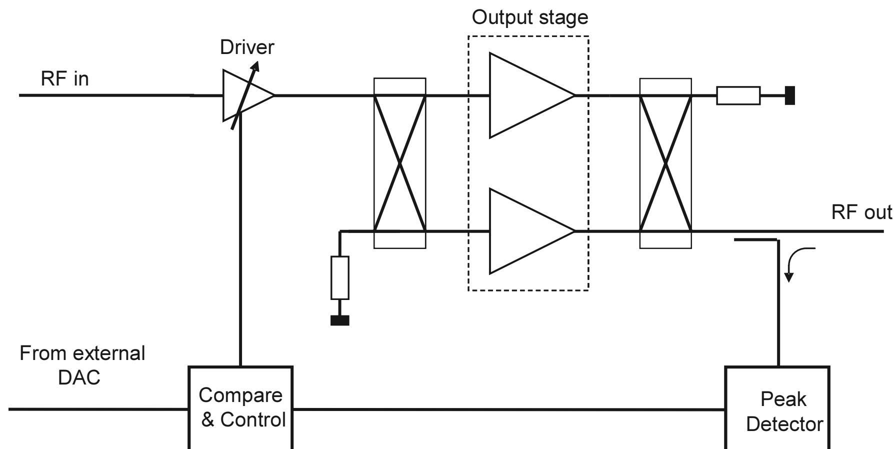

Fig. 10, Topology of feedback based self protecting SSPA.

The output stage is implemented as a balanced amplifier since this minimizes the variation in output power (and therefore the level of reflected power) as the phase of the mismatch is varied. For the balanced output stage two AlGaN/GaN power bars of FBH are used. The peak detector, comparator and control circuit and driver stage are designed in the AlGaN/GaN MMIC process of FBH, which opens the possibility for full integration with the output stage amplifier.

In the closed loop configuration the protection circuit will settle at the situation where the negative-input voltage of the comparator equals the positive-input voltage. The simulated response time of the control circuit is in the 100 ns range. The simulated gate voltage of the input stage is shown in Fig. 11. It is seen that for nominal load conditions the gate bias voltage remains nearly constant, while for higher VSWR values the bias voltage is reduced with increased output power. Fig. 12 shows the simulated dynamic load lines on one of the transistors in the output stage for VSWR values from 1:1 to 10:1. The nominal load line for VSWR=1:1 is shown in black. It can be seen that the maximum voltages and currents for higher VSWR values are only slightly higher than the nominal values, illustrating the functionality of the protection circuit. The simulated output power of the self-protecting SSPA is shown in Fig. 13. It is seen that as expected due to the gate bias reduction of the driver stage also the output power is reduced for higher VSWR values.

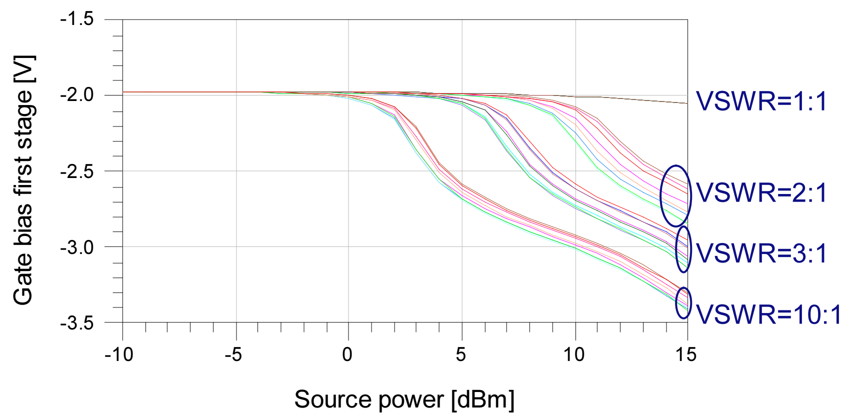

Fig. 11, Simulated gate bias voltage of input stage for various VSWR values.

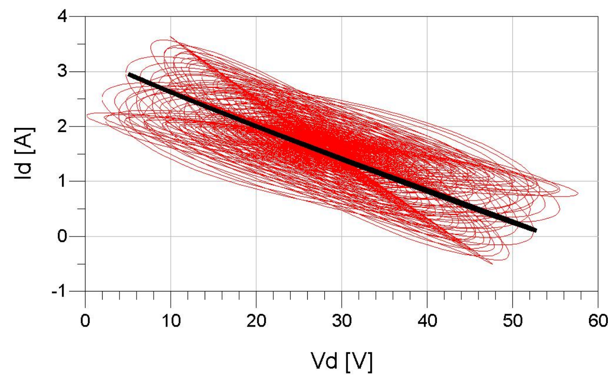

Fig. 12, Simulated dynamic load lines for VSWR from 1:1 to 10:1.

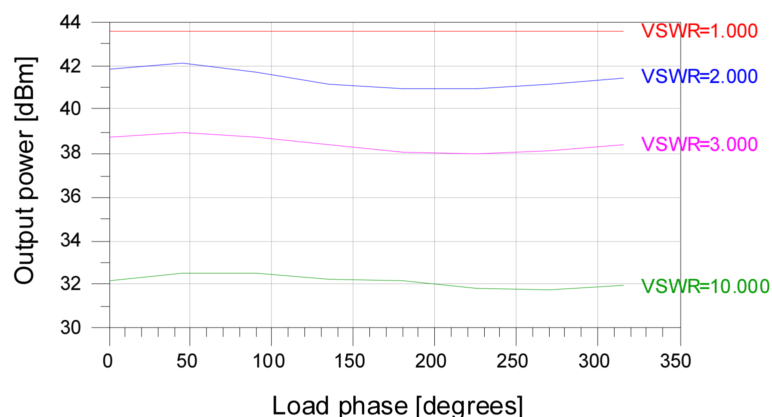

Fig. 13, Simulated output power at 1dB compression of self protecting SSPA for various VSWR values.

CONCLUSIONS

Initial results from VSWR stress tests of GaN-HEMTs has been presented together with a suggested circuit topology designed to prevent excess operation under VSWR stress. With the measurement setup, devices can be tested on-wafer under increasing VSWR stress in continuous or pulsed RF-power operation. In the measurement setup the transistors are stressed at the device interface with pulse lengths down to 20 ns. The results show no significant effect on DC parameters after burn-in and a limited 0.5 dB change in output power which is considered to be tolerable. The presented protection circuit is able to detect high VSWR conditions and limit the drive input power in a 100 ns time frame which from this study is expected to be sufficient for maintained function and reliability for the used GaN-HEMT technology.

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