

# X-band Phase Shifting Power Amplifier MMIC for Phased Array Transmit Modules

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**Abstract**— An X-band Phase Shifting Power Amplifier with six-bit phase control and 5 Watt output power has been developed and tested. The aim of the development is cost reduction for Transmit and Receive components for phased array systems. The device has been developed in the 6-inch 0.5  $\mu\text{m}$  power pHEMT process (PP50-11) of WIN Semiconductors. The use of this process results in cost effective devices with a high power capability.

**Index Terms**— MMICs, Power amplifiers, Phase shifters.

## I. INTRODUCTION

Phased array front ends contain very large numbers of Transmit / Receive (TR) modules. This implies that a cost reduction of the modules will significantly reduce the costs of an entire phased array system. The cost of TR modules is to a large extent determined by the manufacturing and packaging costs of the semiconductor components [1]. The number of different MMICs in a front end can be reduced by further integration of functionality on a single MMIC, which results in lower processing- and assembly costs. The integration of phase shifting, gain control and low noise amplification has frequently been reported during the last decade. However, very little is written on the integration of power amplification together with other typical functions for phased arrays front ends.

For the transmit part of the phased array front end the modules should at least provide phase shifting and power amplification. This paper describes an integrated Phase Shifting Power Amplifier (PSPA) consisting of a separate Phase Shifter (PHS) and High Power Amplifier (HPA) for application in such a transmit module. It is believed that this PSPA shows the trend towards a new concept for TR modules in which transmit and receive functionality are separated.

## II. DESIGN

The use of a power process for the PHS results in a device with a high compression power, which is capable of driving the HPA without the use of an additional driver amplifier. The PHS consists of six individual sections each providing a phase shift of a  $2^n$  multiple of  $5.625^\circ$ . The position of these sections within the phase shifter chain is chosen such that the highest possible compression level is obtained. At crucial positions, a resistive DC path to ground is created in order to enhance the

operating power capabilities of the PHS. Digital control logic enables the use of single ended LVCMOS compatible digital control signals [2].

The High Power Amplifier (HPA) is a three stage amplifier. The first stage consists of a single transistor while the second and third stage contain four and eight transistors respectively. All transistors have eight gate fingers with a width of  $150 \mu\text{m}$  each. The gate biasing of the HPA is performed by an active gate bias circuit with approximately 75% of compensation for threshold voltage variation. The output matching network of the HPA compensates for a bond wire inductance of approximately 200 pH. This corresponds to two bond wires in parallel. Special attention is paid to the stability of the HPA since it should be able to operate with a minimum amount of external components, i.e. bar caps on the drain bias pads only. A thorough loop gain analysis [3] is performed for various biasing, operating power and load conditions.

The layout of the MMIC is shown in Fig. 1. On the upper side the PHS is visible with on the upper right side the digital control logic. The lower part is occupied by the HPA. RF shielding is provided between the HPA and the PHS as well as between the individual phase sections. The dimensions of the MMIC are  $5.4 \times 3.9 \text{ mm}^2$ . On the wafer test structures with different parts of the design were included in order to be able to measure and evaluate certain components individually.

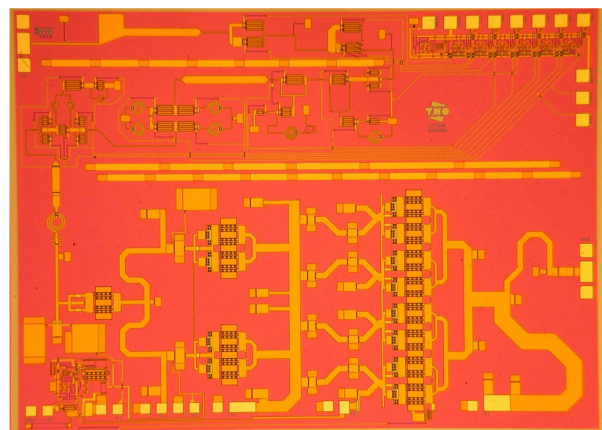


Fig. 1 Photograph of integrated PHS and HPA. Chip dimensions are  $5.4 \times 3.9 \text{ mm}^2$

### III. ON-WAFER MEASUREMENT RESULTS

To minimize the dissipation during the on-wafer measurements, these are performed under pulsed conditions with a Pulse Repetition Frequency (PRF) of 10 kHz and a pulse width (PW) of 10  $\mu$ s. This yields a duty cycle of 10 %.

The measured small signal gain is given in Fig. 2 for all 64 phase states. It is seen that the gain of the device varies within a band of approximately 1 dB. From measurements performed on the individual HPA and PHS it was found that the gain of the HPA is approximately 25 dB, while the PHS has an average loss of 6 dB.

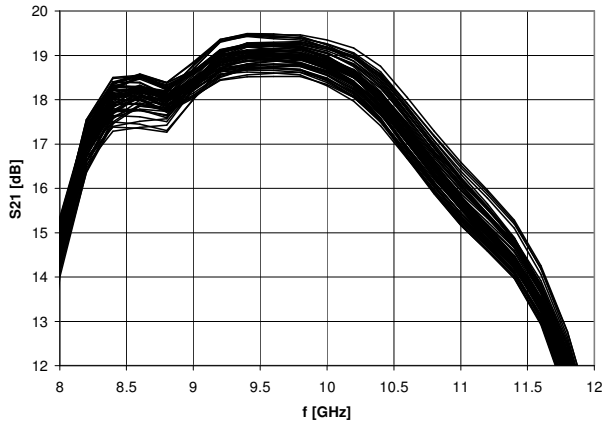


Fig. 2 Small signal gain for all states, average sample measured on-wafer at  $V_d=8$  V,  $V_{gg}=-10$  V,  $T_A=25$  °C, PRF=10 kHz, PW=10  $\mu$ s.

The measured input matching is given in Fig. 3 for all 64 phase states. It is seen the matching is better than -10 dB for all states.

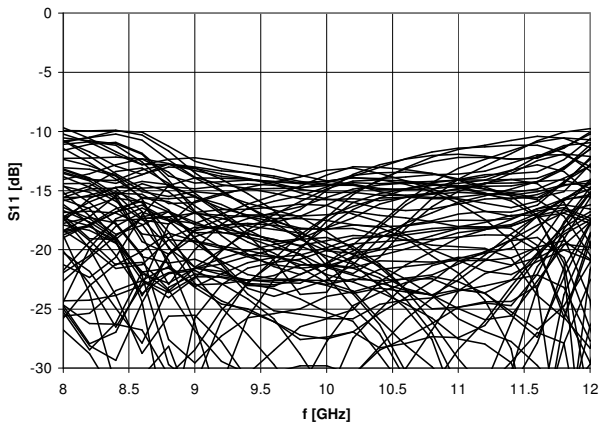


Fig. 3 Small signal input matching for all states, measured on-wafer at  $V_d=8$  V,  $V_{gg}=-10$  V,  $T_A=25$  °C, PRF=10 kHz, PW=10  $\mu$ s.

Fig. 4 shows the phase plane of the device. The device is monotone within a frequency band from 10.3 GHz to 11.3 GHz. Outside this band there is an overlap at the transition from state 31 to state 32. This is caused by the fact that the phase shift of the 180° section is approximately 7° too high. This is to be modified in a next iteration.

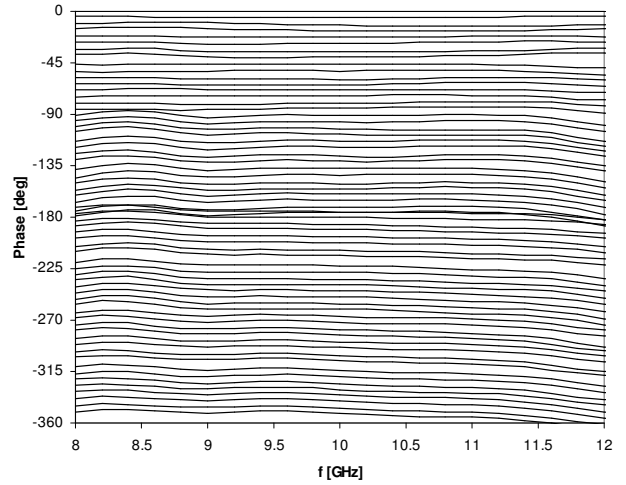


Fig. 4 Phase plane, average sample measured on-wafer at  $V_d=8$  V,  $V_{gg}=-10$  V,  $T_A=25$  °C, PRF=10 kHz, PW=10  $\mu$ s.

The small signal phase error is determined with respect to the phase in state 0 (reference state). In Fig. 5 the small signal RMS- and maximum phase error over all states are given. The main contribution to the errors comes from the 180° section.

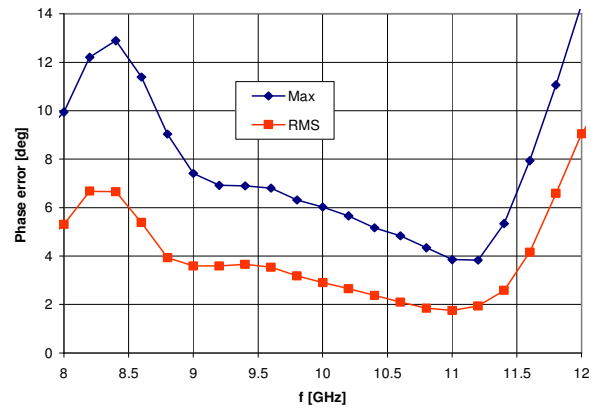


Fig. 5 Maximum- and RMS small signal phase error, average sample measured on-wafer at  $V_d=8$  V,  $V_{gg}=-10$  V,  $T_A=25$  °C, PRF=10 kHz, PW=10  $\mu$ s.

In Fig. 6 the small signal RMS- and maximum attenuation error over all states are given

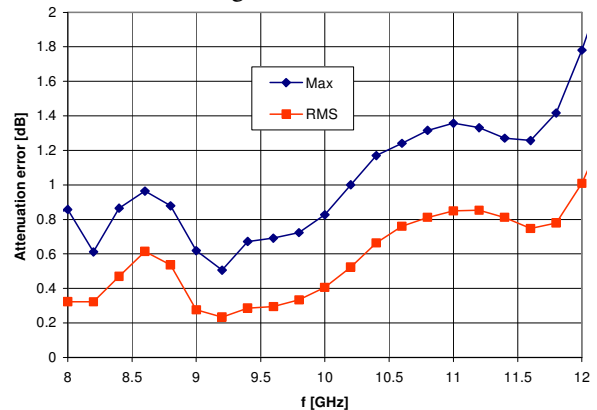


Fig. 6 Maximum- and RMS small signal attenuation error, measured on-wafer at  $V_d=8$  V,  $V_{gg}=-10$  V,  $T_A=25$  °C, PRF=10 kHz, PW=10  $\mu$ s.

The output power for all phase states is given in Fig. 7 at a source power of 21 dBm, where the compression level is approximately 2.5 dB. The output power varies between 37 dBm and 38 dBm.

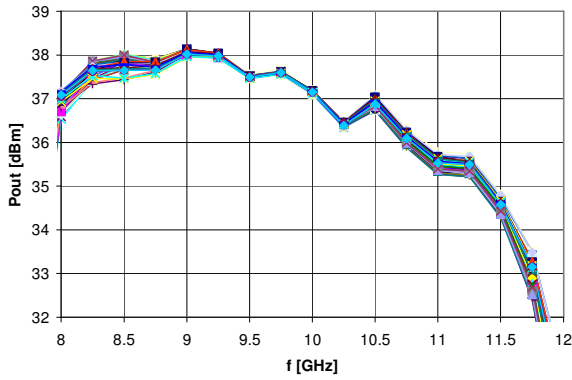


Fig. 7 Output power in all states, measured on-wafer at  $V_d=8$  V,  $V_{gg}=-10$  V,  $P_s=21$  dBm,  $T_A=25$  °C, PRF=10 kHz, PW=10  $\mu$ s.

The large signal phase error can be defined in different ways. It can be referred to the phase in the reference state at equal large signal conditions, or to the small signal phase in the reference state. Both definitions correspond to a different calibration scenario for the phased array antenna. In Fig. 8 the large signal phase error in the major states referred to the small signal reference phase is given as a function of source power at a single frequency of 9.5 GHz. It is seen that the error increases with source power and the increase becomes steeper for source powers over 16 dBm. This situation corresponds to the scenario where the antenna is calibrated under small signal conditions.

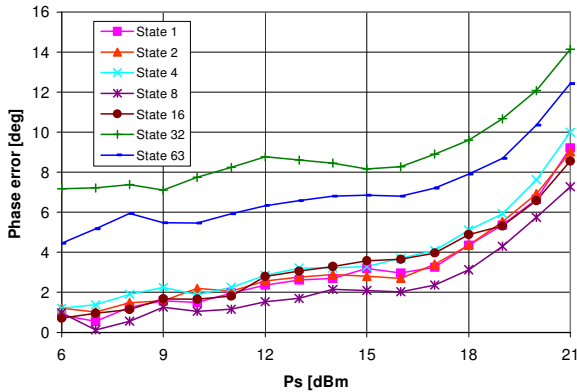


Fig. 8 Phase error in major states versus source power, referred to small signal reference phase,  $f=9.5$  GHz,  $V_d=8$  V,  $V_{gg}=-10$  V,  $T_A=25$  °C, PRF=10 kHz, PW=10  $\mu$ s.

Fig. 9 shows the large signal phase error in the major states referred to the large signal (equal power) reference phase as a function of source power at a single frequency of 9.5 GHz. For this scenario the error decreases with source power and has a minimum at the point where the HPA reaches its maximum

output power. Fig. 10 shows the RMS phase error according to this definition as a function of frequency, at a source power of 21 dBm. This situation corresponds to the scenario where the antenna is calibrated at the power level where it is eventually operated.

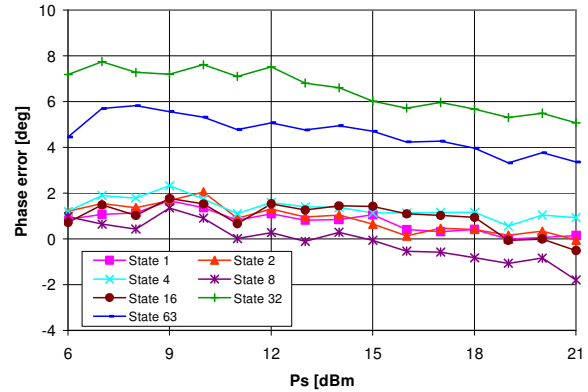


Fig. 9 Phase error in major states versus source power, referred to reference phase at equal source power,  $f=9.5$  GHz,  $V_d=8$  V,  $V_{gg}=-10$  V,  $T_A=25$  °C, PRF=10 kHz, PW=10  $\mu$ s.

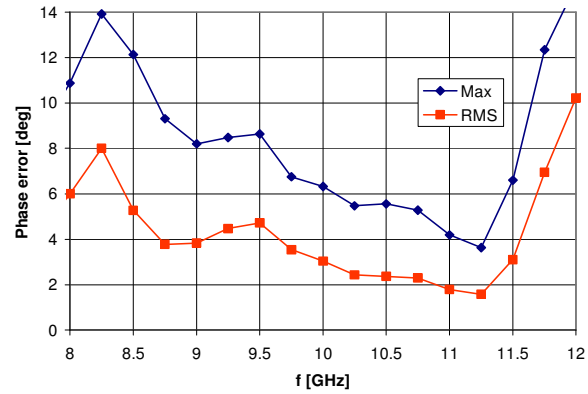


Fig. 10 Large signal maximum and RMS phase error, measured on-wafer at  $V_d=8$  V,  $V_{gg}=-10$  V,  $P_s=21$  dBm,  $T_A=25$  °C, PRF=10 kHz, PW=10  $\mu$ s.

A summary of the measured performance is given in Table 1. This table gives the worst case numbers within the frequency band from 8.5 GHz to 10.5 GHz.

TABLE I  
PERFORMANCE OVERVIEW.

Parameter	unit	value
Output power	dBm	> 37
Large signal gain	dB	> 16
Large signal gain variation	dB	< 2
Power Added Efficiency	%	> 25
Input matching	dB	< -10
RMS phase error	°	< 5 <sup>*)</sup>
RMS attenuation error	dB	< 0.8

<sup>\*)</sup> valid for  $f \geq 8.8$  GHz

#### IV. OPERATION UNDER MISMATCH CONDITIONS

The antenna element to which the PSPA will be connected might provide a fluctuating load impedance to the device. For this reason the influence of load mismatch on the operation has been measured for VSWR values up to 3:1 on samples mounted on a Copper Molybdenum carrier. Fig. 11 shows the output power of the device in the reference state at a fixed source power. It is seen that as the load varies on the VSWR=3:1 circle, the output power variation is approximately 4 dB.

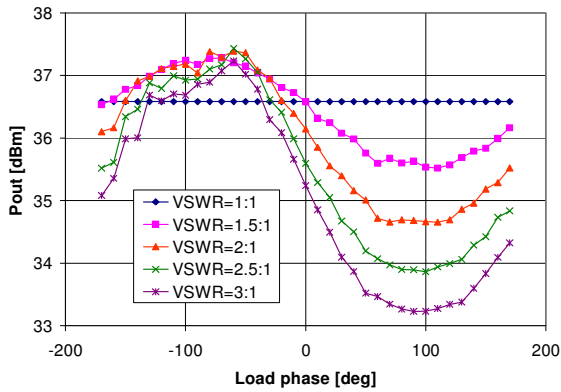


Fig. 11 Output power in reference state as function of output mismatch, measured on carrier at  $V_d=8$  V,  $V_{gg}=-10$  V,  $f=10$  GHz,  $P_s=20$  dBm,  $T_A=25$  °C, PRF=10 kHz, PW=10  $\mu$ s.

The effect on insertion phase is shown in Fig. 12. For VSWR=3:1 a phase variation of approximately  $\pm 11^\circ$  is observed. The variation is caused by the HPA which means that this variation will be equal for all phase states and will therefore not affect the phase errors of the PSPA.

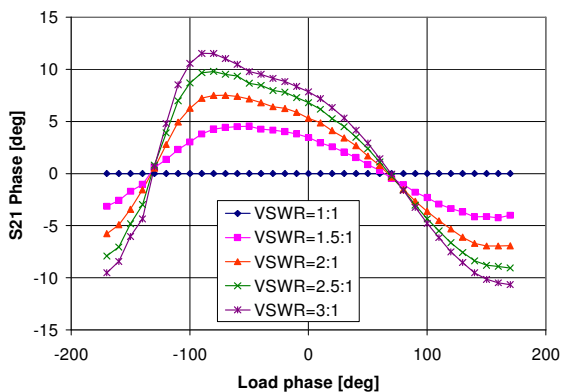


Fig. 12 Transmission phase in reference state as function of output mismatch, measured on carrier at  $V_d=8$  V,  $V_{gg}=-10$  V,  $f=10$  GHz,  $P_s=20$  dBm,  $T_A=25$  °C, PRF=10 kHz, PW=10  $\mu$ s.

The effect of mismatch on dissipated power is shown in Fig. 13. A maximum dissipation increase of 38 % is observed for VSWR=3:1. Since a higher temperature will have a negative effect on the lifetime of the devices, the additional dissipation should be taken into account when the thermal setup of the PSPA in its environment is considered.

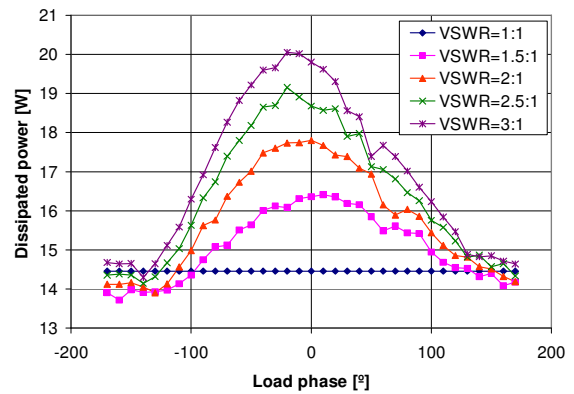


Fig. 13 Dissipated power in reference state as function of output mismatch, measured on carrier at  $V_d=8$  V,  $V_{gg}=-10$  V,  $f=10$  GHz,  $P_s=20$  dBm,  $T_A=25$  °C, PRF=10 kHz, PW=10  $\mu$ s.

#### V. CONCLUSION

A six-bit Phase Shifter integrated with a 5 Watt High Power Amplifier operating at X-band is presented here. An output power of more than 37 dBm, with an RMS phase error smaller than  $5^\circ$  is obtained. The integration of phase shifting and power amplification capabilities is major step towards the production of low cost transmit modules for phased array antenna front ends.

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